Single-bit, oversampling A-to-D converter

Erik Margan developed this simple converter for a battery-powered telemetry transmitter, which needed a signal-to-noise ratio of more than 70dB over a 5kHz bandwidth

Delta A-to-D conversion technique is probably familiar to readers of this journal; most recently, it was described in a Circuit Idea by D.J. Greaves[1]. This type of conversion is attractively simple, needing only a comparator, a D-type flip-flop, a sampling clock and a low-pass filter in the feedback loop (see **Fig. 1(a)**). In contrast to the more commonly used converters which attempt to sample the input signal as accurately as possible at each sample, delta converters make use of the oversampling technique, allowing the error to be arbitrarily large at each sample and reducing the error by averaging the samples at the output. The bit stream which is produced by clocking the flip-flop is integrated by the low-pass filter and fed back as error signal for the comparator.

This configuration has a few drawbacks, the most serious being the degraded signal-to-noise ratio with frequency, which follows the inverse characteristic of the feedback filter. The cause of this degradation lies in the progressively smaller error correction in the feedback loop which, in turn, causes slew-rate limiting and thus smaller undistorted output amplitudes at higher frequencies (**Fig. 1(b)**).

Improving s:n ratio

A rearrangement of the feedback configuration leads to another type of the delta converter, known in theory as the sigma-delta converter, but rarely used (**Fig. 2(a)**). Such a circuit has been recently described in an excellent article by R.W. Adams[2]. The difference is that the input signal is first summed with the output of the flip-flop and then the sum is filtered and compared to a DC reference. The consequence of this change is that the overload level is now flat with frequency (in the band of interest), while the noise spectrum rises with frequency, producing about the same s:n ratio (**Fig. 2(b)**).

This does not seem to be an improvement, but putting the filter after the summing stage gives us another degree

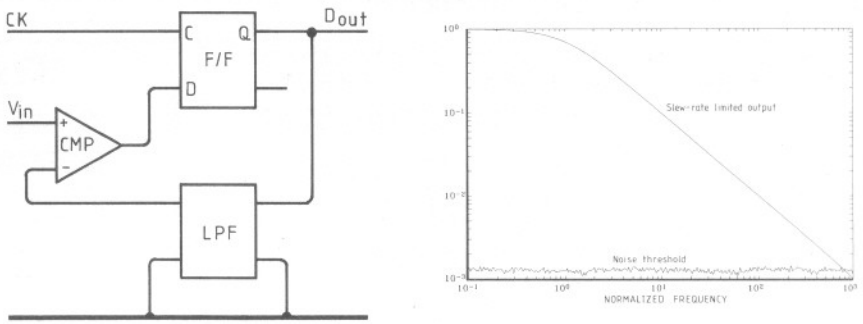

Fig. 1 The Delta-type converter circuit at (a) compares the input signal with the filtered output big stream. When following high-amplitude signals of frequency greater than the filter cut-off, the converter runs into slew-rate limiting, degrading the S/N ratio, as seen at (b).

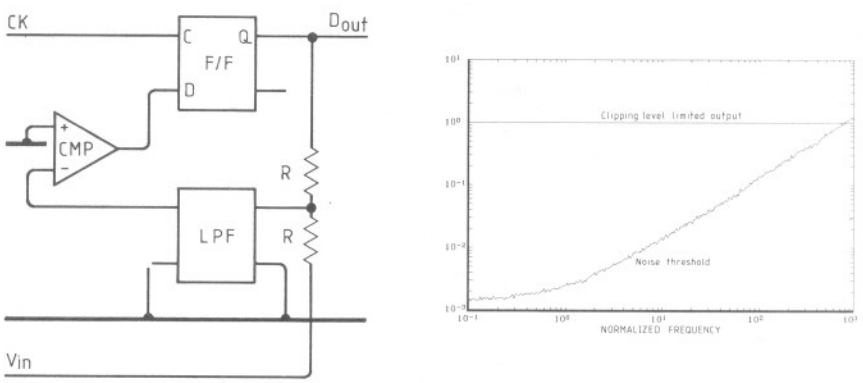

Fig. 2. The Sigma-Delta converter at (a) compares the filtered input and output signal sum to a DC reference. This eliminates the slew-rate limiting; the output level is not affected by the filter frequency response, only the noise following the inverse of the filter response shape, as in (b).

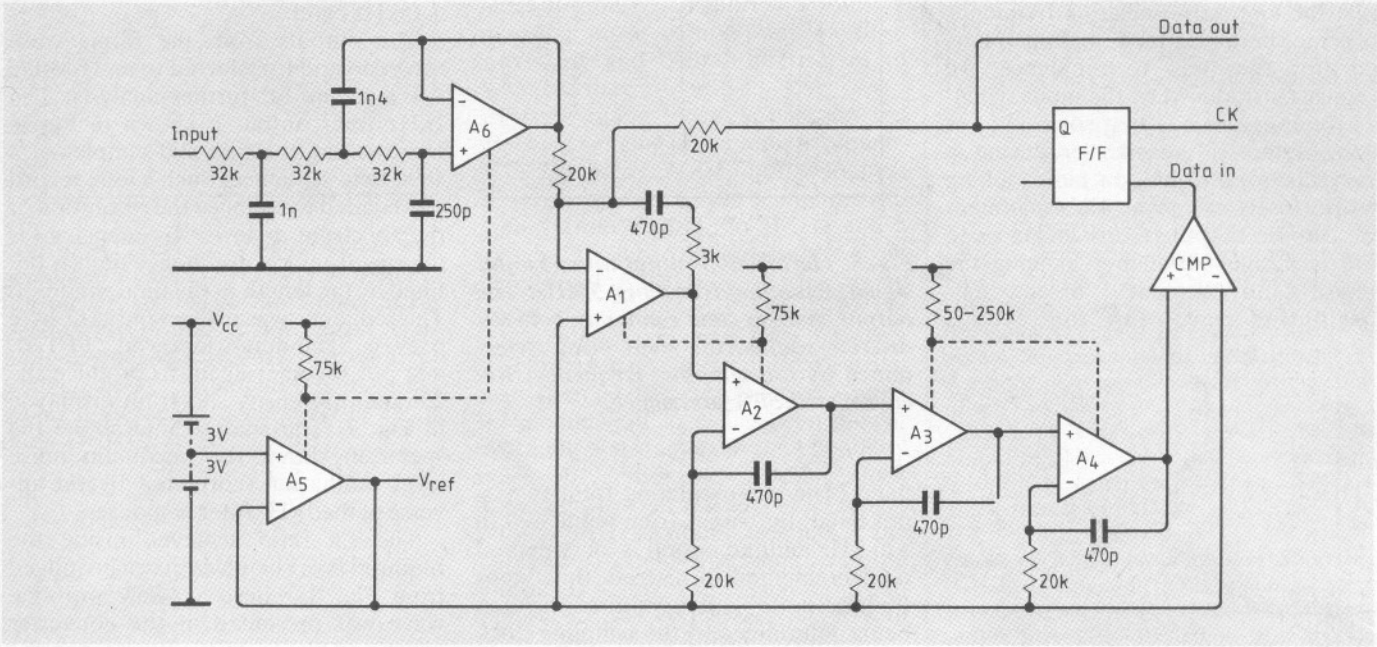

Fig. 3. The proposed circuit diagram of the Sigma-Delta type. Using the programmable c-mos op-amps and comparator (MC 14573 and Mc14575) allows us to control the stability of the feedback loop through controlling the bias and the slew-rate (a non-linear mechanism!) of the last two filter sections.

of freedom. We note that the frequency response is now flat, regardless of the filter response shape, while only the noise spectrum follows the inverse of the filter shape. From this we conclude that by making a suitable choice of filter, we can concentrate most of the noise outside the band of interest and filter it out after the conversion has been performed.

In this way, the s:n ratio can be greatly improved, but this is not an easy task. There are several points to take into account simultaneously:

- selecting optimum filter configuration to achieve required noise shaping;
- reducing the influence of the choice of sampling clock frequency on the noise spectrum;
- maintaining the stability of the closed feedback loop in the broad range of sampling clock frequencies; and
- optimising the idling pattern of the converter for low distortion (the quantisation process should introduce noise only, independently of the signal level or slope).

Each of these requirements introduces some restriction in other areas, so the system must be treated as a whole. The first two points restrict the choice of filter configuration to those with zeros and poles, implying a pronounced attenuation well above the band of interest. Circuit complexity imposes another restriction and the last two requirements are best served if we implement some kind of slew-rate control.

Adams[2] states in his article that single-bit converters are difficult to stabilize, and for that and other reasons he opted for a four-bit configuration. Using a similar filter configuration, but with four zeros and four poles, I came to the conclusion that the required feedback stability can be achieved through slew-rate control of filter amplifiers.

Design

The whole circuit is shown in **Fig. 3.** The programmable operational amplifiers A1, A2, A5 and A6 are contained in an MC14573, while A3, A4 and the comparator (CMP) are contained in an MC14575. The D-type flip-flop (F/F) is one half of a 74HC74. The signal first passes through the input anti-aliasing filter (A6 – a third-order Bessel type was found to be enough) and proceeds to the inverting integrator A1 where the input and output are summed at the virtual-earth point. This eliminates a separate summing stage. The resistor in series with the integrating capacitor sets the transfer-function zero location, and is selected so as not to saturate the comparator's input even under the lowest sampling frequency and largest signal level. The other three zeros are made equal to the first through the use of non-inverting integrators (A2, A3, A4) for the remaining filter sections, with equal RC constants defining the pole position. A further control of the filter is available through the bias control of the programmable operational amplifiers that also influences the slew rate of the signal at the comparator input. Slew-rate limiting is implemented only in the last two filter stages and is adjusted for low distortion and a stable feedback loop at the lowest sampling frequency.

As stated before, the filter is the key to the circuit. We have already stated the main requirements, but now is the time to justify the filter choice given in Fig. 3. First, as the filter is used inside the feedback loop, at least one of its stages should be configured as an integrator to ensure the stability of the loop DC level and to make it equal to the reference. This, in turn, ensures equal positive and negative clipping levels and maximises the signal dynamic range. Next, the loop must have a flat frequency response to well above the desired bandwidth to make the noise spectrum flat inside this band, thus achieving constant s:n ratio. To concentrate the noise in the upper frequency band, the loop gain must be intentionally lowered in this region. This attenuation reduces the loop error correction and, being randomly distributed, the resulting error appears as high-frequency noise.

One can hardly resist a temptation to make this attenuation as deep and as narrow as possible and this, as correctly

assumed, improves the in-band noise reduction. The price to pay, however, is that the loop self-oscillating frequency becomes better defined, making it harder for the loop to rebalance the changes introduced by the input signal. The consequence is that some kind of "bit hysteresis" results, producing a very distorted signal. In fact, looking more closely at how a "bit" is defined, we can see that the loop rebalances to the new signal level by changing the phase (and frequency) of the self-oscillating waveform; thus, for a

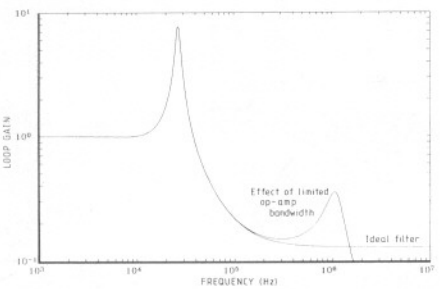

Fig. 4. The analysis of the filter continuous-time loop frequency response. Eliminating the comparator and the flip-flop and closing the filter feedback loop results in these response curves. Finite open-loop bandwidth of the filter op-amps modifies the response around 1MHz. When discrete time steps are introduced in the loop (by putting back the comparator and the flip-flop) most of the error will be produced in the response trough (100-500kHz).

smooth bit-to-bit transition, a low-Q notch is necessary.

As can be seen from **Fig. 4**, the transition from a flat response to attenuation is not smooth. The pronounced resonance peak results from the four poles of the filter being present inside the feedback loop. This peak gives a very high loop gain and reduces the noise in this band to a very low level, but this is not its main function: it is needed mainly for the high phase jump produced at the resonance, which provides an effective boundary that prevents the loop self-oscillations from breaking into the desired signal-frequency band.

Finally, the filter zeros determine the frequency response at the highest frequencies, but it is altered somewhat by the limited op-amp bandwidth (the small second peak).

Now, this continuous-time loop-analysis result is not greatly affected by the introduction of discrete time steps (the sampling clock frequency) if the steps are small enough (less than 2μs). As the feedback factor is lowest in the response trough (100-500 kHz) most of the noise will be concentrated in that

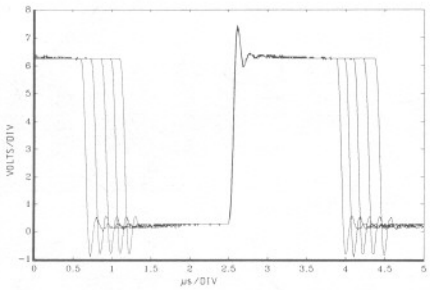

Fig. 5. The flip-flop output with no input signal. Sampling frequency 5MHz. The output changes state randomly between discrete widths, the steps being determined by the sampling frequency. Recorded with 50% pretrigger.

band. The self-oscillating frequency is not fixed, but varies from about 120 to 470 kHz and the period is incremented or decremented in discrete time steps ("phase noise"), the width of the step being determined by the sampling clock frequency (**Fig. 5**).

The effect of slew-rate limiting is not made obvious from Fig. 4. To understand it, we must visualise the time pattern of the signal at the comparator's input. The switching of the flip-flop output is transferred through the filter by the transfer-function zeros, appropriately attenuated. This is the fastest part of the waveform and slew-rate limiting will modify its slope. This slower slope introduces a delay proportional to the error produced at the current sample, the slower part of the waveform, which is due to error integration, being passed unaffected. Bear in mind that the output bit stream is undergoing constant integration, so with no input signal the average width of the high logic state equals the average width of the low logic state. If the error at the current sample is large, it will be compensated to a large extent immediately with the next opposite state width, to which the delay introduced by the slew rate limit will contribute. In this way, we have gained a fast bit-to-bit error correction, transferring the noise spectrum to higher frequencies. Fast error correction contributes also the loop stability at higher frequencies.

To evaluate the s:n performance and the noise spectrum shaping effect, the output bit stream was sent to two filters: a single pole 1kHz filter, used to evaluate the noise shaping and a 7-pole, 5kHz Bessel filter, used to evaluate the s:n ratio and signal distortion in the 5kHz bandwidth. The Bessel-type filter was used to preserve the shape of the input impulse waveform that my application required, but for other purposes a 5th-order Butterworth or Chebychev filter type would give much lower noise in the 5-15kHz band.

The outputs from the filters were recorded and transferred to an IBM PC AT machine for further analysis. The 1kHz filter output is shown in **Fig. 6** representing the first 500 samples of a 4096-byte sequence. Such a long record was needed to enhance the resolution of the spectrum at lower frequencies (as the spectrum low-frequency limit is defined by the length of the time window). The sequence was broken into 512-byte packets, Hanning-windowed, FFTed, and put together again to produce the 256-point intensity spectrum displayed in **Fig. 7**. The smooth line above the spectrum shows the maximum noise level estimation, corrected by the inverse of the 1kHz filter response.

The s:n ratio achieved inside the required 5kHz bandwidth can be judged from **Fig. 8**, where a 20mV p-p sine wave was presented at the converter input and the output signal from the 5kHz 7-pole filter was recorded. Sampling frequency was 5MHz. Here we can see that the noise peak-to-peak level is about 1mV. If we consider the fact that the system supply voltage is 6V

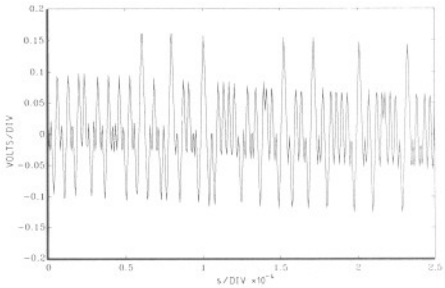

Fig. 6. Passing the output bit stream through the 1kHz single-pole filter to evaluate noise performance. The randomness of the "bit" pattern is clearly displayed. Worst case condition – 500kHz sampling frequency.

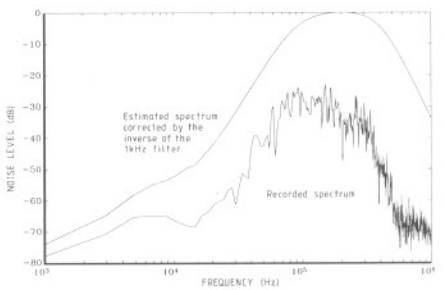

Fig. 7. Noise spectrum estimation and the resulting spectrum of the signal from Fig. 6. The effect of concentrating the noise outside the required signal frequency band (5kHz) is evident.

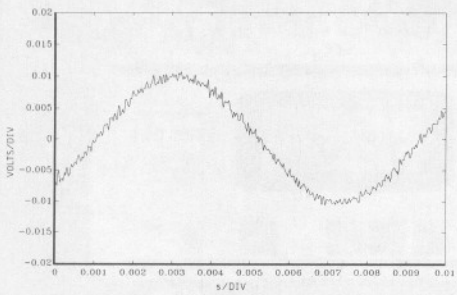

Fig. 8. A 20mV$_{p-p}$, 120Hz signal was presented to the converter and the output bit stream fed to the 7-pole, 5kHz Bessel filter produced this figure. Sampling frequency was 5 MHz. Noise level is about 1mV$_{p-p}$. Compared to the maximum undistorted signal level of 5V$_{p-p}$ gives 74 dB s:n ratio.

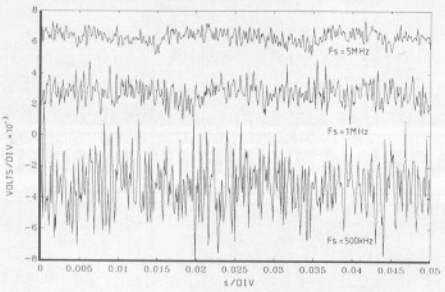

Fig. 9. Output bit stream filtered by the 7-pole, 5kHz Bessel filter, with converter input tied to the DC voltage reference. The influence of the sampling frequency to output noise is shown.

(two 3V lithium cells) and if we assume maximum undistorted output of 5V p-p, we arrive at the peak-to-peak voltage ratio of 5000:1 or 74 dB. If we take into account that the noise peak-to-average ratio is much greater than the sine-wave peak-to-average ratio, we can add some 4-6 dB, arriving at nearly 80 dB.

Further improvement in s:n performance can be achieved either by raising the supply voltage, and thus maximum input and output signal levels, or by increasing the sampling clock frequency. Unfortunately, if you insist on battery supply, this results in either prohibitive power drain, or space and weight. However, even if you renounce the battery supply you are faced with the 18V supply limit of the 4013 c-mos flip-flop used in place of the 74HC74. A CA3080 transconductance amplifier can be used instead of the feedback summing resistor, as well as in the place of MC14573, and a PMI's CMP-01 in the place of the MC14575 comparator stage, thus arriving at about 25V p-p signal swing and resulting in more than 86 dB dynamic range. On the other hand, there is little benefit if the sampling frequency is raised beyond 5MHz, since the noise at the input of the comparator and the filter-stage amplifiers determinate the final result. A better approach is to improve resolution by using more comparators (a flash converter) and digital filtering as in Adams' article[2].

Finally, in **Fig. 9**, we can compare the effect of changing the sampling frequency on the noise. A 3:1 improvement is achieved by raising the sampling frequency from 500kHz to 1MHz and a further 2:1 improvement results from increasing it to 5MHz.

A single-bit converter with flat overload level and nearly flat noise spectrum more than 70 dB below overload in the 5kHz bandwidth is, as has been shown, realisable and stable and the possibility exists of varying the sampling clock frequency in one decade-wide range. With a 1MHz sampling frequency, the s:n ratio is roughly the same as in the standard 12-bit, successive-approximation A-to-D converter system with 15kHz sampling frequency. If there is a need to convert the received data back to analogue form, a simple analogue filter will do the job. If a digital format is needed, the received bit stream can easily digitally be filtered and resampled with the required resolution at a lower rate, single-bit filtering being much simpler than 12-bit, and will easily run in real time in most cases.

The author feels greatly indebted to the excellent article by R.W. Adams, as it triggered my curiosity and offered a good guideline to this successful design.

References

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2. Design and implementation of an audio 18-bit analog-to-digital converter using oversampling techniques, R.W. Adams *Journal of the Audio Engineering Society*, vol. 34, no. 3, March 1986, p. 153-166 ■

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Useful Network Theorems, fifth edition, by Dr Harry E. Stockman. Comprehensive collection of theorems, with historical notes on their origin, applications and a set of worked problems. The theorems, some of which are contributed by the author, include those dealing with the periodic steady state and those for transient analysis. Appendices provide guidance on methods of calculation, tabular information, definitions and short biographical notes on people who have made notable contributions to network analysis. The book is in typescript form with diagrams drawn and annotated by hand; on occasion, this makes it difficult to read, since the printing quality is also rather poor. Sercolab, Box 767, E. Dennis MA, 02641, USA, 160 pages, soft covers, $11.50.

Advanced BASIC scientific subroutines, by B.V. Cordingley and D.J. Chamund, Extensive collections of mathematical and statistical subroutines, written in a structured form of Basic which should run without significant modification on IBM PCs and various other computers. Subject groupings include the generation of random numbers; probability, density and distribution functions; analysis of variance; matrix operations; interpolation; numerical analysis (Chebyshev polynomials and Fourier series); calculus; solution of equations, and complex numbers. The routines are liberally commented. Macmillan Education, soft covers, 178 pages, £9.50. The software is also available from the publishers on a disk suitable for the IBM PC.

Taming Technology: how to manage a development project by Geoff Vincent (senior consultant with PA Technology). Concise, readable, practical guide to improving one's competitive position, for both engineers and managers. Sections cover the development cycle, from concept to product launch; projects and the project leader; the need to plan, and the improved planning methods made possible by the microcomputer; creating an effective organization; and estimating cost and time. The author states persuasively the case for a scientific approach to project management, as distinct from simply playing it by ear. Kogan Page, in association with the British Institute of Management, 173 pages, hard covers, £14.95.

Electronics Sourcebook for technicians and engineers, edited by Milton Kaufman and Arthur H. Seidman. Generously-filled crib (it's nearly 45mm thick) for technicians and students, describing the properties and uses of electronic components, circuit elements and instruments of all kinds. Entries include a little theory, a lot of useful advice and, where appropriate, a scattering of worked examples. This edition is a condensed, soft-cover version of the same publisher's Handbook of Electronics Engineering Technicians. McGraw-Hill, £19.95.