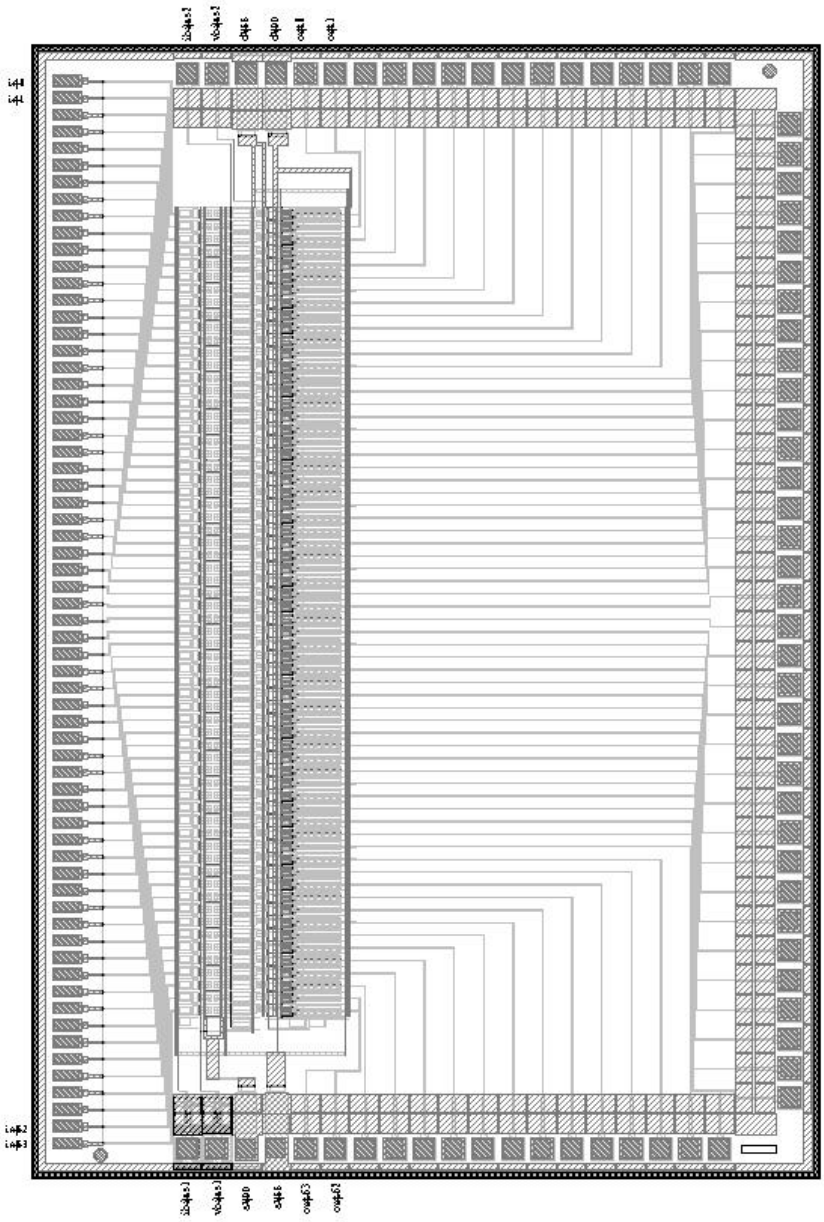
LS64



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Ideas ASA, Veritasveien 9, Box 315, N-1323 Høvik, Norway
Phone: +47 67 55 18 18, Fax: +47 67 55 96 30, E-mail: ideas@ideas.no, homepage: http://www.ideas.no
Bank: Kreditkassen, Account no: 6094.05.51881, Swift: XIAN NO KK, Enterprise Number: NO 96 56 50 776

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Introduction

The LS64 is a logic level generator that converts current logic from an open drain output transistor to (0V, DVDD) CMOS logic with DVDD in the range 2.5-5 V. The LS64 offers minimum input voltage signal swing minimizing coupling noise from the digital circuitry to the noise sensitive analog chip. The LS64 is a 64-bit wide logic level shifter with a load driving capability up to 40 pF.

2. Physical

?? Process:	0.8 µm N-well CMOS, double POLY, double METAL.	
?? Die size:	3735.0 µm x 5380.0 µm (including scribe) Thickness: ~ 600 µm	
?? Input pads:	64 + 2 current biases + 2 voltage biases	
	Pad size:	120 µm x 50µm
	Pad pitch:	80 µm
?? Output, control, test and power pads:	Pad size:	90 µm x 90 µm
	Pad pitch:	140 µm

3. Electrical

(*Simulated values, to be verified*)

Power rails: AVDD = +2 V, AVSS = -2 V
DVDD = 2.5 V – 5 V, DVSS = 0 V
AVSS and AVDD are power rails inherited from the preceding chip for which logic conversion is carried out.
DVSS and DVDD are power rails representing the low and high logic levels output by LS64. DVDD can be chosen in the range 2.5 V – 5 V.

Back contact: Connect to AVSS (-2V)

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Current draw: (*Quiescent*)	AVDD	81.6 µA x 64 channels = 5.222 mA + current bias = 240 µA
	AVSS	40.1 µA x 64 channels = 2.566 mA + current bias = 40 µA
	DVDD	res. bias 250 µA
	DVSS	41.5 µA x 64 channels = 2.656 mA + current bias = 200 µA res bias = 250 µA

Input bias currents: Nominal values
(*Current direction: positive referred to AVDD fed into the chip***)**

ibias1:	40 µA
ibias2:	200 µA

Input bias voltages: Nominal values
(Internally generated. Optionally adjustable, externally)

vbias1:	0V (= 0.5 x (AVDD + AVSS))
vbias2:	0.5 x (DVDD + DVSS)

ESD Protection: Inputs: ~600 ? series pad resistor for ibias1 and vbias1

Power dissipation *(Quiescent)*: 16.761 mW - 17.386 mW corresponding to a DVDD range of 2.5 V – 5 V

16.961 mW for 3.3 V CMOS logic

Input signal: Open drain fed to current biased cascode input current mirror.

Input node potential: - 0.87 V

4. Pad description

LS64 is a pad limited chip. The chip has 64 data inputs and a similar number for data outputs. There are 4 input bias pads, 2 for current biases and 2 for voltage biases. The chip is supplied with 4 power supplies, each with a pad. The following table summarizes the pad structure beginning clockwise from top left:

Pad name	Type	Description	Nominal value
Ibias2	ai	Input current bias	200? A
Vbias2	ai	Input voltage bias (internally generated)	0.5 x (DVDD + DVSS)
DVSS	p	Digital VSS	0 V
DVDD	p	Digital VDD	2.5-5 V
AVSS	p	Analogue VSS	-2 V
AVDD	p	Analogue VDD	2 V
Vbias1	ai	Input voltage bias (internally connected to DVSS)	0.5 x (AVDD + AVSS))

5. Layout

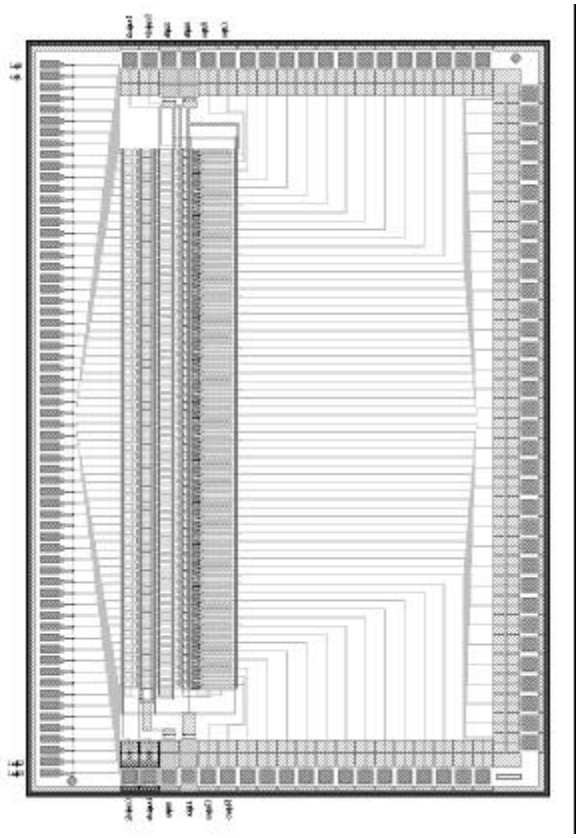

Fig. 1 Chip plot of LS64

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