MODEL 2277
32 CHANNEL CAMAC TDC

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CAUTION

Cooling

It is imperative that the module 2277 TDC be well cooled. Be sure fans move sufficient air to maintain exhaust air temperature at less than 50 C.

Installation

Crate power should be turned off during insertion or removal of modules in accordance with the CAMAC specification.

Specifications

The information contained in this manual is subject to change without notice. The reference for product specification is the Technical Data Sheet effective at the time of purchase.

Electrostatic Sensitivity

While measures have been taken to protect the MTD132 ASIC from electrostatic damage, it is still imperative to follow antistatic procedures when handling this CMOS device. Removal of the MTD132 from its socket may void the warranty.

CAUTION

LeCroy

2277 DIGITAL COUNTER TIME-TO-DIGITAL CONVERTER

- 1 nsec LSB
- 16-Bit Range, 64 μsec Full Scale
- 32 Channels Per CAMAC Module
- Common START or STOP
- Multihit Capability, 16 Measurements (Hits)/Channel
- Leading and/or Trailing Edge, Allows Pulse Width Measurements
- 20 nsec Double Edge Resolution
- Zero Pedestal
- Chip Level Zero Suppression

TDCs FOR HIGH RATE EXPERIMENTS

The 32-channel, CAMAC-based Model 2277 Digital Counter Time-to-Digital Converter (TDC) has been designed for a wide variety of timing applications. The module features a 16-bit dynamic range, 1 nsec LSB (750 psec R.M.S.) and a 16 element pipeline. The double edge resolution is below 20 nsec. The module is ideal for time measurements of drift chambers, time projection chambers or other detectors requiring time interval measurements with high accuracy.

The Model 2277 can be operated in either a COMMON STOP or COMMON START mode. At the end of the acquisition period, the time elapsed between each hit and the COMMON STOP or START along with the address of the associated channel may be read out via CAMAC. The data is automatically zero suppressed. A trigger port with prompt outputs is also provided.

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FUNCTIONAL DESCRIPTION

The Model 2277 Digital Counter TDC is a CAMAC instrument for the measurement of multiple time intervals, accurate to 1 nanosecond for time ranges greater than 64 microseconds.

The times are measured with respect to a common reference time mark or "COMMON HIT", which can occur (before) or (after) the individual time signal (also called "HIT") inputs to be measured. This common reference concept is appropriate when the relative times between (one input channel) and (any other input channel) is of interest, since they are both measured with respect to a common time. It is also appropriate for absolute time measurements between (the individual signal inputs) and (the reference itself).

Because many experiments will need many time measurements, the 2277 has incorporated a large number of independent signal channels (however, single measurements are just as appropriate). In addition, each individual input channel has a FIFO type buffer attached to it such that up to 16 hits can be recorded on the channel with respect to the common hit.

The 2277 inputs are an edge sensitive design. Consequently the polarity of the logic signal inputs is selectable. The module will record the time of the rising, falling, or both signal edges.

Common Start and Common Stop Modes

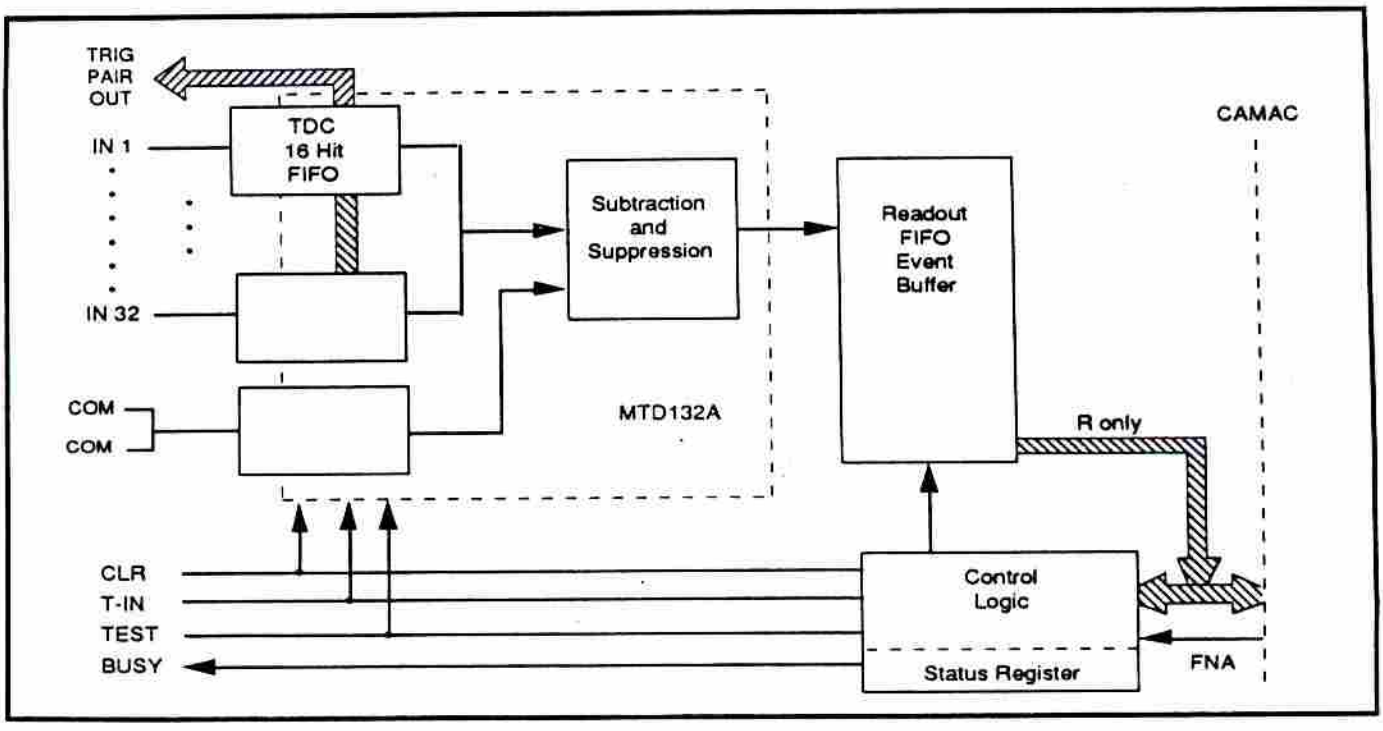
When the common reference time precedes the signal times, the 2277 is operating in a "COMMON START" mode. Alternatively, if the inputs precede the reference the "COMMON STOP" mode is used. Of course, by adding delays to the common or individual signals either mode can be used.

Common start mode is typically preferred in synchronous situations, such as colliding beam accelerators or pulsed laser experiments, when the time interval to be measured can be associated in time with a causal effect. In common start mode, a time window for the measurements must also be provided to terminate the measuring process. This can be internally generated (in the 2277) or (supplied from an external source via a front-panel input).

Common stop mode is better suited to (continuous beam) or (randomly occurring events) when a trigger decision is required.

Operation of the TDC

The 2277 must be configured and operated from CAMAC. The configuration of the module is determined by the status register. The data value stored in the register is decoded as a bit pattern (see Table 1). The bit pattern permits the mode selection, internal time window duration, edge sensitivity, test features and trigger output type. Once the status register is configured time measurement can be made.



Model 2277 Block Diagram

The actual measurements are a combination of front panel signals and CAMAC commands. A typical operation sequence begins with a CAMAC Clear command or pulse on the CLR input. This readies the module for data taking. The registration of individual hits and common hits begins automatically. At the completion of the measurement, (a time-out in common start mode from the internal timer or front-panel T-IN input, or the arrival of a hit in common stop mode) the embedded data processor takes over. This processor primarily does two things. It combines the individual hit marks and the common mark to produce the time data desired, and it suppresses data which results in a zero or overflow condition. The accumulated data is passed to a readout FIFO in the 2277. During this process a BUSY signal is output from the front panel. The busy condition can also be monitored by CAMAC.

The data can now be read through CAMAC to the host computer. Readout is accomplished with a single CAMAC function code. The channel number associated with each data value is passed along with it. In fact, readout can begin as soon as the embedded processor has transferred the first word into the 2277 readout FIFO. In this way, ("conversion" time and data transfer time can overlap, resulting in reduced dead-time and increased data throughput. The readout is complete when both Busy and CAMAC Q are returned as zero.

If for some reason the data is not read, it can be cleared. This restarts the data acquisition cycle again.

Test Features

The 2277 contains an internal pulse generator so that signals can be injected to verify the behavior of each channel. The internal tester is controlled by the status register. In addition, there is a front panel TEST input so an external pulse generator can be used.

Additional Features and Applications

Prompt hit information is presented at the front panel TRIG PAIR OUT port for inclusion in first level trigger decisions. The input channels are paired and OR'd together. A hit on either channel of the pair produces a pulse or latched output bit. These outputs are designed to match the LeCroy ECLine programmable trigger logic standard.

By capturing both the leading and trailing edge time information, the 2277 can be used in a time-over-threshold technique to simultaneously determine time and charge from a given detector element. This low cost technique avoids many of the traditional problems of using ADCs and TDCs together.

This TDC is based on the LeCroy MTD132A Monolithic Time Digitizer chip. The 2277 is essentially identical to the Model 1177 VME TDC and is similar to the Model 1877 FASTBUS TDC. For this reason the 2277 is an ideal testbed for chamber developments.

SPECIFICATIONS

GENERAL

Channels: 32, differential ECL inputs. Impedance 112 Ω. Unused inputs/outputs are allowed to float.
COMMON START/STOP: Front-panel ECL 2-pin connectors; 112 Ω terminating resistors.
Range: 16 bits.
Full Scale: 65.535 µsec.
Sensitivity (Resolution): 1 nsec least count, (750 psec R.M.S.).
Double Edge Resolution: < 20 nsec.
Long Term Stability: 10 ppm/year.
Integral Non-Linearity: None (0%).
Differential Non-Linearity: < ±20%.
Digital Clear: 100 nsec.
Buffering: 4.3 µsec + 533 nsec per hit.
Data Format: 16 bits data, 1 bit edge polarity, 5 bits channel address.
Power: -24 V at < 25 A; -6 V at < 2 A; +6 V at < 1 A; +24 V at < 20 mA.
Mechanical: #1 CAMAC Module according to IEEE-583 Standard.
Weight: 1.5 lbs. (0.7 kg).

FRONT PANEL LEDs

N:	Red LED indicates accessing module.
MODE:	Bicolor LED. Green indicates COMMON START. Red indicates COMMON STOP.
HIT:	Yellow LED indicates whether any channel received a hit.
COM HIT:	Green LED indicates whether a COMMON START/STOP was received.

INPUT SIGNALS

All inputs are differential ECL signal standard.

IN 0-31:	32 channel inputs.
COM:	2 bridged connectors.
CLR:	Clear; resets module - aborts conversion.

T-IN: Time out; terminates COMMON START acquisition window.

TEST: Used to provide test pulses to the odd and even numbered channels.

OUTPUT SIGNALS

TRIG PAIR OUT: 16 outputs - pairwise OR'd channels.

BUSY: Indicates front end disabled due to buffering and readout.

CAMAC COMMANDS

F(0)•A(0): Read Data. Q = 1 if valid data. Q = 0 if FIFO is empty.

F(1)•A(0): Read Status Register.

F(8)•A(0): Test LAM. Q = 1 if LAM is set.

F(9)•A(0): Clear. F(9) does not affect status register.

F(10)•A(0): Clear LAM.

F(17)•A(0): Write Status Register.

F(24)•A(0): Disable LAM.

F(25)•A(0): Test Cycle.

F(26)•A(0): Enable LAM.

F(27)•A(0): Test "Buffering in Progress". Q = 1 if true.

F(27)•A(1): Test Busy. Q = 1 if Busy is true.

Notes

1. Any CAMAC command must be accompanied by a valid N (Station Number).
2. An X = 1 response is generated for any valid CAMAC command.

STATUS REGISTER BIT CONFIGURATIONS

BIT(S)	CONTROL FUNCTION	PATTERN	VALUE
16	MODE	0	COMMON STOP
		1	COMMON START
15, 14, 13 Controlled	COMMON START TIMEOUT	000	Front Panel
		001	1024 nsec
		010	2048 nsec
		011	4096 nsec
		100	8192 nsec
		101	16384 nsec
		110	32768 nsec
		111	65536 nsec
12	HIT LEADING EDGE RECORDING	0	DISABLE
		1	ENABLE
11	HIT TRAILING EDGE RECORDING	0	DISABLE
		1	ENABLE
10	EVEN CHANNEL TEST INPUT	0	DISABLE
		1	ENABLE
9	ODD CHANNEL TEST INPUT	0	DISABLE
		1	ENABLE
8	TRIGGER MODE	0	PULSE
		1	LATCH
4, 3	TESTER HIT DURATION	00	128 nsec
		01	256 nsec
		10	1024 nsec
		11	2048 nsec
2, 1	TESTER HIT BURST	00	1 hit
		01	2 hits
		10	4 hits
		11	8 hits

General Information

1.1 Purpose

This manual is intended to provide instruction regarding the setup and operation of the LeCroy Model 2277 Time to Digital Converter. In addition, it describes the converter's theory of operation and presents information regarding its function and application.

1.2 Unpacking and Inspection

It is recommended that the shipment be thoroughly inspected immediately upon delivery. All material in the container should be checked against the enclosed Packing List and shortages reported promptly. If the shipment is damaged in any way, please notify the Customer Service Department or the local field service office. If the damage is due to mishandling during shipment, you may be requested to assist in contacting the carrier in filing a damage claim.

1.3 Warranty

LeCroy warrants its instrument products to operate within specifications under normal use and service for a period of one year from the date of shipment. Component products, replacement parts, and repairs are warranted for 90 days. This warranty extends only to the original purchaser. Software is thoroughly tested, but is supplied "as is" with no warranty of any kind covering detailed performance. Accessory products not manufactured by LeCroy are covered by the original equipment manufacturers' warranty only.

In exercising this warranty, LeCroy will repair or, at its option, replace any product returned to the Customer Service Department or an authorized service facility within the warranty period, provided that the warrantor's examination discloses that the product is defective due to workmanship or materials and has not been caused by misuse, neglect, accident or abnormal conditions or operations.

The purchaser is responsible for the transportation and insurance charges arising from the return of products to the servicing facility. LeCroy will return all in-warranty products with transportation prepaid.

This warranty is in lieu of all other warranties, express or implied, including but not limited to any implied warranty of merchantability, fitness, or adequacy for any particular purpose or use. LeCroy shall not be liable for any special, incidental, or consequential damages, whether in contract, or otherwise.

1.4 Product Assistance

Answers to questions concerning installation, calibration, and use of LeCroy equipment are available from the Customer Service Department, 700 Chestnut Ridge Road, Chestnut Ridge, New York, 10977-6499, (914) 578-6030, or your local field service office.

1.5 Maintenance Agreements

LeCroy offers a selection of customer support services. For example, Maintenance Agreements provide extended warranty that allows the customer to budget maintenance costs after the initial warranty has expired. Other services such as installation, training, on-site repair, and addition of engineering improvements are available through specific Supplemental Support Agreements. Please contact the Customer Service Department or the local field service office for details.

1.6 Documentation Discrepancies

LeCroy is committed to providing state-of-the-art instrumentation and is continually refining and improving the performance of its products. While physical modifications can be implemented quite rapidly, the corrected documentation frequently requires more time to produce. Consequently, this manual may not agree in every detail with the accompanying product and the schematics in the Service Documentation. There may be small discrepancies in the values of components for the purposes of pulse shape, timing, offset, etc., and, occasionally, minor logic changes. Where any such inconsistencies exist, please be assured that the unit is correct and incorporates the most up-to-date circuitry.

1.7 Software Licensing Agreement

Software products are licensed for a single machine. Under this license you may:

- Copy the software for backup or modification purposes in support of your use of the software on a single machine.
- Modify the software and/or merge it into another program for your use on a single machine.
- Transfer the software and the license to another party if the other party accepts the terms of this agreement and you relinquish all copies, whether in printed or machine readable form, including all modified or merged versions.

1.8 Service Procedure

Products requiring maintenance should be returned to the Customer Service Department or authorized service facility. If under warranty, LeCroy will repair or replace the product at no charge. The purchaser is only responsible for the transportation charges arising from return of the goods to the service facility. For all LeCroy products in need of repair after the warranty period, the customer must provide a Purchase Order Number before any inoperative equipment can be repaired or replaced. The customer will be billed for the parts and labor for the repair as well as for shipping. All products returned for repair should be identified by the model and serial numbers and include a description of the defect or failure, name and phone number of the user. In the case of products returned, a Return Authorization Number is required and may be obtained by contacting the Customer Service Department in your area.

Product Description

2.1 Introduction

The LeCroy Model 2277 provides 32 channels of either common start or common stop multihit Time to Digital Conversion designed for elementary particle or nuclear physics experiments. All input time signals to be measured ('hits') are received via differential ECL (dECL) front panel inputs. Each channel exhibits 1 nsec resolution (LSB) and can store up to 16 hits within a 65 μsec range. The time measurement is performed using the MTD132, a full custom ASIC developed by LeCroy Corporation.

2.2 Product Description

The 2277 can be programmed to operate in either common start or common stop mode. When operating in Common Start Mode, a hit window is necessary. This window of up to one full scale may be controlled via the front panel or by programming three bits within the control register. If none is provided, the hit window defaults to full scale or 65 μsec. See sections 4.2 and 4.4 for further details regarding common start and common stop modes.

Each 2277 has 32 channels of front panel inputs and a common input. All inputs are dECL and are terminated by an impedance matching network. Each channel can store up to 16 hits and can be programmed to detect leading and/or trailing edges. Selected edges can be detected with as little as 20 nsec of time separating them. If more than 16 hits occur per channel, the last 16 hits are retained. Two common inputs exist for easy board to board distribution using a "daisy chain connection".

Readout can occur as quickly as 5.12 μs after the end of acquisition. Acquisition ends with either a common stop pulse or a timeout for common stop and common start modes respectively. The MTD132s inherently sparsify the data, so time is not wasted reading out empty channels. The data of the 2277 is readout as a 22 bit word. The least significant 16 bits are the data; the next bit is the hit phase (denoting leading or trailing edge); and the next 5 most significant bits are the channel information.

Trigger outputs are provided on the front panel in dECL. For trigger purposes only, the input pulses are pairwise OR'ed (0 & 1, 2 & 3, etc.).

The functionality of the 2277 can be tested using either an internal tester or a front panel dECL test input. The internal tester can be programmed to produce 1, 2, 4 or 8 pulses with durations of 128, 256, 1,024, or 2,048 nsecs. Either or both edges of the pulses are selectable for detection, creating up to 16 internal hits per channel. Internal tester hits may be applied to odd and/or even channels simultaneously. Channels may also be tested by supplying pulses via the TEST front panel input and selecting odd and/or even channels by programming the status register accordingly. Testing can be performed in both Common Start and Common Stop Modes.

2.3 Specifications

Please refer to the model 2277 technical data sheet for a complete summary of all relevant specifications.

2.4 Front Panel

Below is a picture of the front panel of the Module 2277 TDC

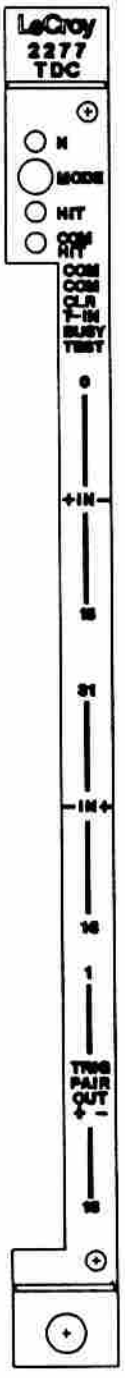


Figure 2-1 2277 Front Panel - Not drawn to size.

2.5 Controls and Connectors

Four LEDs on the front panel of the 2277 indicate status of operation. The first is the N LED. It flashes red when the module is addressed via CAMAC. The second is a bi-colored mode LED. If colored green the module is in a Common Start Mode, and if colored red it is in a Common Stop Mode. The third LED flashes yellow if a pulse (HIT) is detected on any of the 32 channels or the TEST input. The final LED flashes green when a COMMON HIT (ie. start or stop) occurs.

The first header, or the upper most five inputs, receives the control signals for the board. For further explanation of the front panel control signals see section 4.4. The next two headers marked IN receive the hit inputs. The first sixteen hit inputs are numbered in ascending order from 0 to 15, while the last sixteen hit inputs are numbered in descending order from 31 to 16. The bottom pair of pins on the first header and the top pair of pins on the next header should be properly grounded. The final front panel header marked TRIG PAIR OUT provides signals for triggering purposes and is numbered in ascending order from 1 to 16. The bottom pair of pins on the TRIG PAIR OUT header should be properly grounded. All front panel inputs and outputs are briefly described below.

- **COM:** A dECL input used to receive the common hit. The leading edge of the signal is latched. Two inputs and socketed terminators are present to aid in daisy chaining boards together. See section 4.7 for further information on daisy chaining the 2277.
- **CLR:** A dECL input used to clear the board. The on board memory is cleared, but the control word maintains its integrity. The board is ready to accept hits 60 nsec after the trailing edge of the clear pulse which must have a width of at least 20 nsec.
- **T-IN:** A dECL input used to receive the common start timeout. The trailing edge of the timeout marks the end of acquisition in Common Start Mode. If the front panel common start timeout does not end within 65 µsec after the leading edge of the common hit (start) pulse, the 2277 is automatically disabled.
- **BUSY:** A dECL output which indicates when the front_end is prohibited from accepting hits. The 2277 will not register hits while BUSY is true.
- **TEST:** A dECL input used to aid in test and calibration by providing a test hit to the even and/or odd channels at one time, depending on the status of the control register. The 2277 can be programmed to latch the leading and/or the trailing edges of the pulses.
- **IN:** All 32 dECL inputs are used to receive individual channel hits. The 2277 can be programmed to latch the leading and/or the trailing edges of the pulses.
- **TRIG PAIR OUT:** All 16 dECL outputs provide signals to be used for external triggering. Input pulses are pairwised OR'ed (0 & 1, 2 & 3, etc.) to create each output pulse. The 2277 can be programmed to provide triggering in either a latched mode or a pulsed mode. See section 4.3 for a complete description of latched versus pulsed modes.

2.6 CAMAC Commands and Functions

In typical operation, the crate controller issues a CAMAC command which includes specifying a station number (N), a subaddress (A), and a function code (F). In response, the module will generate a valid command accepted or a X response. If the command requires a response, the module will act on the command and produce a Q response. For further information on CAMAC protocol, read "Introduction to CAMAC" found in the LeCroy Research Instrumentation Catalog. The commands recognized by the 2277 are listed and briefly described below.

- **(F0·A0·S1) Read Data:** The data can be read as soon as the module produces a Look-at-Me (LAM). This can occur as quickly as 5.12 µs after the COMMON STOP HIT or the COMMON START TIMEOUT. The 2277 needs no subaddressing for proper readout. If the data word read is valid, a Q equal to one will be generated. The end of valid data occurs when a word is read out with Q equal to zero and Buffering in Progress is false. See section 2.8 for data word bit

definitions.

- **(F1·A0·S1) Read Status:** This command allows the user to read status of the control register. Both an X and a Q response will be generated.
- **(F8·A0·S1) Test LAM:** This command presents the state of the Look –at–me (LAM) on the Q bus line. An X response will always be generated and a Q response will be generated if a Look–at–me is present.
- **(F9·A0·S1) Clear:** Command clears all channels of the module, but maintains the integrity of the control register. Either a front panel or a CAMAC clear must be issued to reenable the module for acquisition if the entire event has not been readout. The 2277 is ready to accept hits 60 nsec after the trailing edge of the clear arrives at the board. Both an X and a Q response will be generated.
- **(F10·A0·S1) Clear LAM:** Clears the LAM source in the module. Both an X and a Q response will be generated.
- **(F17·A0·S1) Program Status:** Programs the control register which controls the operating mode of the module. Both an X and a Q response will be generated. See section 2.7 for status bit definitions.
- **(F24·A0·S1) Disable LAM:** Disables the LAM source. Both an X and a Q response will be generated.
- **(F25·A0·S1) Test Cycle:** This command creates an internal tester cycle as determined by the control register. An F25·0·S1 should only be done when the board is in acquisition mode, meaning the 2277 has been cleared and is waiting for hits. Both an X and a Q response will be generated.
- **(F26·A0·S1) Enable LAM:** This command enables the Look–at–Me source. The module powers up with the LAM already enabled. Both an X and a Q response will be generated.
- **(F27·A0·S1) Test BIP:** This command allows the user to determine the status of the Buffering In Progress signal. While BIP is true, the data is being buffered and the data is not guaranteed to be ready. An X response will always be generated and a Q response will be generated if BIP is true.
- **(F27·A1·S1) Test BUSY:** This command allows the user to determine the status of the BUSY signal. While BUSY is true, the 2277 front end is disabled and will not latch hits. An X response will always be generated and a Q response will be generated if BUSY is true.
- **(C+Z·S2) Master Reset:** A C or a Z clears all channels and resets the control register to zero. Both an X and a Q response will be generated.

2.7 Control Word

The Model 2277 has a 16 bit control register which controls the acquisition mode, the common start timeout, leading and trailing edge selection, even and odd channel test input selection, the trigger mode and the internal test patterns. The control register may be programmed using the CAMAC code, F17·A0·S1. The value of the control register can be read with the CAMAC code, F1·A0·S1. See table 2–1 below for individual bit definitions.

After a power–on, the state of the control register is undetermined. The CAMAC initialization function C or Z will set the control register to zero. The control register must be programmed before it will register hits. The CAMAC clear function (F9·A0·S1) has no effect on the control register.

The functions of the 16 control register bits are:

- **Acquisition Mode:** Bit 16 determines whether the module will operate in (common start) or (common stop mode). When a one is written the board operates in common start mode, and when a zero is written the board operates in a common stop mode. When read, the status of the bit is presented.

- **Common Start Timeout:** Bits 13–15 determine the length of the common start timeout. The timeout can be provided via the front panel in which case bits 13–15 should be zeroes, or a timeout between 1,024 nsec and 65,536 nsec can be programmed. When read, the status of the bits is presented.

- **Hit Leading Edge:** Bit 12 determines whether the 2277 will latch the leading edges of the hits (received via the front panel connector marked IN, the front panel connector marked TEST or from the internal tester). When a one is written the leading edges of the hits are latched, and when a zero is written the leading edges of the hits are not latched. When read, the status of the bit is presented.

- **Hit Trailing Edge:** Bit 11 determines whether the 2277 will latch the trailing edges of the hits (received via the front panel connector marked IN, the front panel connector marked TEST or from the internal tester). When a one is written the trailing edges of the hits are latched, and when a zero is written the trailing edges of the hits are not latched. When read, the status of the bit is presented.

- **Even Channel Test Input:** Bit 10 determines whether the even channels of the 2277 will latch the test inputs (received via the front panel connector marked TEST or the internal tester). When a one is written the even channels of the 2277 will latch test hits, and when a zero is written the even channels will not latch test hits. When read, the status of the bit is presented.

- **Odd Channel Test Input:** Bit 9 determines whether the odd channels of the 2277 will latch the test inputs (received via the front panel connector marked TEST or the internal tester). When a one is written the odd channels of the 2277 will latch test hits, and when a zero is written the odd channels will not latch test hits. When read, the status of the bit is presented.

- **Trigger Mode:** Bit 8 determines whether the 2277 will present (a latched) or (a pulsed trigger output). When a one is written, the 2277 will latch the hit for a given channel and the corresponding signal coming out of the front panel connector marked TRIG PAIR OUT will remain true until the module is cleared. When a zero is written, the 2277 will provide a dECL pulse via the front panel connector marked TRIG PAIR OUT each time a given channel receives a hit. When read, the status of the bit is presented.

- **Unused:** Bits 5–7 are not used. However the bits are physically available, thus they may be programmed to any status. When read, the status of the bits is presented.

- **Tester Hit Duration:** Bits 3 and 4 determine the width of the internal tester's hit pulses. The width can be programmed to be 128, 256, 1,024, or 2,048 nsec when a 0, 1, 2 or 3 are written respectively. When read, the status of the bits is presented.

- **Tester Hit Burst:** Bits 1 and 2 determine the number of pulses the internal tester will create. The internal tester can be programmed to create 1, 2, 4 or 8 pulses when a 0, 1, 2 or 3 are written respectively. When read, the status of the bits is presented.

Note the X's represent used bits and the *'s represent unused bits.

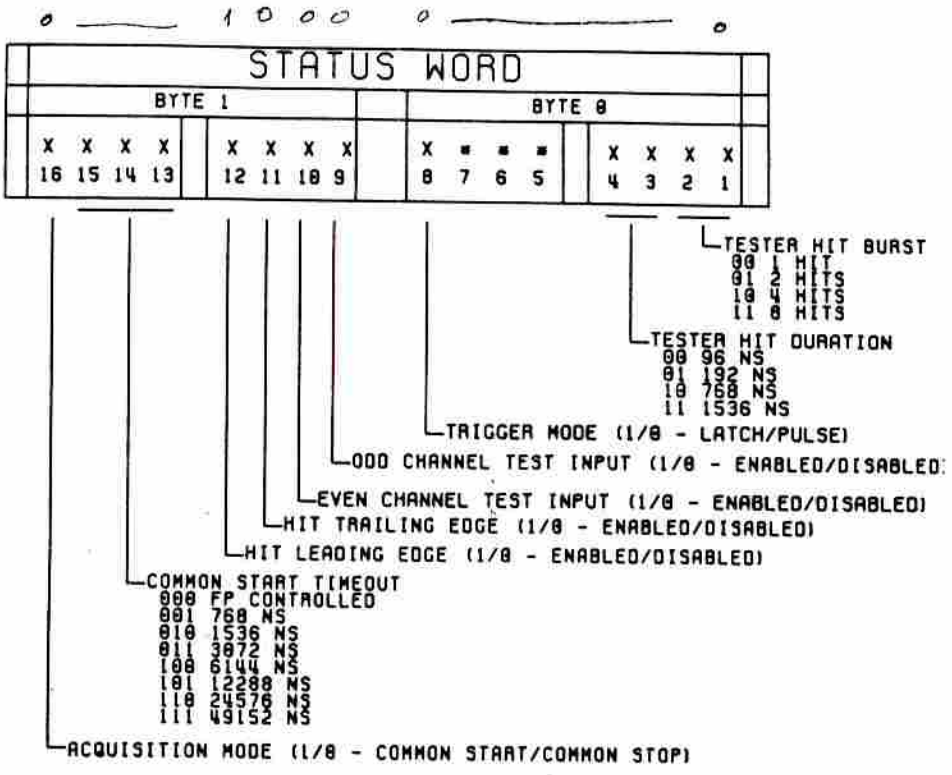


TABLE 2-1 Status Word Definition

2.8 Output Word

The 2277 data is read out as a 22 bit data word. The 16 least significant bits are the data, the next bit is the hit phase (denoting leading or trailing edge), and the next 5 bits are the channel information. The hit phase is one for a leading edge hit and zero for a trailing edge hit. The data can be read from the board using the CAMAC code, F0·A0·S1; no subaddressing is necessary.

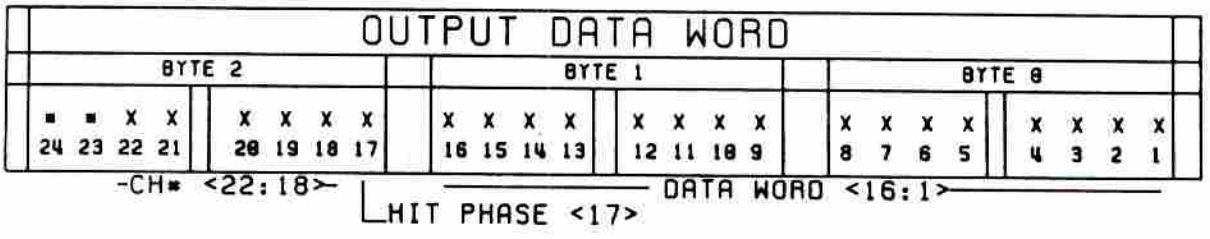


TABLE 2-2 Output Data Word Definition

Installation

3.1 General Installation

The LeCroy Model 2277 TDC is intended for use within a standard CAMAC crate such as the LeCroy Model 8025 CAMAC Crate with 25 slot positions or the Model 8013A with 13 positions. The following voltage sources must be properly connected to the backplane: +6 V , −6 V and +24 V . Each crate must be controlled by either a slave or an intelligent controller. The controller must occupy the rightmost slot of the crate. Its purpose is to issue CAMAC COMMANDS to the modules and transfer information between a computer (or other digital device) and the CAMAC modules. LeCroy offers several such crate controllers, including the Model 8901A. The 8901A is a GPIB/CAMAC slave interface that operates as a "Talker/Listener", allowing the crate to act as one GPIB instrument.

With the power off, the 2277 is inserted into one of the slots of the CAMAC crate. The edge connector on the module should mate with the bus connector with modest pressure. The thumb screw located on the lower edge of the card should be engaged and tightened. Note the slot number of the module, as it will later be used for addressing.

3.2 Cables

The optimal method of cabling is the use of coax cables as signal cables. They generally result in less noise pick-up and less crosstalk. However, the use of twisted-pair cables generally results in lower cabling costs and typically higher density, thus the 2277 was designed to accept 34 connector ribbon cable. If using twisted-pairs, care should be taken to install high quality, shielded cables to minimize the effects of noise and crosstalk. Many of such cables can be purchased from LeCroy Corporation. In particular, there are two types of 34 conductor multiwire cables available, one for short connections using flat cable and the second for long connections using twisted and flat ribbon cable.

The model numbers of such cables are as follows:

- STC-DC/34/L - flat multiwire cable for short interconnections
- LTC-DC/34-L or DC2/34-L - twisted-pair multiwire cable for long interconnections
- STP-DC/02-L - single twisted-pair cable, 3 ft maximum length

NOTE that L is the length in feet that must be specified by the user.

All inputs are differential ECL and terminated by 112 ohms. The terminations are SIP components and may be easily replaced to accommodate other characteristic impedances.

Operating Instructions

4.1 General Operation

The operation of the 2277 can be divided into four unique phases. The first phase includes all the setup necessary before the 2277 TDC can successfully be used. This includes installation of the module and programming the control register. The module will not latch hits until the control register has been programmed. Once all the setup is complete, the module is in acquisition mode and ready to accept hits. The module remains in acquisition mode until either a common stop or a common start timeout occurs depending on the acquisition mode programmed. Following acquisition mode, the module buffers the data in a single event data buffer. It can take up to 5.12 μsec for the first dataword to be buffered. The first dataword has been buffered once the module issues a Look-at-me demanding attention. While the data is being buffered, the Buffering-In-Progress (BIP) signal is true. The user can begin the final phase, readout, either after or while the buffering is in progress. If the user begins the readout phase while the data is being buffered, it is possible for the user to issue a CAMAC read and receive an invalid word. The invalid word is easily identified because its Q will be false. If the user waits until after the buffering has been finished, an invalid data word indicates end of event. Refer to the flowchart provided in figure 4-1 for further assistance.

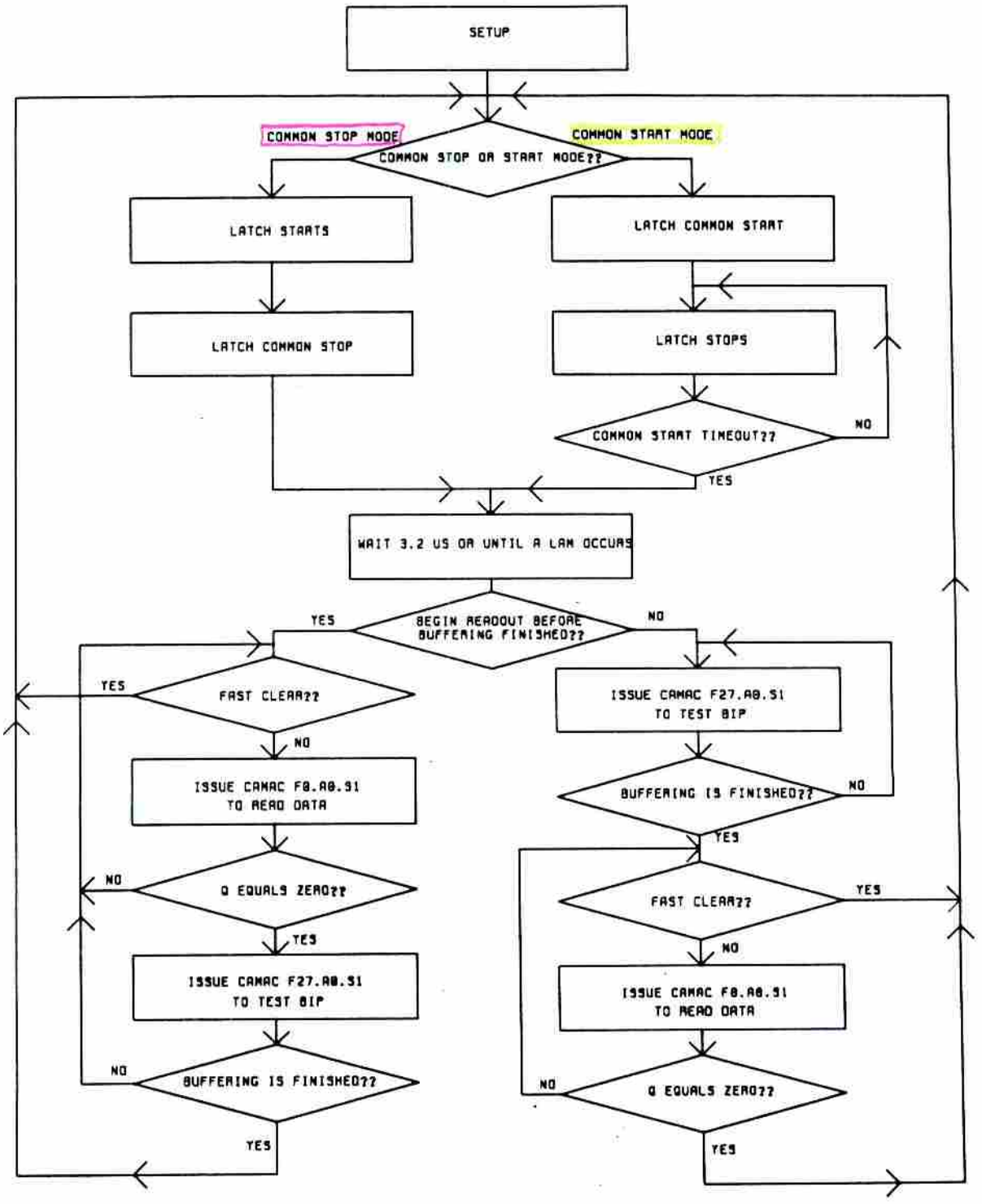


Figure 4–1 2277 General Operation Flowchart

4.2 Common Start vs. Common Stop Modes

The LeCroy Model 2277 TDC was designed to operate in both Common Start and Common Stop modes. Sensitivity for the individual channel input pulses can be programmed in the control register to trigger on either the leading and/or the trailing edge. In either mode, channels can store the time interval of a maximum of 16 edges. The common hit (stop or start), always measures from the leading (low-to-high transition) edge.

When in Common Stop Mode, the individual hit pulses must precede the common stop pulse. The hit pulses are received via the front panel inputs marked IN, and the common pulse is received via either of the front panel inputs marked COM. Time is measured from the leading and/or trailing edges of the hits to the leading edge of the common stop pulse. In Common Stop Mode, the last 16 edges before the common are recorded with earlier hits being discarded. The module 2277 will not accept multiple common input pulses.

Figure 4-2 demonstrates proper timing of the signals in Common Stop mode where 16 start pulses have been provided via the hit input and a stop pulse has been provided via the common input. After a power-on which creates a Power on Reset pulse to the module (POR), the 2277 is in acquisition mode and is ready to accept hits provided the control register has been programmed properly. If both edges of the 2277 were enabled, all 16 edges shown in the figure would be latched. The leading edge of the COM stop pulse disables the 2277 from accepting further HITs. The common pulse must be at least 20 nsec wide and the trailing edge must arrive before readout can occur. The 2277 can be readout via CAMAC as quickly as 5.12 µsec after the leading edge of the common stop pulse provided the trailing edge of the common stop pulse has arrived. If the module's Look-at-me (LAM) has been enabled, readout can begin as soon as a LAM occurs. However, valid data cannot be guaranteed until Buffering in Progress (BIP) becomes false which could take up to 240 µsec. See section 4.6 for more information regarding the BIP signal. The front end is prohibited from accepting inputs while the BUSY signal is true. The BUSY signal is true until either the TDC detects a CLR pulse or all the current event's data has been readout. The module will accept either a CAMAC or a front panel clear at any time. The front panel CLR signal must be at least 20 nsec wide. The module will automatically return to acquisition mode 60 nsec after the trailing edge of the clear pulse.

When operating in Common Start Mode, a full scale time hit window is necessary. The hit window determines the period during which the module will latch hits. The hit window begins when the module detects a start via the COM input and ends when the module receives a timeout pulse. The common start timeout is CAMAC programmable, or it may be provided via the front panel input marked T-IN. If a timeout, either from the front panel or internally generated as programmed, is not provided within 65,536 nsec after the leading edge of the start pulse, the module uses a default timeout and disables itself. The window is opened immediately following the leading edge of a COM input pulse or a start, and it is closed after 65,536 nsec. While the window is open, the module will latch the leading and/or trailing edges of all pulses received either via the front panel connectors marked IN, the front panel connector marked TEST or the internal tester. Hits received after the timeout window has closed are not recorded. In the event more than 16 hits arrive during the hit window, those 16 hits furthest in time from the common start are registered. Multiple common hits are not accepted.

Figure 4-3 demonstrates proper timing of the signals in Common Start mode where a start pulse has been provided via the COM input and 16 stop pulses have been provided via the input labeled IN. As in Common Stop mode, the 2277 enters acquisition mode immediately after a power-on (POR). Provided the Hit Leading Edge and the Hit Trailing Edge bits have been enabled, the 2277 will latch all edges received after the leading edge of the common start input pulse. There must be at least 20 nsec between selected edges in order for the hits to be latched. The common start input pulse must be at least 20 nsec wide and the trailing edge must arrive before readout can occur. Readout can occur as quickly as 5.12 µsec after the trailing edge of the common start timeout has arrived, or if the module's Look-at-me (LAM) has been enabled, readout can begin as soon as a LAM occurs. To read the entire event, continue to issue read data commands until Q becomes false. If the Buffering In Progress (BIP) signal is also false, the event has been completely readout. However if the BIP signal is true, the data is still being buffered. The front end is prohibited from accepting inputs while the BUSY signal is true. The BUSY signal is true until either the TDC detects a CLR pulse or all the current event's data has been readout. All data which is returned with Q equal to zero is not valid.

Note that the scale at the bottom of the figures are in nsec.

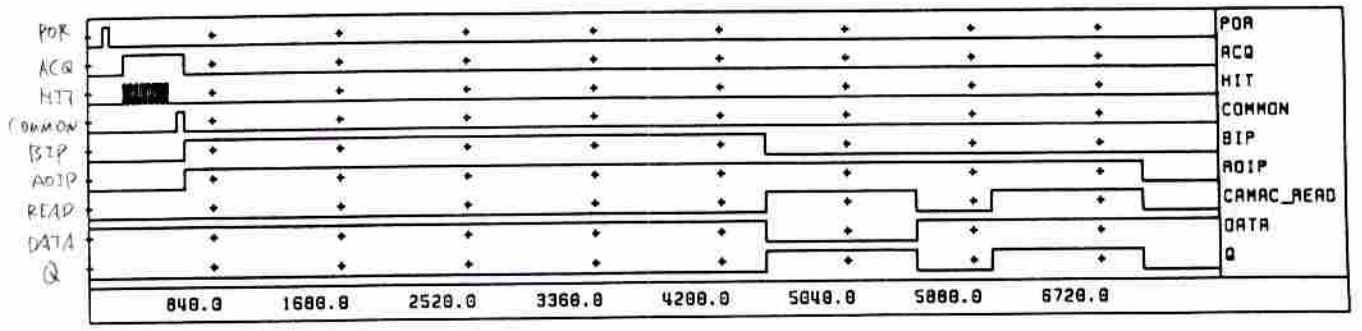


Figure 4-2 An example of proper signal timing for operation in Common Stop Mode.

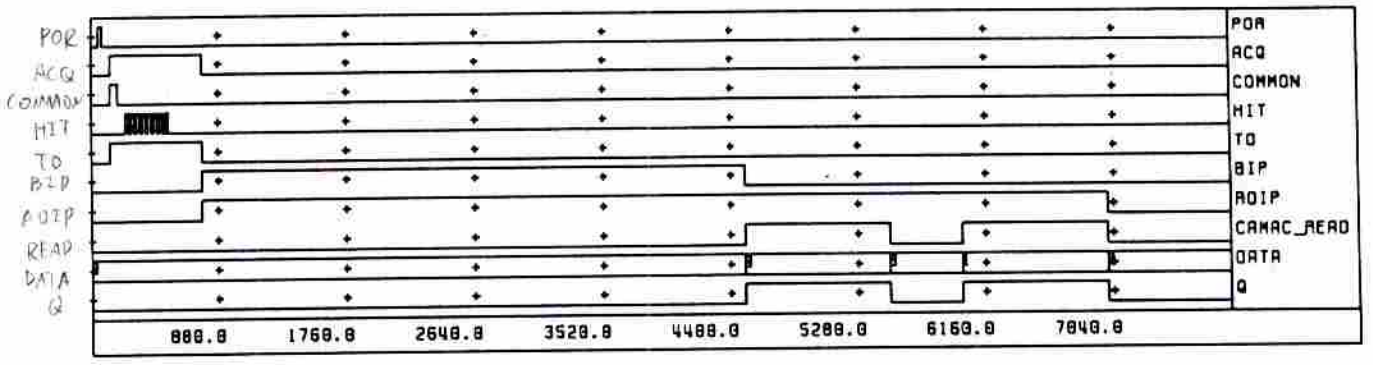


Figure 4-3 An example of proper signal timing for operation in Common Start Mode.

4.3 Pulse vs. Latch Modes

Sixteen dECL front panel trigger outputs marked TRIG PAIR OUT are available to the user for external trigger logic. Neighboring channels are "pairwised OR'ed" (0 & 1, 2 & 3, etc.) to produce a true trigger out when either of the channels receives a hit. The trigger outputs can be programmed to work in either a Pulsed or a Latched Mode by programming bit 8 of the control register. See Section 2.7 for further information on programming the control register. When in Latched Mode, the trigger outputs are cleared by either a front panel clear, a CAMAC clear or when events are read out of the MTD132. When in Pulse Mode the trigger outputs remain logic true for approximately 20 nsecs, and then they are cleared.

the clear signal. The clear signal must have a width of at least 20 nsec. If a clear signal arrives during readout, the remainder of the current event's data will be corrupted.

- **IN:** The two 34 pin connectors on the front panel marked IN are used to receive the pulses whose times are to be measured from the COM input pulse. In Common Stop Mode, the pulses mark the beginning of the time interval which is digitized by the 2277. In Common Start Mode, the pulses mark the end of the time interval which is to be digitized.

- **COM:** The two front panel inputs marked COM are used to accept the common input pulse. In Common Start Mode, the leading edge marks the beginning of the time interval which is digitized by the 2277. In Common Stop Mode, the leading edge marks the end of the time interval which is digitized. Two front panel inputs are available for daisy chaining several modules together. See Section 4.7 for further details on daisy chaining the 2277.

- **T–IN:** When operating in Common Start Mode, it is necessary to supply a full scale window. The window is a defined period during which the module will latch hits. The window begins after a start pulse and ends when the module receives a timeout pulse. This timeout pulse may be provided on board by programming the control register appropriately as explained in Section 2.7. Alternately, an external timeout may be provided via the front panel input marked T–IN. If the trailing edge of the front panel hit window does not occur within 65,535 nsec after the leading edge of the common input pulse (start), the module uses a default timeout and disables the board from accepting further hits. When using the front panel timeout, bits 13–15 of the control register should be set to 0.

- **TEST:** For testing purposes, a front panel input marked TEST is available. In Common Stop Mode, pulses received via the test input marked TEST begin the time interval to be digitized and the common input marked COM provides the stop. In Common Start Mode, the common input provides the common start, and the test input provides the stops. The last 16 enabled edges provided via the test input are stored. For example, if both (the Hit Leading Edge) and (the Hit Trailing Edge) bits of the control register are enabled, the last 16 edges will be stored. However, if only the Hit Leading Edge bit is enabled, the last 16 leading edges will be stored.

4.5 Front Panel Outputs

All Front panel outputs are differential ECL and are asserted when the pin labeled "+" is ECL high and the pin labeled "–" is ECL low. All outputs are described below:

- **BUSY:** BUSY is a single dECL signal provided to aid in readout. BUSY is true to indicate when the 2277 inputs are inhibited. At power–up, BUSY is false and the module is ready to accept inputs. When the module receives either a common start timeout or a common hit, depending on the mode, BUSY becomes true and the module will no longer respond to IN inputs. BUSY remains true until the module is cleared, a master reset is issued or the user has completely read out the module.

- **TRIG PAIR OUT:** Sixteen dECL outputs are provided for external triggering purposes. Input pulses received via the front panel inputs, the front panel TEST input or the internal tester are pairwised OR'ed (0 & 1, 2 & 3, etc.) to create each trigger output. When in latched mode, the output is set by an input pulse and is not reset until the 2277 receives a clear or is readout. When in pulsed mode, the output creates a pulse for each latched input edge. See section 4.3 for a complete description of latched versus pulsed modes.

4.6 Reading the Data

The user may read out the 2277 as quickly as 5.12 μsec after the module receives either (a common start timeout) or (a common stop hit), depending on the mode. When the module receives either (a common start timeout) or (a common stop hit), the BUSY signal becomes true and the module will no longer respond to inputs. The 2277 immediately begins to transfer valid data to the single event buffer. While the 2277 is transferring the data, the Buffering In Progress (BIP) signal is true. The BIP signal can be tested by issuing a CAMAC F27·A0·S1 Test BIP command. If the module is still buffering the

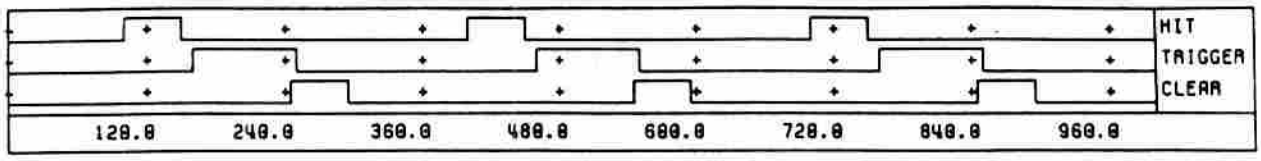


Figure 4–4 Example of timing relationship between hits and the trigger outputs when operating in Latch Mode.

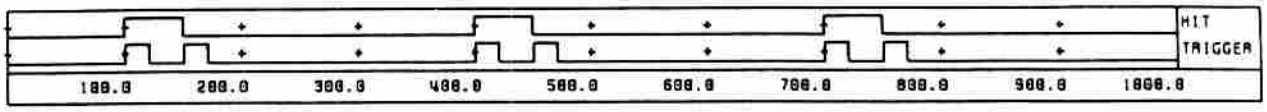


Figure 4–5 Example of timing relationship between hits and the trigger outputs when operating in Pulse Mode.

4.4 Front Panel Control Signal Inputs

All Front panel control signals are differential ECL and are asserted when the pin labeled "+" is ECL high and the pin labeled "–" is ECL low. All inputs are terminated by 112 ohms, as shown. The terminations are SIP components and may be easily replaced to accommodate other characteristic impedances.

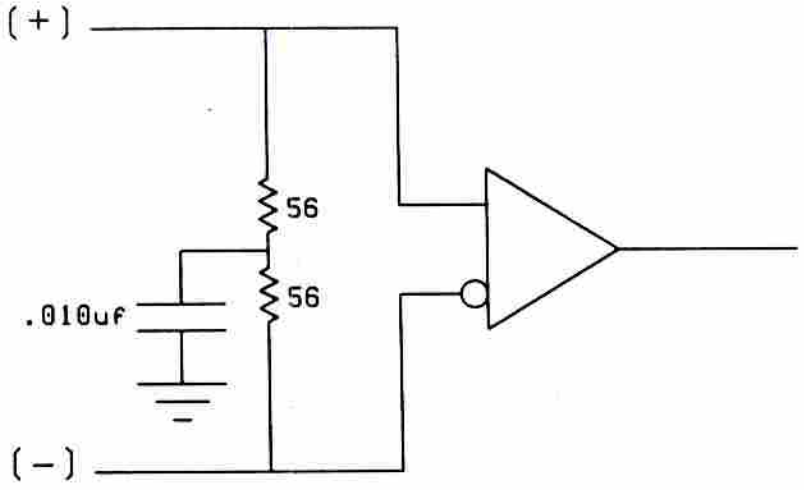


Figure 4–6 ECL Terminations

All front panel inputs are dECL and are briefly described below:

- **CLR:** A clear signal may be sent to the module at any time via the front panel input marked CLR. All channels of the module are immediately cleared without changing the status of the control register. The module enters acquisition mode and is ready to accept hits 60 nsec after

data. Q will return a true response. After BIP becomes false, it is safe to readout the data by issuing a F0·A0·S1 read data command. To read the entire event, continue to issue read data commands until Q is false indicating the end of event. The last data word returned with Q equal to zero is not valid.

However, the data can be read out before the buffering has finished provided the user waits 3.2 µsec after the end of acquisition or a Look-at-Me occurs. If reading before the end of the buffering, it is possible the user will read a Q equal to zero which does not indicate the end of event, but rather that the next data word was not ready. To determine the meaning of the false Q, it is necessary to issue a CAMAC F27·A0·S1 Test BIP command. If BIP is returned true, the module is still buffering data. If BIP is returned false, the false Q is indicative of the end of event.

The module will automatically be returned to acquisition mode if the user reads out all data. However, in the event the user wishes to return to acquisition mode before the entire event has been read, either a CAMAC or a front panel clear can be issued. The clear signal clears the single event buffer and returns the module to acquisition mode 60 nsec after the end of the clear pulse.

4.7 Daisy Chaining the 2277

Two COM connections are implemented on the 2277 TDC for easy board to board distribution of the common input pulse. Daisy chaining may be achieved by simply connecting the COM input of one module to the COM input of another module. The termination network for each board should only be left on the last board in the chain, thus the jumpers J5 and J6 should be removed from every module except for the last one in the chain when daisy chaining. The termination networks for the TIME IN signal and the FP CLEAR signal are also jumpered to ease in daisy chaining modules. See figure 4-7 for assistance in identifying jumpers J5 and J6 of the COM termination network, jumpers J7 and J8 of the TIME IN termination network, and jumpers J9 and J10 of the FP CLEAR termination network.

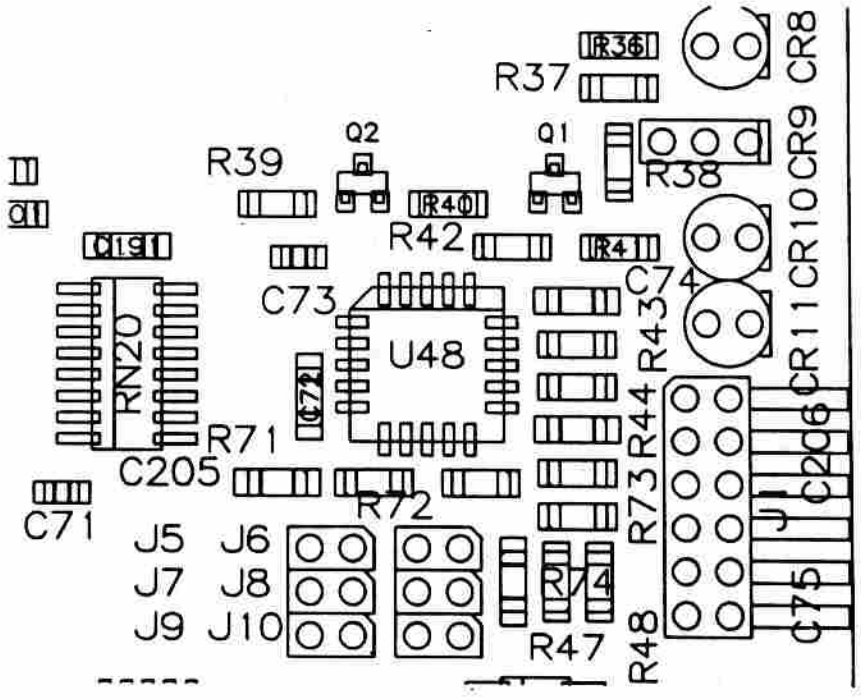


Figure 4-7 Front Panel COM Input Termination Network

4.8 Internal Tester

An internal tester has been implemented on-board the module 2277 TDC for testing and calibration purposes. The internal tester can be programmed to produce 1, 2, 4, or 8 pulses with a pulse width of 128, 256, 1,024, or 2,048 nsecs. Leading and/or trailing edge selection is permissible allowing the internal tester to produce up to sixteen edges. The internal tester can operate in either Common Start or Common Stop Mode.

A test cycle is initiated by issuing the CAMAC command F25·A0·S1. A test cycle should only be performed when the module is in acquisition mode, meaning 60 nsec after the trailing edge of a clear pulse. The default status for the internal tester will produce a single hit pulse with a width of 128 nsec. Provided the Hit Leading Edge and the Hit Trailing Edge bits of the control register are enabled, the single event buffer will store 64 data words with each channel's data similar to that shown below:

Raw Data	Hit Phase	Channel Number	Time Measurement (in bins)
0x10c02	1	0	3074
0x00b84	0	0	2948

It should be noted, the internal tester is not particularly useful for calibrating the 2277. The front panel TEST input would be of much greater use for calibration purposes. However, it is quite useful for testing the single event buffer, the control register and the overall functionality of each channel.

4.9 Testing the 2277 using the Internal Tester

1. Install the module in the crate as indicated in the Installation section.

2. Power up the crate.

3. Issue a Master Reset to the module using a CAMAC C or Z.

4. Write 0F0F (hex) to the control register of the 2277 via CAMAC using a F17·A0·S1. This will place the module in Common Stop Mode, enable both the odd and the even channels for testing, enable both the leading and the trailing edges, and put the trigger in Pulse Mode. The internal tester will be set to produce 8 pulses with a width of 2,048 nsec.

5. Read the control register to be certain all the bits are functioning using a F1·A0·S1.

6. Create a test cycle by writing a F25·A0·S1.

7. Wait 5.12 μs or until a Look-at-Me occurs, then test the Buffering in Progress signal by issuing a CAMAC F27·A0·S1. If Q is true, reissue the command until buffering is complete.

8. Read the data using a F0·A0·S1. Continue to read the data until Q is false. Q equal to zero signifies all data has been readout and the current data word accompanying Q equal to zero is invalid.

9. To test the module in common start mode, write ff00 (hex) to the control register, and repeat steps 5 through 7. Other test patterns can be created as well.

4.10 Testing the 2277 Using the Test Input

1. Install the module in the crate as indicated in the Installation section.

2. Power up the crate.

3. Issue a Master Reset to the module using a CAMAC C or Z.

4. Write 0F00 (hex) to the control register of the 2277 via CAMAC using a F17·A0·S1. This will place the module in Common Stop Mode, enable both the odd and the even channels for testing,

enable both the leading and the trailing edges, and put the trigger in Pulse Mode.

5. Read the control register to be certain all the bits are functioning using a F1·A0·S1.

6. Provide an external common stop pulse by connecting a twisted-pair cable from an external pulser to the front panel input marked COM. Provide external hits by connecting twisted-pair cables from an external pulser to the test input marked TEST. Make certain the start pulses reach the test inputs before the stop pulse reaches the common input.

7. Wait 5.12 μs or until a Look-at-Me occurs, then test the Buffering in Progress signal by issuing a CAMAC F27·A0·S1. If Q is true, reissue the command until buffering is complete.

8. Read the data using a F0·A0·S1. Continue to read the data until Q is false. Q equal to zero signifies all data has been readout and the current data word accompanying Q equal to zero is invalid.

9. Write FF0F (hex) to the control register to test the module in Common Start Mode. Exchange the test input cable with the common input cable. Repeat steps 5 though 7.

4.11 Example Code

Included below is an example of code written in C to use as a reference when operating the 2277. The example code assumes the user has linked to a library containing IEEE standard subroutines for CAMAC. For a further explanation of such subroutines, refer to the *IEEE Standard Subroutines for CAMAC* (ANSI/IEEE Std 758-1979) published by The Institute of Electrical and Electronics Engineers.

The example assumes a crate full of 2277's. Only the LAM of the first 2277 has been enabled. It is assumed that this 2277 will always receive a trigger. Once the lead 2277 has issued a Look-at-me, the remainder of the 2277's will be readout. After the data has been readout, the data is written to file.

```
/*
-------------------------------------------------------------------------
 example.c - An example of typical 2277 operation using IEEE Standard Subroutines for CAMAC.
-------------------------------------------------------------------------
*/

#include <stdio.h>
#include <graph.h>
#include <math.h>
#include <conio.h>

/* prototypes */
extern int cfsa( int function_code, int ext_add, long *camac_data_word, int *q );
extern int cccc( int ext_add );
extern int cdreg( int *ext_add, int branch_number, int crate_number, int station_number, int
        subaddress );
extern int main( void );

/* branch number */
#define BRANCH 0

/* crate number */
#define CRATE 0

/* station numbers */
#define FIRST_SLOT 1
#define LAST_SLOT 23
```

```
/* subaddress - The 2277 has no subaddress except zero! */
#define ADDRESS 0

main()
{
/* CAMAC x and q responses */
int x = 0, q = 0;

/* program parameters */
int ext_address[LAST_SLOT - FIRST_SLOT + 1];
int i, slot2277, ext;
unsigned int event_num = 0;
FILE *stream;
long data_word;
long status = 0x0f00;
long zero = 0x0;

/* Calculate the address for each 2277 module to be addressed. The calculated addresses will be stored
in the array ext_address[]. */
   for( slot2277 = FIRST_SLOT; slot2277 <= LAST_SLOT; slot2277++ )
   {
      cdreg( &ext, BRANCH, CRATE, slot2277, ADDRESS );
      ext_address[slot2277 - FIRST_SLOT] = ext;
   }
/* Reset the 2277's in the crate defined by the variable ext_address[] by causing a Dataway Clear (C). */
   cccc( ext_address[0] );

/* Enable the Look-at-me for the first 2277. Assume the first 2277 will receive a trigger if the other
2277's receive triggers.*/
   cfsa( 26, ext_address[0], &zero, &q );
   if( !q )
   printf( "The LAM for the 2277 in slot %2d has not been enabled.\n", FIRST_SLOT );

/* Disable the Look-at-me for the other 2277's. */
   for( i = 1; i < (FIRST_SLOT - LAST_SLOT + 1); i++ )
   {
      cfsa( 24, ext_address[i], &zero, &q );
      if( !q )
         printf( "The LAM for the 2277 in slot %2d has not been disabled.\n", (i + FIRST_SLOT) );
   }

/* Program the control registers for each module. The control word STATUS is written to each 2277.
*/
   for( i = 0; i < (FIRST_SLOT - LAST_SLOT + 1); i++ )
   {
      cfsa( 17, ext_address[i], &status, &q );
      if( !q )
         printf( "The status register for the 2277 in slot %2d is not properly programmed.\n", (i +
            FIRST_SLOT) );
   }

/* Open a file that the data readout from the 2277's can be stored. */
   stream = fopen( "example.dat", "w" );
   while( !kbhit() )
   {
/* Clear the 2277's to begin acquisition. */
      for( i = 0; i < (FIRST_SLOT - LAST_SLOT + 1); i++ )
      {
         cfsa( 9, ext_address[i], &zero, &q );
         if( !q )
```

```
            printf( "The 2277 in slot %2d has not been properly cleared.\n", (i + FIRST_SLOT) );
        }

    /* Do a test cycle. */
        for( i = 0; i < (FIRST_SLOT - LAST_SLOT + 1); i++ )
        {
          cfsa( 25, ext_address[i], &zero, &q );
          if( !q )
            printf( "Test cycle wasn't done in slot %2d.\n", i + FIRST_SLOT );
        }

    /* Wait for a LAM from the first 2277. Q represents the state of the LAM. */
        cfsa( 8, ext_address[0], &zero, &q );
        while( !q && !kbhit() )
        {
          cfsa( 8, ext_address[0], &zero, &q );
        }

    /* Clear the Look-at-me of the 2277 in the lead slot. */
        cfsa( 10, ext_address[0], &zero, &q );

    /* Read out the 2277's until q equals zero and write the data to file. */
        for( i = 0; i < (FIRST_SLOT - LAST_SLOT + 1); i++ )
        {
          bip = 1;
          fprintf( stream, "event number: %u\t slot number: %2d\n", event_num, (i + FIRST_SLOT) );
          while( bip )
          {
            cfsa( 0, ext_address[i], &data_word, &q );
            while( q )
            {
              fprintf( stream, "%#6x\n", data_word );
              cfsa( 0, ext_address[i], &data_word, &q );
            }
            if( !q )
            {
              cfsa( 27, ext_address[i], &zero, &q );
              bip = q;
            }
          }
        }
        event_num++;
      }

    /* Close the data file */
      fclose( stream );
      return( 0 );
    }
    /*****************************END OF MAIN*************************************************/
```

Theory of Operation

At the heart of the LeCroy Model 2277 TDC is the MTD132. The MTD132 is an eight channel Time to Digital Converter (TDC) implemented as a full custom CMOS ASIC. It combines a synchronous counter and an asynchronous interpolation system with eight parallel memory channels. Each channel is capable of recording the arrival of sixteen pulse edges with sixteen bits of dynamic range. Both Common Start and Common Stop operation are permitted with equal facility. On-chip sparse data readout is implemented, with all possible ambiguities resolved.

5.1 Gray Code Counter Coarse Time Measurement

A sixteen bit gray code counter provides the backbone of the time measurement system. This counter is executed using a bitwise-pipelined and interleaved divide by two technique. Two-way interleaving permits the count frequency to be double that of the counter clock frequency. The counter output is buffered and distributed to the eight channel memories and to the common register.

The counter includes a reset capability. The MTD132 has a reset input which is used to clear the counter and data memories, etc. The counter is zeroed during a clear. In general, the clear input is used only on power on, and to destroy the data from the hit memories and the trigger latches.

5.2 Asynchronous Delay Line Time Interpolation

To increase the resolution of the TDC beyond that expected due to the counter, an asynchronous delay line interpolator is incorporated. This consists of three tapped delays. The input to the first tap is fed by one of the counter clock phases. Each delay tap consists of a controlled current starved inverter followed by a conventional inverter. The current starved inverters allow some measure of control over tap delay.

Following the delay line tap outputs are buffers identical to those used by the counter. The state of the delay line is stored along with that of the coarse counter for each hit.

5.3 Common Input Latch

The buffered counter and delay line outputs are transmitted to both the channel memories and to a "common hit" register. This is used to record a common start or common stop value. The meaning is relevant only to the operation of the output data processor, not to operation during data collection.

5.4 Leading and Trailing Edge Detection

The MTD132 allows the selective recording of leading, trailing or both edges on channel inputs. These modes are selected using two CMOS input pins. These inputs are not latched and must be maintained at the selected values during chip operation. The leading/trailing edge nature of the time measurement is recorded on hit arrival and presented during readout.

5.5 Test Input

A mechanism for stimulating channels for test and calibration purposes is included. During the acquisition period, a pulse on the TEST test input can register all the odd and/or even channels based on the programming of the status register. The edge(s) recorded depends on the state of the edge selection inputs. The channels essentially OR their test and hit inputs. No distinction is made between test and hit inputs during readout.

5.6 Data Processor

During read-out of the MTD132, the data from the common latch and the individual channel memories are converted to binary and subtracted from each other. This produces the time difference between the individual channel input pulses and the common pulse. The direction of the subtraction is determined by the mode of operation - common start or common stop. All data processing is done in a pipelined fashion to expedite data readout.

5.7 Read Only Memory Channel Number Encoding

A means of identifying which channel each data word is read from is necessary, because channels may be skipped entirely, and a variable number of words read out from each channel. A small read only memory is used inside the MTD132 to produce a one of eight to three bit binary encoding of channel number. As a chip is activated for read-out, the ROM word associated with the channel is activated, and the resulting encoded position is transmitted off chip by a set of three tri-state output pads. In addition, it is necessary to identify which chip is active when many chips share a data bus. A Chip Active flag becomes valid when a chip is reading out. The Chip Active flags are encoded externally for chip identification

5.8 Sparse Data Priority Readout System

The MTD132 has a sparse priority read-out system. Only potentially valid words are read out of a given MTD132. Empty words, empty channels and even empty chips are skipped over transparently. This system of priority search is extended to multi-chip systems, such as is the case with the 2277, by the propagation of a priority search flag between chips. Two pins, Priority In and Priority Out receive and transmit the signals.

A chip level look-ahead is used to speed up the search function. The Priority Input does not go directly into the first channel's search string. Rather, the input to the first channel is always set as though no previous channel assumes priority. The search proceeds in each chip in parallel - the first channel with priority in each chip is found. The Priority Out flag is just the OR of the chip Priority In flag and the priority out of the last channel. The Priority In flag is used to inhibit read-out in chips which do not have priority. In this way, a large speed improvement is obtained in systems that daisy chain many chips.

5.9 Wire-ORed Trigger Outputs

Each pair of channels in the MTD132 maintains an SR flip flop that is set when a individual channel detects an edge or a test input arrives . The edge at which this occurs is determined by the state of the leading and trailing edge selection. These four OR'ed values are transmitted off chip by modified CMOS output buffers. A mode control pin determines the function of the trigger outputs, making them latching or transparent. When high, the trigger outputs are transparent, pulsing low briefly each time a selected edge arrives on the appropriate channel hit input. When low, the trigger outputs are latched. The trigger flip-flops are cleared during a chip reset. Once off-chip the trigger outputs are buffered and provided at the front panel outputs.

5.10 Readout Data Processor

Data from channels are combined with the common hit latch externally to identify which chip is being read out. The middle delay line tap data becomes the second least significant bit, and an XOR of the first and third tap data becomes the least significant bit. The fourteen course counter bits become bits 2 to 15 (of 0 to 15).

5.11 Single Event Buffer

The 2277 possesses a single event buffer in the form of a dynamic first in first out memory (FIFO). As soon as the data is exerted on the data bus, it is read out into the FIFO. Only valid data is read into the buffer. While the data is being buffered, the Buffering in Process (BIP) signal is true. When BIP becomes false, the module issues a CAMAC Look-at-Me demanding attention. The data is then ready to be read out via CAMAC. However, readout over CAMAC can occur at anytime. If the dataword is returned with Q equal to one, the dataword is valid. All datawords returned with Q equal to zero are not valid.

APPLICATION NOTE

LeCroy

Innovators in Instrumentation

AN-50

MEASUREMENT PRECISION OF THE NEW LECROY MTD132

The new MTD132 chip represents a revolutionary advance in time measurement capability. As such, it also requires an increase in understanding of the techniques of time measurement.

A conceptual schematic of the MTD132 is shown in Figure 1 on the next page. The MTD132 uses a high speed clock, a continuously counting scaler, and an interpolator. When a signal arrives the contents of the scaler and a four state interpolator are latched and stored in a 16 word first in first out (FIFO) buffer memory. The quantizing step size is 0.75 nanoseconds (nsec). Later signals on the same channel simply store another word in the FIFO. A special input, the COMMON HIT (either START or STOP) input signal is also latched using similar circuits, but without the FIFO memory. External circuitry suspends the latching process promptly when in Common Stop Mode, and after a delay (the measuring period) when in Common Start Mode. During readout each of the stored signal times is automatically subtracted from the COMMON HIT time. The final output is the time difference between the input signal and the COMMON HIT signal. Hits older than the 49 microsecond full scale are automatically discarded. If more than 16 hits occurred within the full scale time interval, only the most recent 16 are saved. In COMMON START mode, a time out interval must be specified to define the full scale time (when the latching process is suspended). All hits until the end of the time out interval are stored in the FIFO. Again, if there are more than 16 hits, only the most recent 16 are saved.

A short list of the MTD132 specifications includes:

- Wide Dynamic Range, 49 μsec Full Scale (16 bits)
- Least Count: 0.75 nsec
- Differential Non-Linearity Better than 20%
- Pipelined Multi-Hit Operation, Up to 16 hits Per Channel
- Multi-Hit Resolution Less than 20 nsec
- COMMON STOP or COMMON START Selectable
- Leading or Trailing Edge (or both) Recorded
- Output Data Corrected for COMMON HIT
- Fast Readout, No Conversion Time or Searching for Hits
- Digital CMOS, Low Power
- High Density, 8 Channels Per Monolithic

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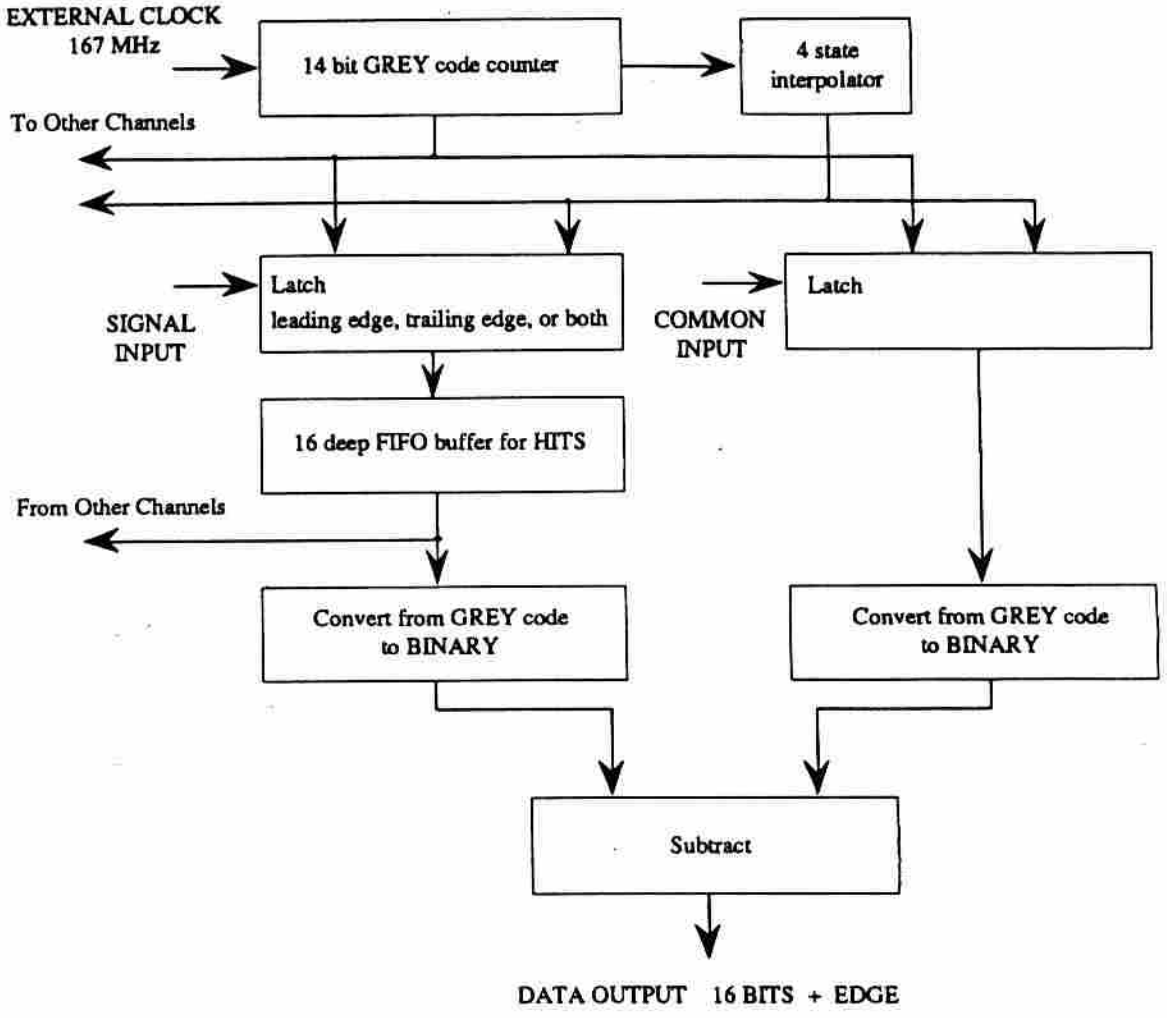


Figure 1
MTD132 Conceptual Schematic

MEASURING TIME INTERVALS

Since the MTD132 clock is always running, the start or stop pulse can arrive at random times with respect to the clock, i.e., the quantizing phase is random. For a single measurement, the error can be as large as ±½ of the LSB, depending on the phase of the arrival of the pulse, with respect to the clock. As an example, think of this as measuring the time of day with a digital clock that shows only the hours (the minutes display is broken!). The quantizing error depends on exactly when you ask what time it is! The error can be as large as ±½ hour. The MTD132 has exactly the same error, but on a vastly smaller scale. The error distribution is square as shown in Figure 2. The rms error is 1 LSB/√12.

Any useful measurement is the combination of two single measurements, one of the start pulse, and one of the stop pulse. The error on the difference of these two measurements can be as large as ±1 LSB. Using the digital clock analogy, the time difference between 10:59 and 11:00 is one hour, if you can't see the minutes display. The difference between 11:00 and 11:59 is zero, and the difference between 10:59 and 12:00 is two hours! The error distribution is triangular, 2 LSB wide at the base, shown in Figure 3. The rms error is now 1 LSB/√6, just the result of combining the two single errors in quadrature. Using 0.75 nsec for the LSB, the rms error is 0.3 nsec (for the digital clock, the rms error is 24 minutes).

Measuring the actual rms error of the MTD132 is not as simple as creating a stable delay and measuring repeatedly to get the error distribution. We obviously must average many measurements to see the effect of the random clock phase, but that is not enough. So far we have assumed that the start and stop times are uncorrelated, which is the case for many of the things the MTD132 will be used to measure. But if we are

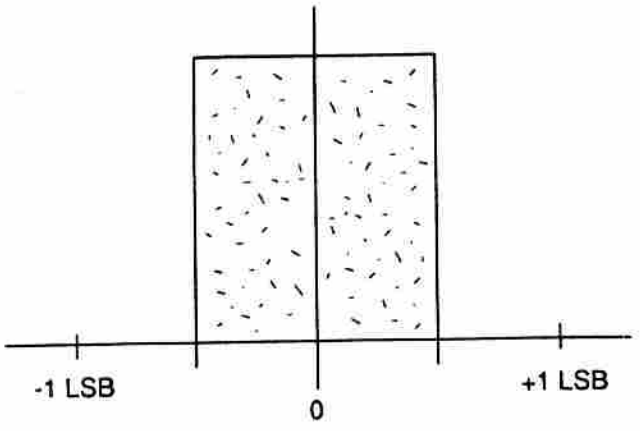


Figure 2

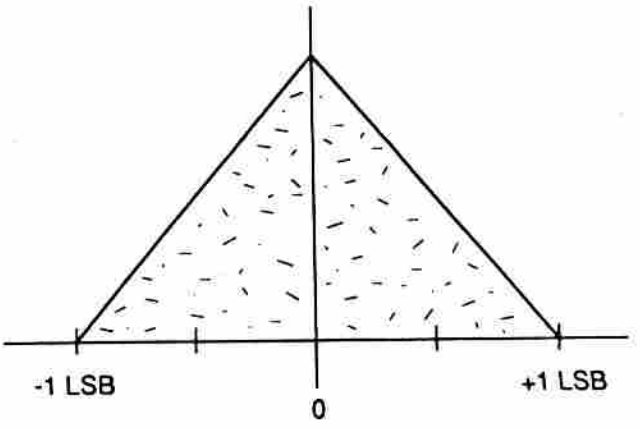


Figure 3

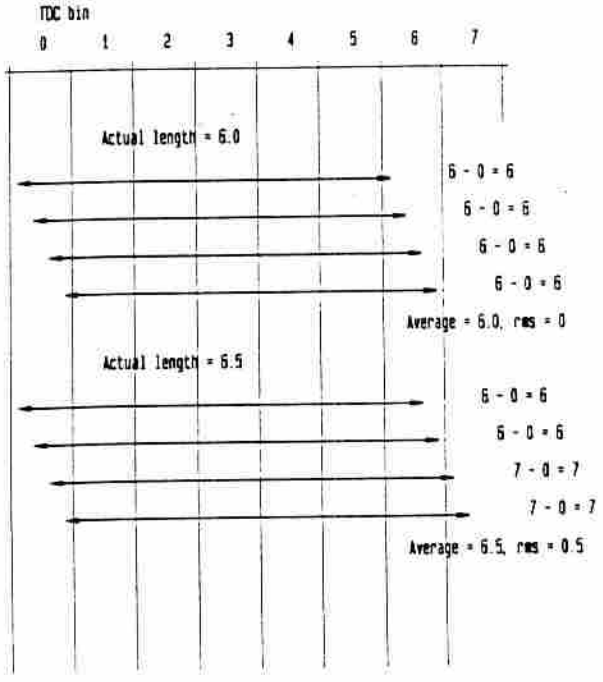


Figure 4

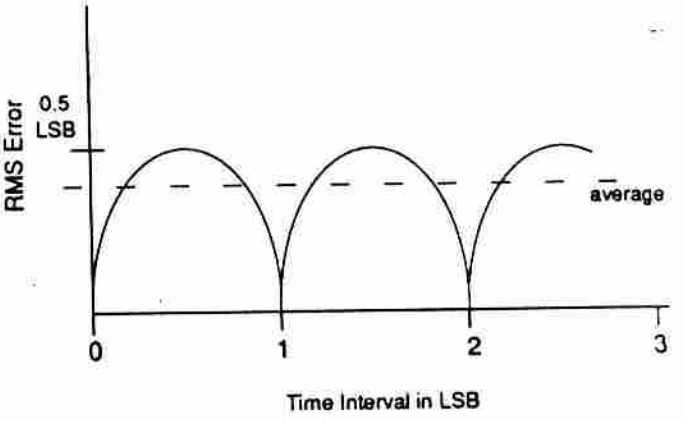


Figure 5

measuring an unknown, but fixed, time interval, the start and stop phases are no longer independent. This, of course, is the usual case for a test setup, measuring a fixed delay time.

The measured rms error depends on the length of the time measured. For example, if the measured interval is exactly an integral number of LSBs, the error will be very small, reflecting only the noise in the system (which includes the differential non-linearity of the MTD132). For the case of a half-integral number of LSBs, the rms error is at its maximum, and dominated by the quantizing error (0.5 LSBs). This is illustrated in Figure 4. A plot of the rms error as a function of time interval measured is shown in Figure 5. The horizontal scale is in units of the LSB of the TDC. To get the correct error distribution we must average over all possible time intervals, at least over a range of 1 LSB. Note that Figure 5 is for a perfect TDC, with no noise, and with perfect quantizing and linearity. The average rms error is 0.4 LSBs. This is exactly the same as the rms error of Figure 3, of course.

Because of the interpolation method used in the MTD132 to achieve the very high resolution, some differential non- linearity is expected which should repeat at least every 8 LSBs. Therefore, the time intervals used to measure the resolution of the MTD132 should uniformly cover a range of 8 LSBs (the period of the external clock), which is 6 nsec.

The results of such a measurement are shown in Figure 6, for a prototype 2277 CAMAC module. The horizontal scales are all in LSBs. The input signal was produced by an RF frequency synthesizer running at about 1 MHz, a LeCroy Model 621 discriminator and a Model 4616 NIM-to-ECL converter. The 2277 was operated in COMMON STOP mode, an F25 command produced the stop. The first 2 leading edge hits read out were used to measure the period of the RF generator. The frequency was then changed in small steps, corresponding to a change in the period of 10 picoseconds. The period was varied from 1.006 microseconds to 0.993 microseconds, which corresponds to 16 LSBs. Several hundred measurements were taken at each RF frequency to correctly average over all possible clock phases (random delays between measurements ensured random clock phase). The top plot shows the average error as a function of the time interval measured. The middle plot shows the observed RMS error, also as a function of time interval (the horizontal line is the average). Note the repetition with an 8 LSB period. This should be compared with Figure 5. The horizontal line is the average RMS error. The last plot shows the observed error distribution, averaged over clock phase and measuring interval. The triangle is the theoretical distribution from Figure 3, and is scaled to have the same integral as the data. For this particular MTD132 channel, the actual RMS error is 0.70 LSBs (0.53 nsec), about 70% greater than the theoretical value of 0.41 LSBs (0.3 nsec).

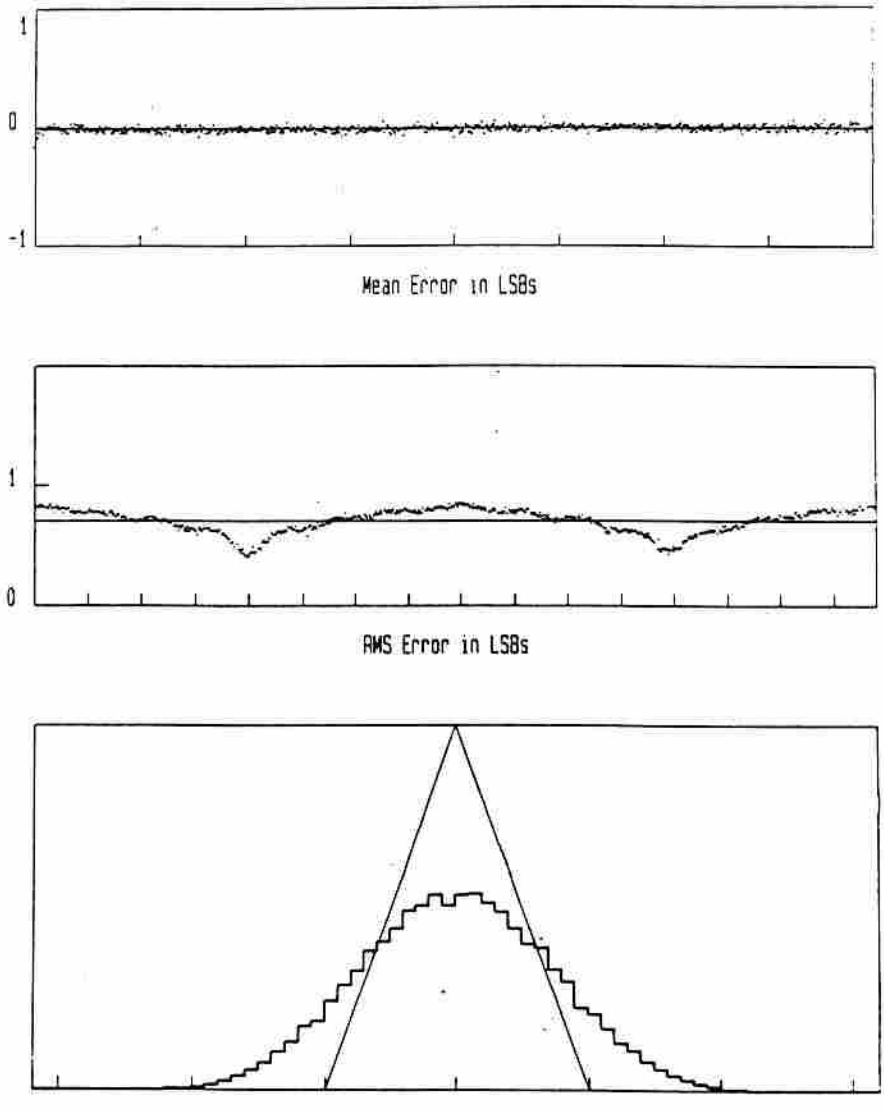
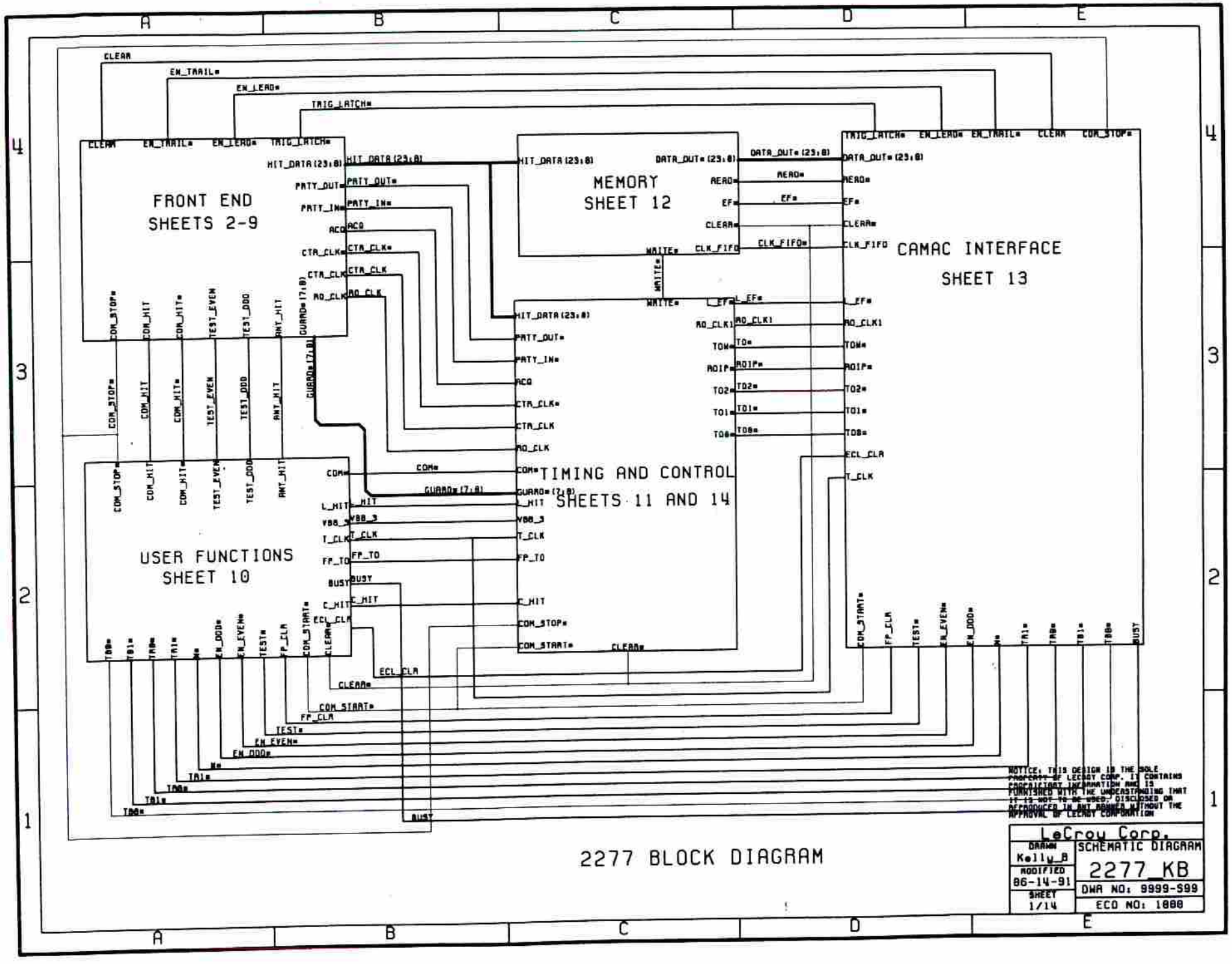
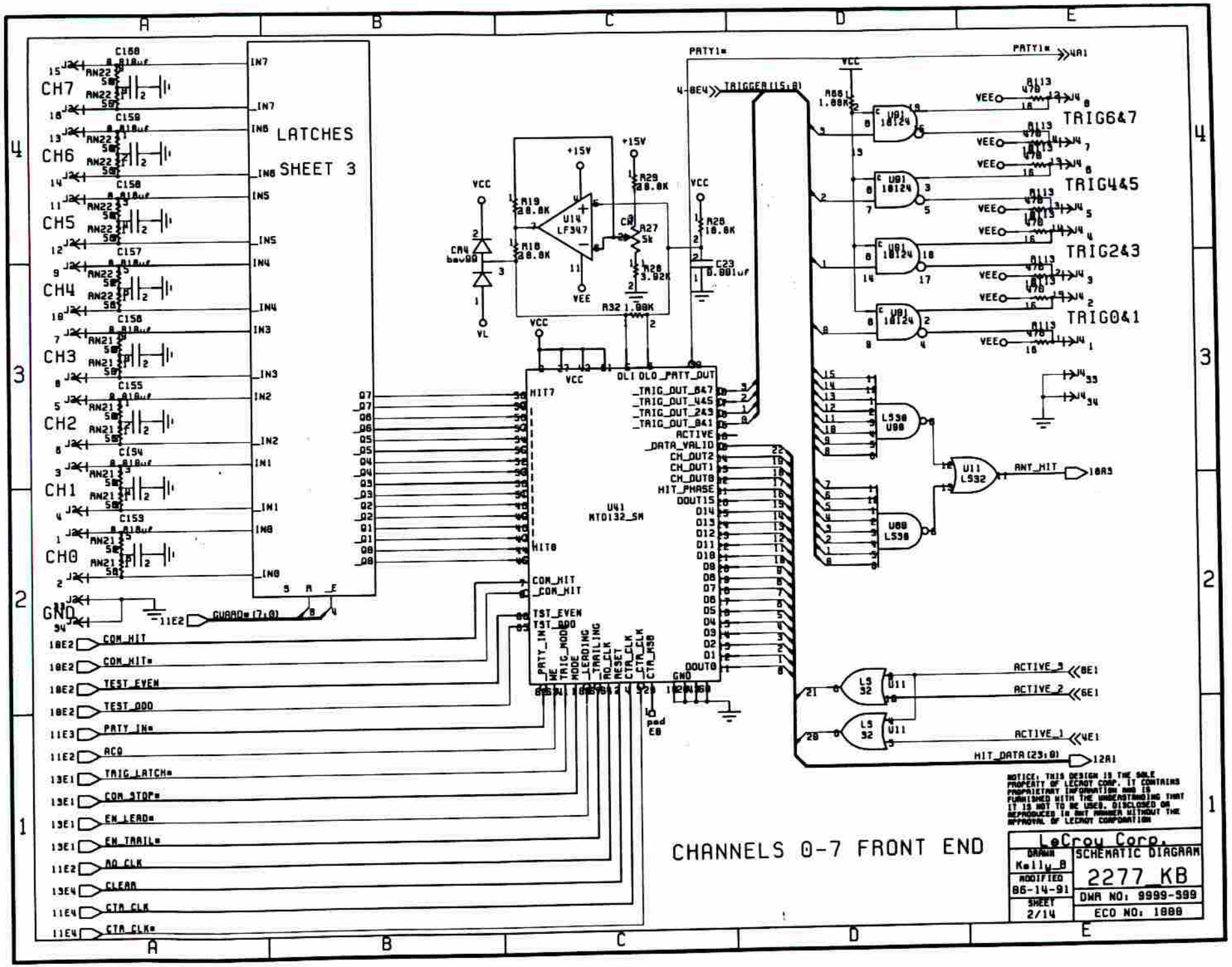


Figure 6



2277 BLOCK DIAGRAM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CH4
CH3
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CH1
CH0
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TRIG4&5
TRIG2&3
TRIG0&1
U41
MTD132_SM
LF347
L532
L530
L538
LS 32
CHANNELS 0-7 FRONT END
LeCroy Corp.
SCHEMATIC DIAGRAM
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ECO NO: 1888
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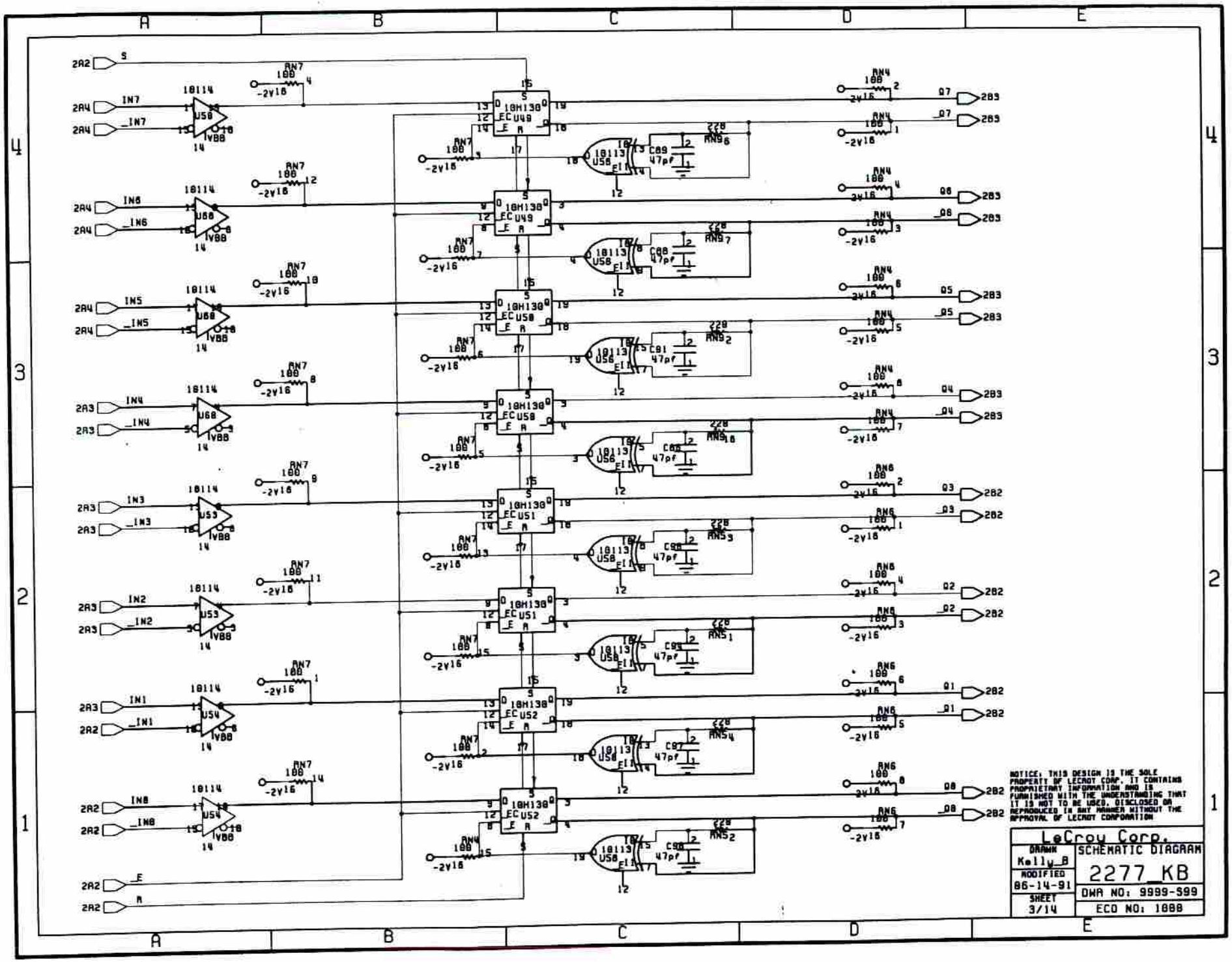
2/14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D
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IN4
_IN4
IN3
_IN3
IN2
_IN2
IN1
_IN1
IN8
_IN8
E
A
10114
U68
U53
U54
VBB
AN7
100
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10H130
EC U49
EC U58
EC U51
EC U52
10113
U58
C89
C88
C81
C86
C98
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282
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3/14
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DWA NO: 9999-599
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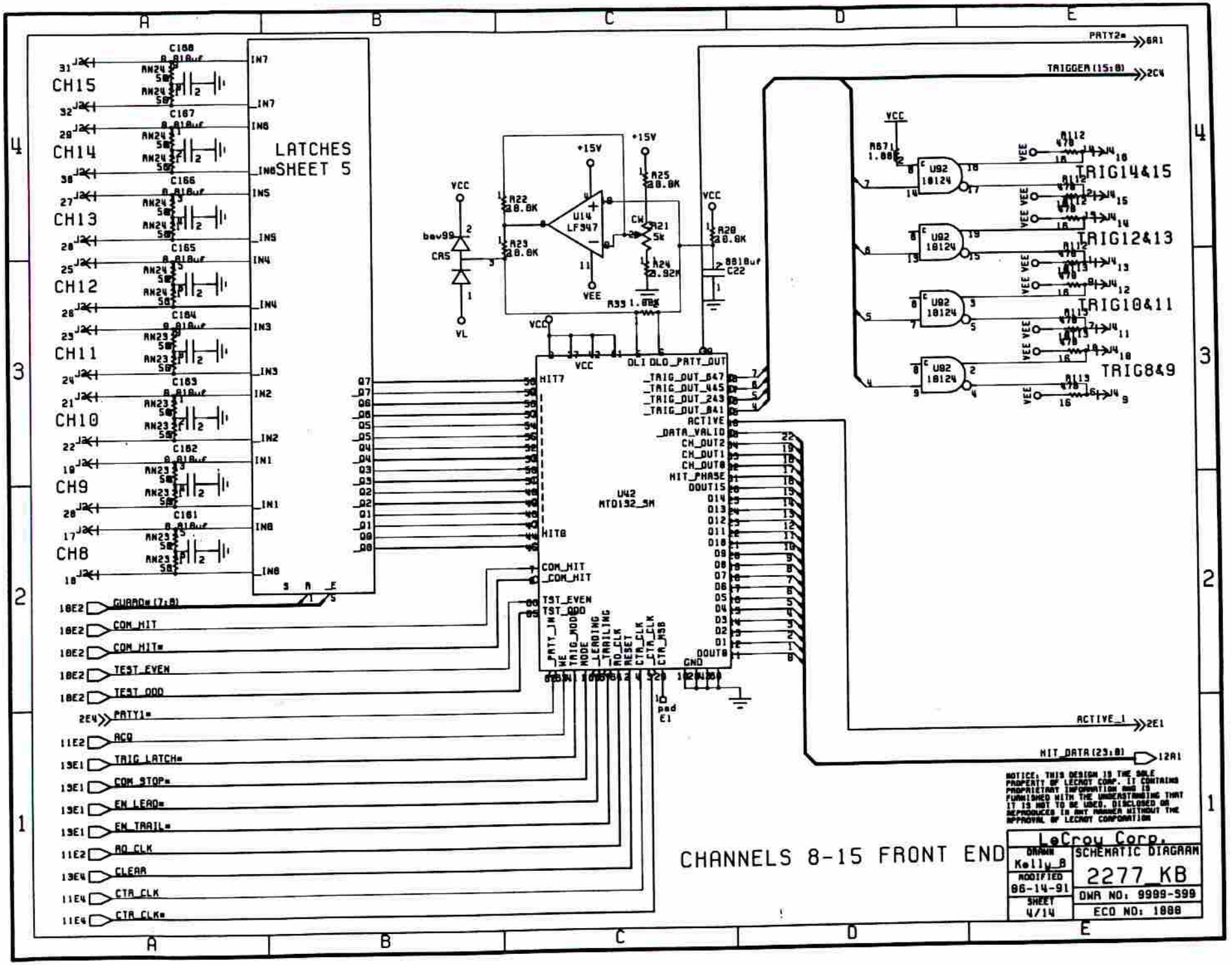
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C164
C163
C162
C161
AN24
AN23
IN7
IN6
IN5
IN4
IN3
IN2
IN1
IN0
S A F
GUARD= (7:0)
COM_HIT
COM_HIT=
TEST_EVEN
TEST_ODD
PATY1=
ACQ
TRIG_LATCH=
COM_STOP=
EN_LEAD=
EN_TRAIL=
AQ_CLK
CLEAR
CTR_CLK
CTR_CLK=
+15V
VCC
VEE
VL
bav99
CR5
R22 20.0K
R23 20.0K
R25 20.0K
R21 5k
R24 2.82K
R33 1.00K
R20 20.0K
U14 LF347
C22 .0018uf
U42 MTD132_SM
HIT7
HIT8
DLI DLO_PATY_OUT
_TRIG_OUT_847
_TRIG_OUT_445
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_TRIG_OUT_841
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CH_OUT1
CH_OUT0
HIT_PHASE
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DOUT0
GND
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WE
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TRAILING
AQ_CLK
RESET
CTR_CLK
CTR_CLK
CTR_MSB
pad E1
PATY2=
TRIGGER (15:0)
R671 1.00K
U92 18124
R112 470
R113 470
R114 470
R115 470
TRIG14&15
TRIG12&13
TRIG10&11
TRIG8&9
ACTIVE_1
HIT_DATA (23:0)
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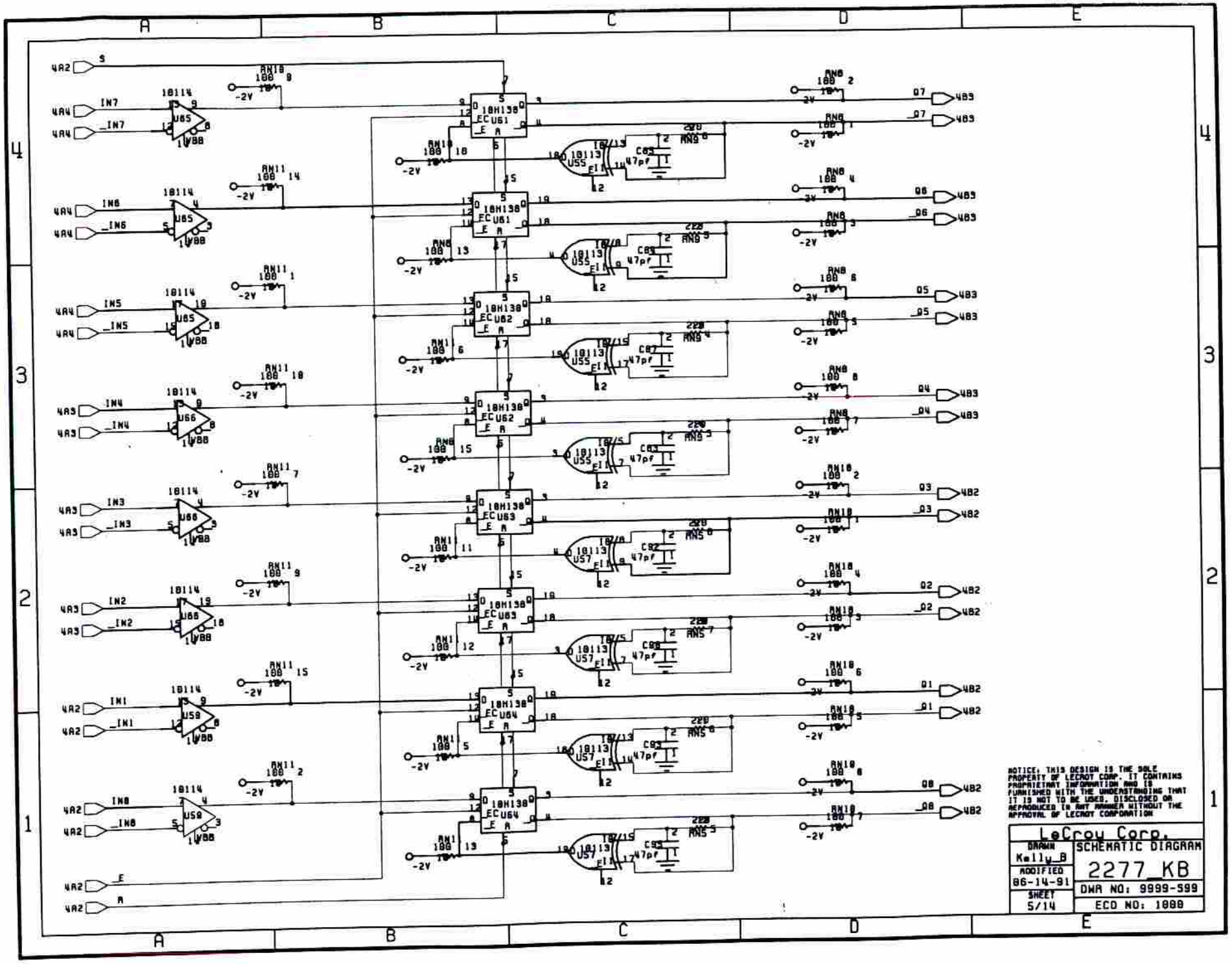
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U87
U88
U89
U90
U91
U92
10114
10113
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ECU61
ECU62
ECU63
ECU64
RN1
RN5
RN6
RN8
RN9
RN10
RN11
100
-2V
220
47pf
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C84
C85
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C88
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5/14
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2277_KB
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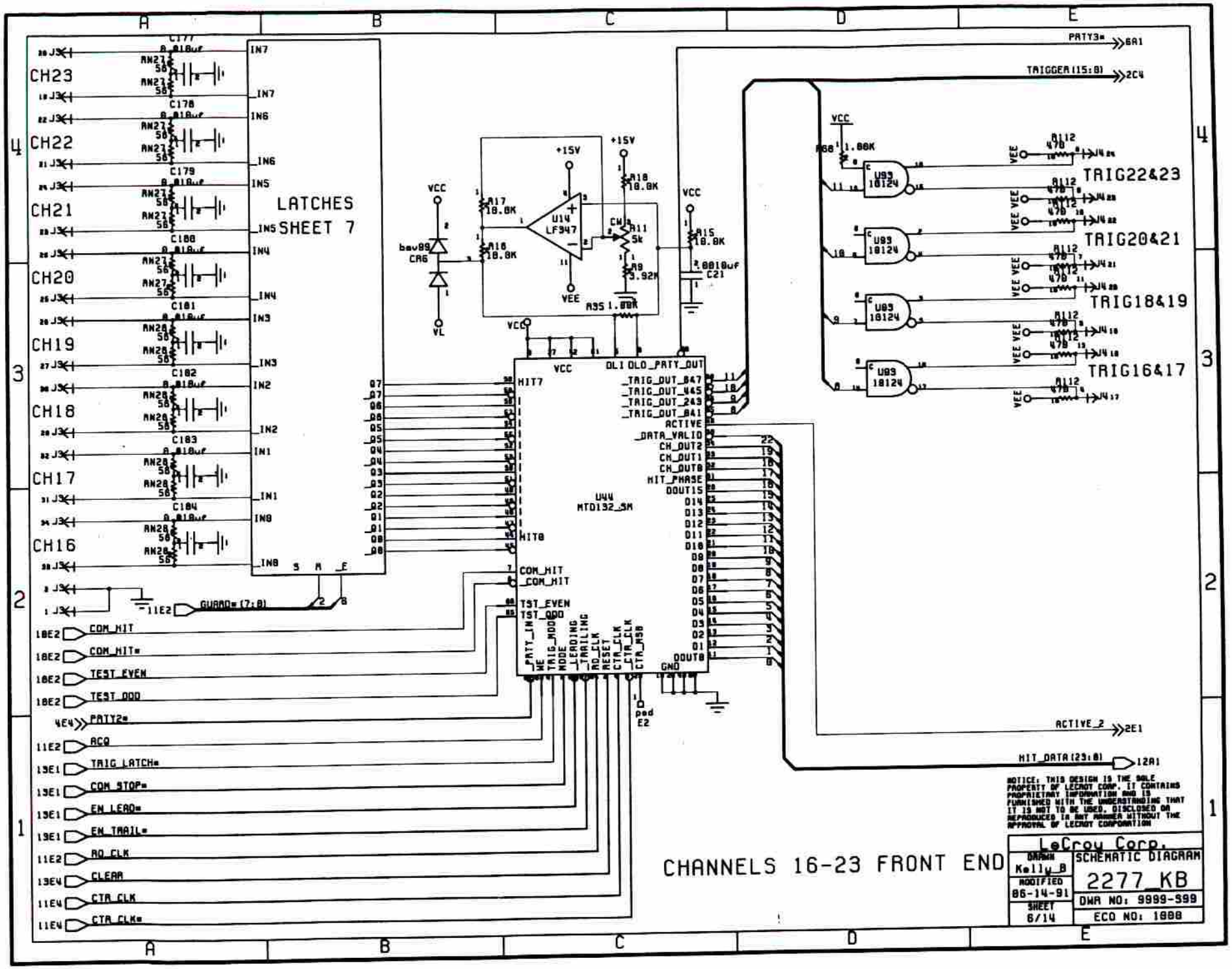
ECO NO: 1000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CH21
CH20
CH18
CH17
CH16
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IN7
IN6
IN5
IN4
IN3
IN2
IN1
IN0
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COM_HIT=
TEST_EVEN
TEST_ODD
PATY2=
ACQ
TRIG_LATCH=
COM_STOP=
EN_LEAD=
EN_TRAIL=
RD_CLK
CLEAR
CTR_CLK
CTR_CLK=
PATY3=
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ACTIVE_2
HIT_DATA(23:8)
+15V
VCC
VEE
VL
U14 LF347
U44 MTD132_SM
U93 10124
TRIG22&23
TRIG20&21
TRIG18&19
TRIG16&17
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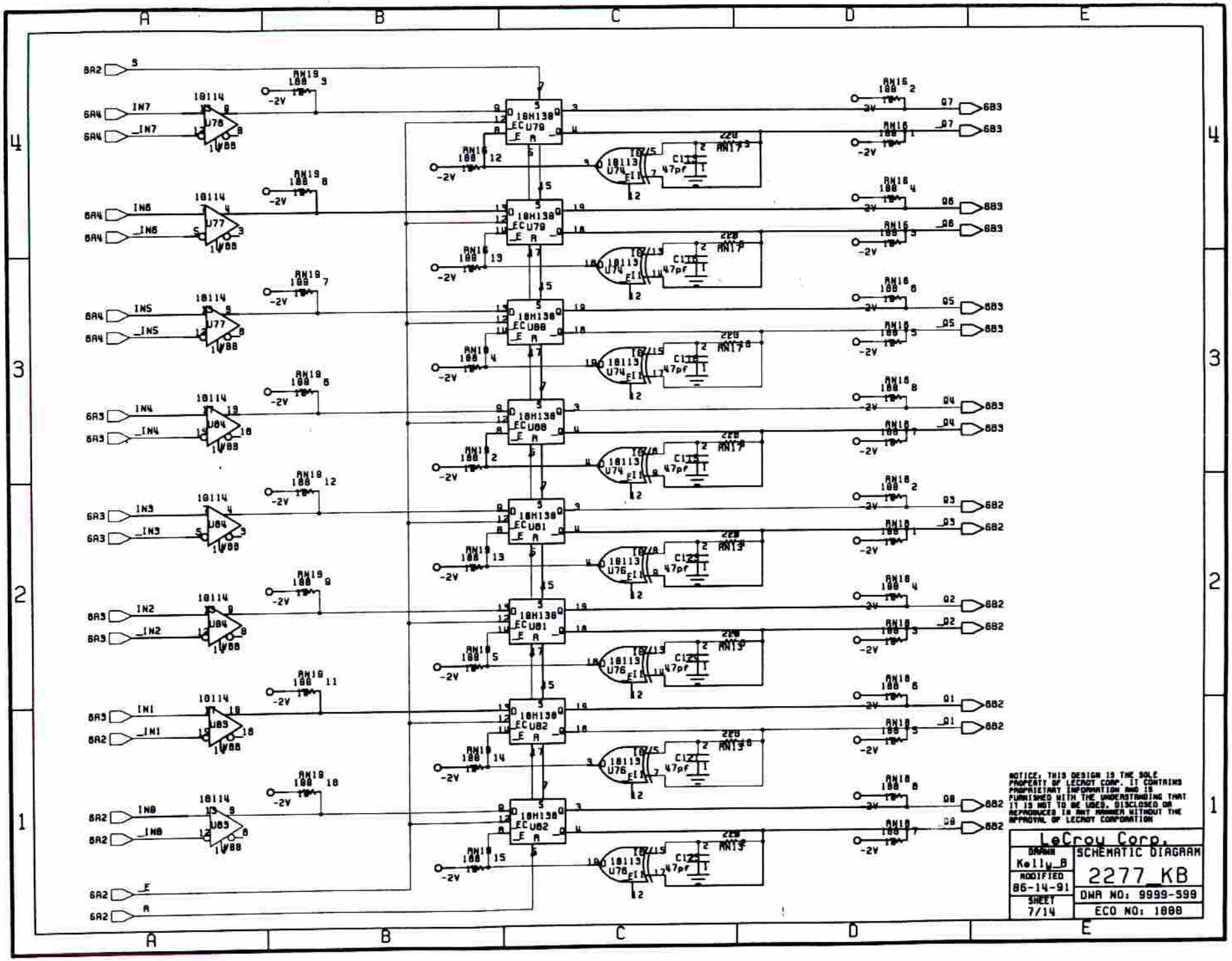
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_IN3
IN2
_IN2
IN1
_IN1
IN0
_IN0
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U84
U85
U88
U79
U80
U81
U82
U74
U76
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18113
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3V
Q7
_Q7
Q6
_Q6
Q5
_Q5
Q4
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Q3
_Q3
Q2
_Q2
Q1
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Q0
_Q0
683
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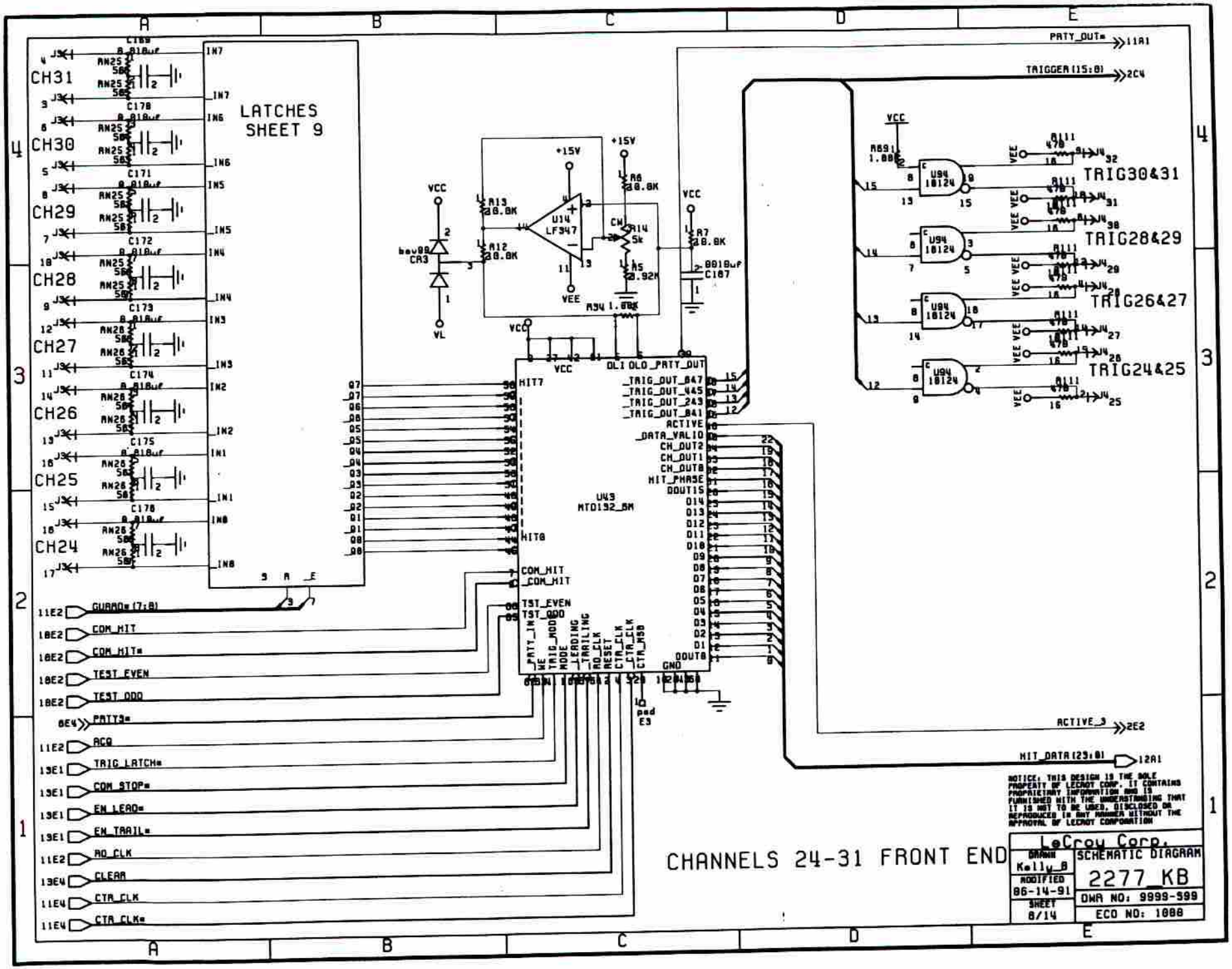
DWG NO: 9999-599
ECO NO: 1000


LATCHES SHEET 9
CH31
CH30
CH29
CH28
CH27
CH26
CH25
CH24
TRIG30&31
TRIG28&29
TRIG26&27
TRIG24&25
U43 MTD192_8M
U14 LF347
PRTY_OUT»
TRIGGER(15:8)
ACTIVE_3
HIT_DATA(23:8)
GUARD»(7:8)
COM_HIT
COM_HIT»
TEST_EVEN
TEST_ODD
PRTY3»
ACQ
TRIG_LATCH»
COM_STOP»
EN_LEAD»
EN_TRAIL»
RD_CLK
CLEAR
CTR_CLK
CTR_CLK»
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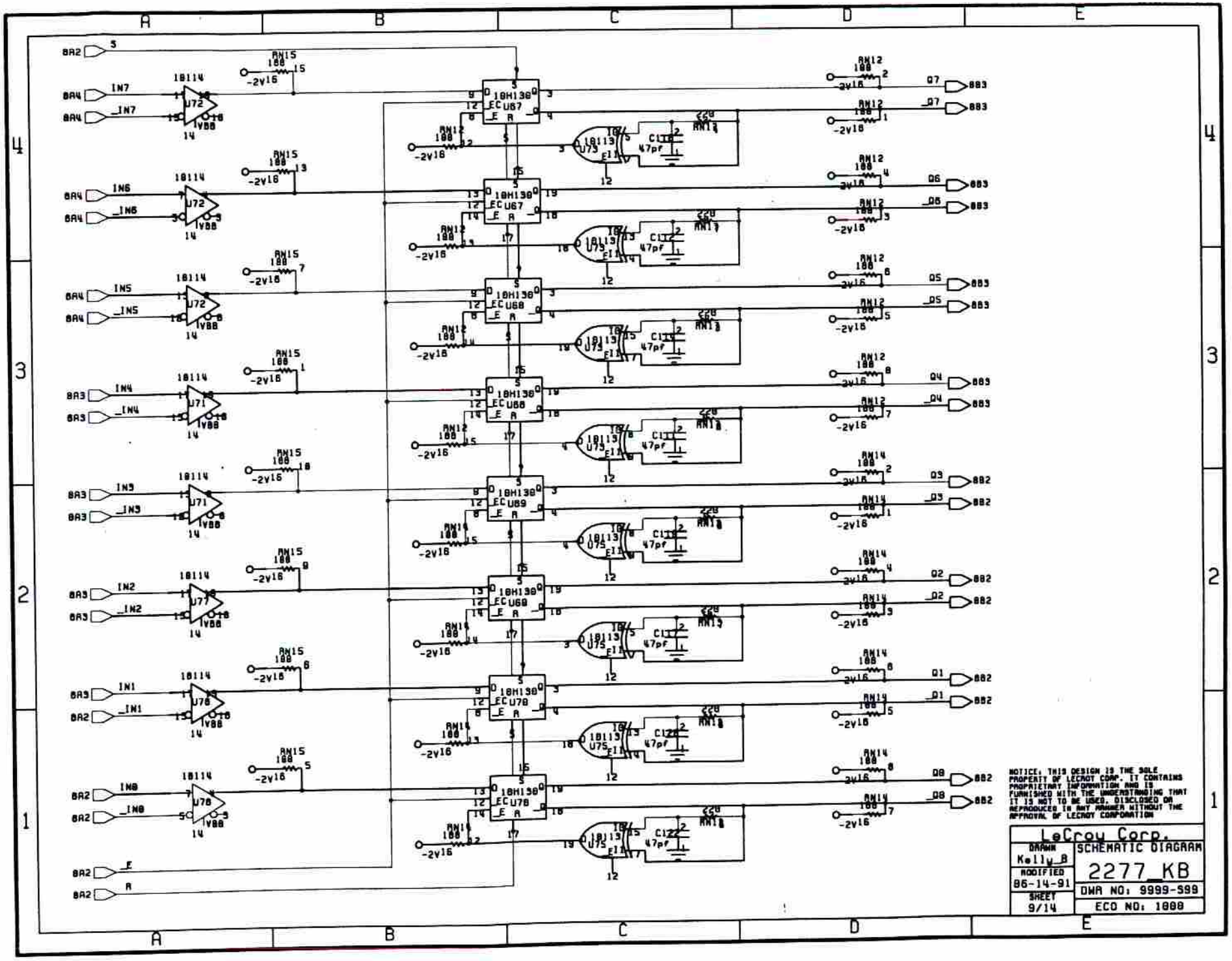
CHANNELS 24-31 FRONT END
LeCroy Corp.
DRAWN Kelly B
MODIFIED 06-14-91
SHEET 8/14
SCHEMATIC DIAGRAM 2277_KB
DWG NO: 9999-999
ECO NO: 1088


A
B
C
D
E
1
2
3
4
8A2
8A4
8A3
IN7
_IN7
IN6
_IN6
IN5
_IN5
IN4
_IN4
IN3
_IN3
IN2
_IN2
IN1
_IN1
IN0
_IN0
E
R
18114
U72
U71
U77
U76
VBB
14
AN15
100
-2V16
10H130
ECU67
ECU68
ECU69
ECU70
F
A
AN12
AN13
AN14
18113
U75
C112
C122
47pf
220
Q7
_Q7
Q6
_Q6
Q5
_Q5
Q4
_Q4
Q3
_Q3
Q2
_Q2
Q1
_Q1
Q0
_Q0
883
882
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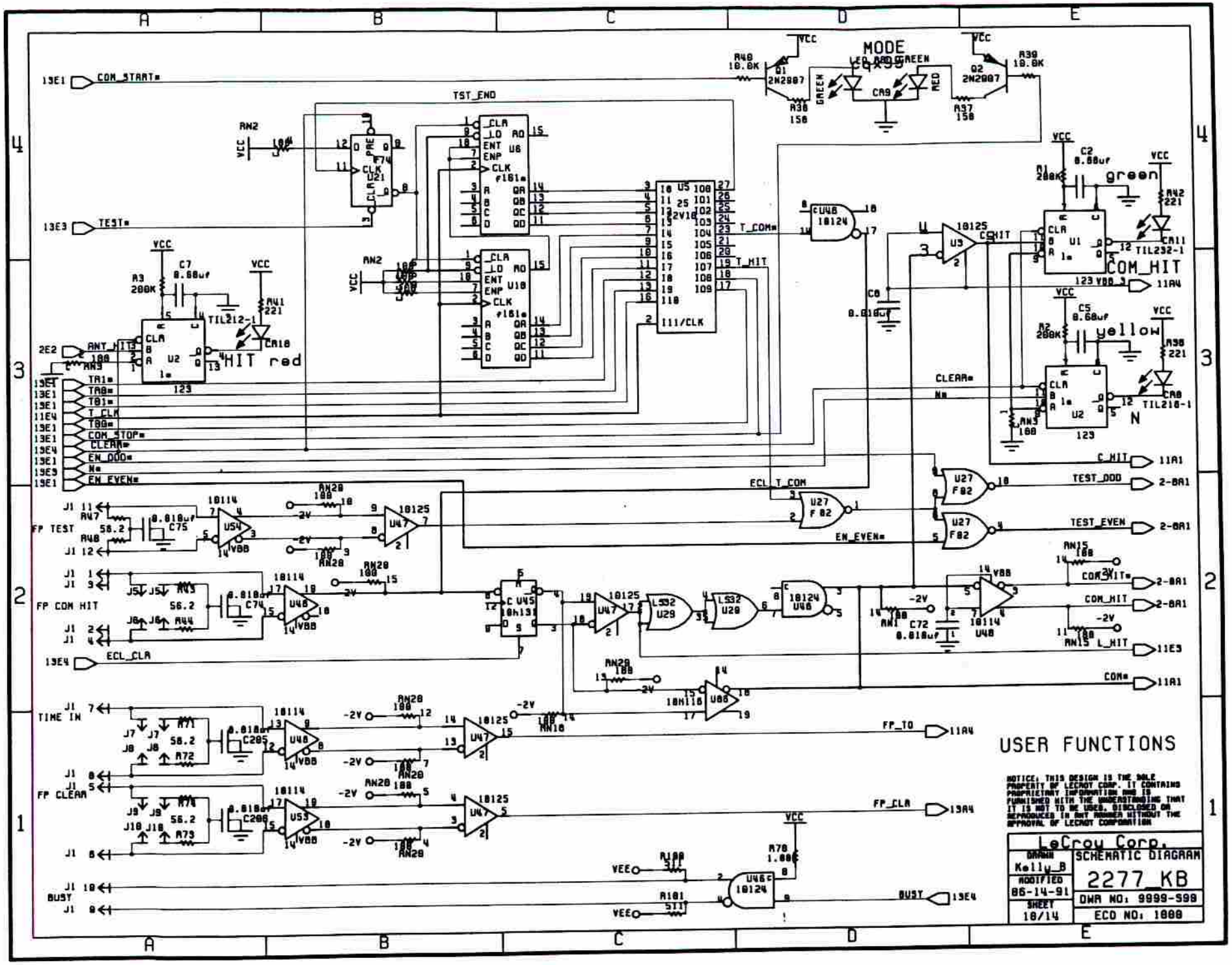
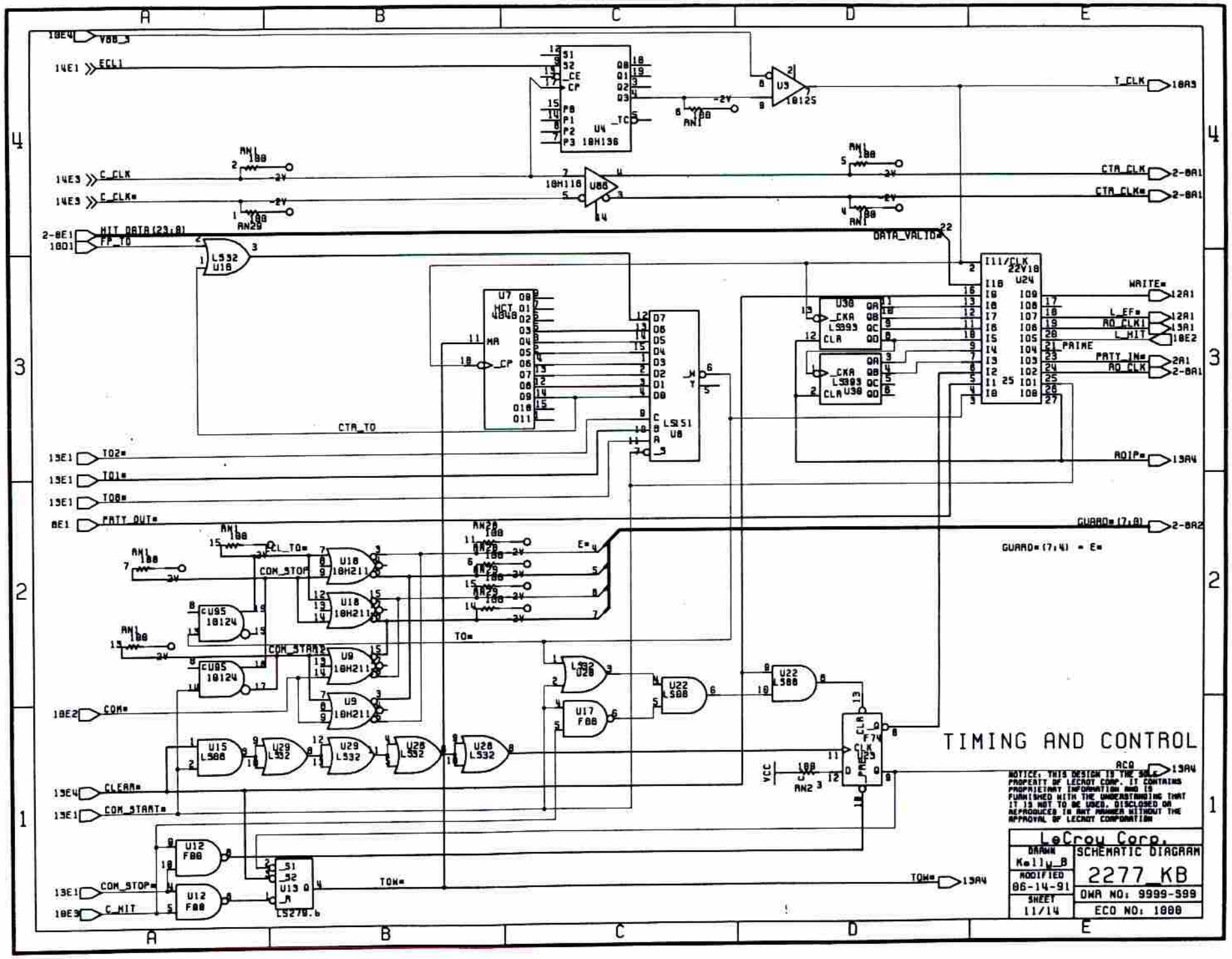
LeCroy Corp.
DRAWN
Kelly B
MODIFIED
86-14-91
SHEET
9/14
SCHEMATIC DIAGRAM
2277_KB
DWG NO: 9999-599
ECO NO: 1008


MODE
COMM
LED RED/GREEN
COM_START*
TEST*
TST_END
T_COM*
T_HIT
COM_HIT
green
yellow
HIT red
TIL232-1
TIL212-1
TIL218-1
CLEAR*
N*
EN_EVEN*
EN_ODD*
COM_STOP*
T_CLK
TA0*
TA1*
TB0*
TB1*
ANT_J
FP TEST
FP COM HIT
FP CLEAR
TIME IN
BUSY
ECL_CLR
ECL T_COM
C_HIT
L_HIT
COM*
TEST_ODD
TEST_EVEN
FP_TO
FP_CLR
BUSY
USER FUNCTIONS
LeCroy Corp.
SCHEMATIC DIAGRAM
2277_KB
DWN NO: 9999-598
ECO NO: 1000
DRAWN Kelly_B
MODIFIED 86-14-91
SHEET 10/14


TIMING AND CONTROL
T_CLK
CTR_CLK
CTR_CLK=
WRITE=
L_EF=
RQ_CLK1
L_HIT
PRIME
PRTY_IN=
RQ_CLK
RQIP=
GUARD=(7:0)
GUARD=(7:4) = E=
ACQ
TOW=
DATA_VALID=
HIT_DATA(23:0)
FP_TO
CTR_TO
TO2=
TO1=
TO0=
PRTY_OUT=
TO=
COM=
CLEAR=
COM_START=
COM_STOP=
C_HIT
C_CLK
C_CLK=
VCC
LeCroy Corp.
SCHEMATIC DIAGRAM
2277_KB
DRAWN Kelly B
MODIFIED 06-14-91
SHEET 11/14
DWG NO: 9999-599
ECO NO: 1000
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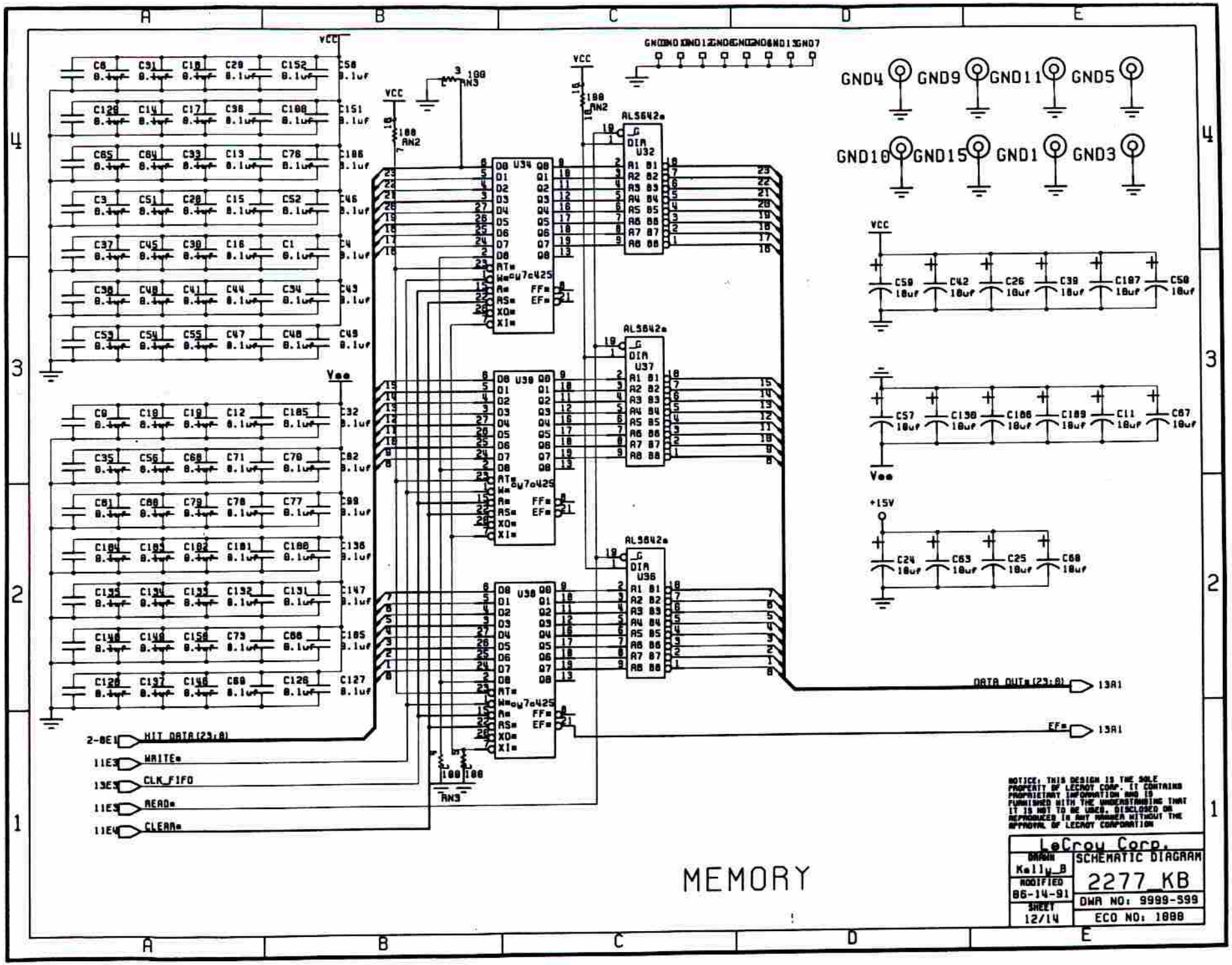
MEMORY
LeCroy Corp.
SCHEMATIC DIAGRAM
2277_KB
DWN NO: 9999-599
ECO NO: 1088
DRAWN Kelly B
MODIFIED 86-14-91
SHEET 12/14
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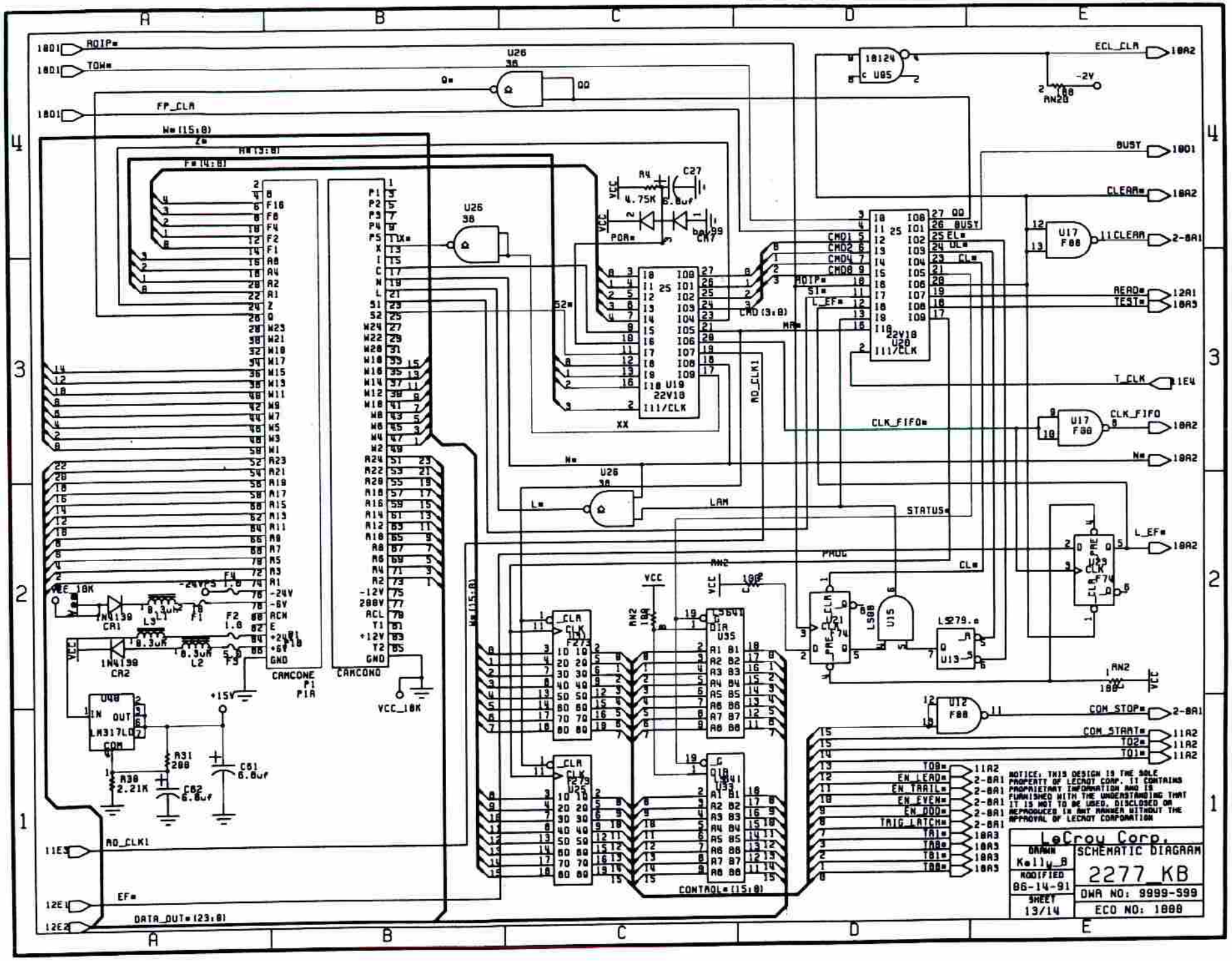
VCC
Vee
+15V
GND4 GND9 GND11 GND5
GND10 GND15 GND1 GND3
AL5842a
U32
U37
U36
U34
U38
DATA OUT<23:0>
EF
HIT DATA<23:0>
WRITE
CLK_FIFO
READ
CLEAR


ADIP*
TOW*
FP_CLR
W*(15:8)
Z*
A*(3:0)
F*(4:0)
U26
38
Q*
QQ
18124
U85
ECL_CLR
-2V
AN28
BUSY
CLEAR*
U17
F08
CLEAR
READ*
TEST*
T_CLK
CLK_FIFO
CLK_FIFO*
N*
L*
LAM
STATUS*
L_EF*
PROG
CL*
AN2
VCC
VEE 18K
-24V
-6V
+24V
+6V
+15V
VCC_18K
CAMCONE
CAMCONO
P1
P1A
CR1
CR2
1N4139
L1
L2
L3
F1
F2
F3
F4
F5
U48
LM317LC
COM
R31
200
R30
2.21K
C61
6.8uF
C62
6.8uF
R4
4.75K
C27
6.8uF
PDA*
CM7
XX
U19
22V10
I11/CLK
CMD1
CMD2
CMD4
CMD8
CMD(3:0)
ADIP*
ST1*
L_EF*
MR*
AD_CLK1
U35
U41
U33
U25
U15
U13
U29
F74
F273
F279
LS640
LS279.a
LS08
CONTROL*(15:0)
COM_STOP*
COM_START*
TO2*
TO1*
TO0*
EN_LEAD*
EN_TRAIL*
EN_EVEN*
EN_ODD*
TRIG_LATCH*
TA1*
TA0*
TB1*
TB0*
DATA_OUT*(23:0)
EF*
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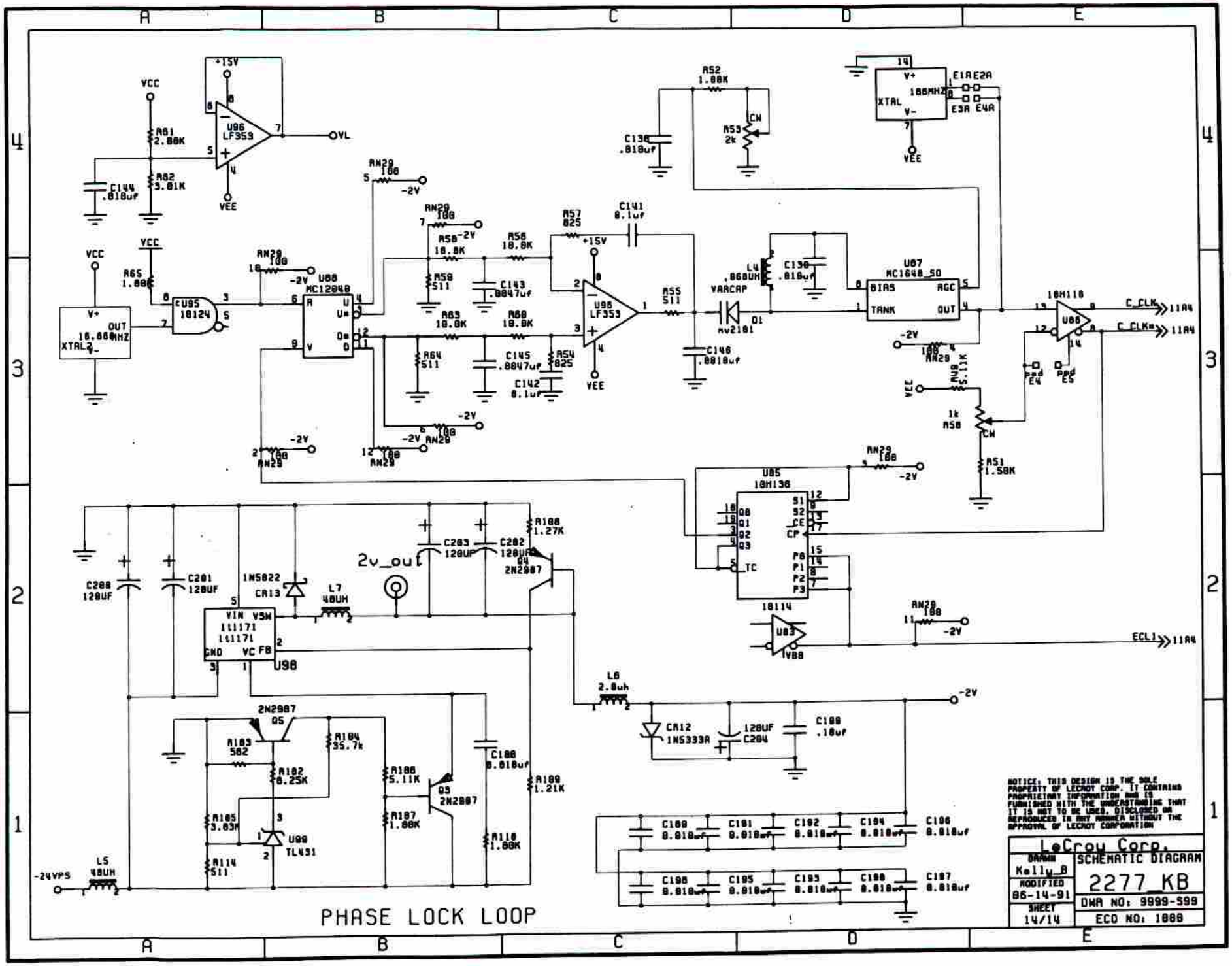
SCHEMATIC DIAGRAM
DRAWN
Kelly B
MODIFIED
06-14-91
SHEET
13/14
2277 KB
DWA NO: 9999-S99
ECO NO: 1000


PHASE LOCK LOOP
LeCroy Corp.
SCHEMATIC DIAGRAM
2277 KB
DWN NO: 9999-599
ECO NO: 1088
DRAWN Kelly_B
MODIFIED 06-14-91
SHEET 14/14
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2v_out
C_CLK
C_CLK=
ECL1
-24VPS
VCC
VEE
VL
XTAL
186MHZ
U86 LF359
U88 LF353
U87 MC1648_SO
U85 10H136
U86 10H116
U83 10114
U89 TL431
U95 10124
U98 MC12048
Q4 2N2907
Q5 2N2907
Q3 2N2907
CR13 1N5822
CR12 1N5333A
L4 .868UH
L5 48UH
L6 2.8uh
L7 48UH
VARCAP MV2101
R52 1.88K
R53 2k
R54 825
R55 511
R56 18.8K
R57 825
R58 18.8K
R59 511
R60 18.8K
R61 2.88K
R62 3.81K
R63 18.8K
R64 511
R65 1.88K
R102 8.25K
R103 562
R104 35.7k
R105 3.83K
R106 5.11K
R107 1.88K
R108 1.27K
R109 1.21K
R110 1.88K
R111 511
R114 511
R58 1k
R59 5.11K
R51 1.58K
C130 .818uf
C131 .818uf
C132 .818uf
C133 .818uf
C134 .818uf
C135 .818uf
C136 .818uf
C137 .818uf
C138 .818uf
C139 .818uf
C140 .818uf
C141 8.1uf
C142 8.1uf
C143 .0047uf
C144 .818uf
C145 .0047uf
C146 .0818uf
C201 128UF
C202 128UF
C203 128UF
C204 128UF
C208 128UF
C188 .18uf
RN29 100
Pad E4
Pad E5
E1A E2A
E3A E4A

PART NUMBER	DESCRIPTION REMARK	QTY PER
106448104	CAP CERA MONO .1UF C199	1
146654120	CAP MINI ALUM 20% 120 UF C200 C201 C202 C203 C204	5
208591171	IC SWITCH REG 2.5A 100KHZ LT1171 U98	1
208591431	IC ADJ SHUNT REG TL431 U99	1
235050001	DIODE RECTIFIER 1N4139 CR1 CR2	2
240035333	DIODE ZENER 3.3V 1N5333A CR12	1
253065822	DIODE SCHOTTKY 1N5822 CR13	1
256030095	DIODE LED RED/GRN CQX-95 CR9	1
256232216	DIODE LED (RED) TIL216-1 CR8	1
256432212	DIODE LED (YEL) TIL212-1 CR10	1
256532232	DIODE LED (GRN) TIL232-1 CR11	1
300050001	CHOKE FERRITE SINGLE LEAD L1 L2 L3	3
300050002	CHOKE FERRITE SINGLE LEAD L6	1
302380480	FILTER CHOKE 2 AMP 48 UH L5 L7	2
309040125	CYRSTAL OSCILLATOR 125 MHZ XTAL	1
403119234	HDR DBL ROW RT ANGL 34 J2 J3 J4	3
408110008	TERMINAL DOUBLE TURRET GND1 GND3 GND4 GND5 GND9 GND10 GND11 GND15 2V OUT	9
433220001	FUSE PICO II 125V 10 AMP F1	1
433221004	FUSE PICO II 125V 1 AMP F2 F4	2
433225001	FUSE PICO II 125V 5 AMP F3	1
454310002	HDR DIP SOLD TO PC BD 2 J5 J6 J7 J8 J9 J10	6
454711012	HDR SOLD TAIL/MALE 12 J1	1
500460005	MOUNTING KIT FOR TO-220	1
521000004	SPACER HEX 2-56X.417	4
540203001	SIDE COVER CAMAC STD(LIP)	1

PART NUMBER	DESCRIPTION REMARK	QTY PER
540206178	RAIL CAMAC STD BOT W/LIP	1
540209101	REAR PANEL CAMAC SIZE 1	1
540213001	SIDE COVER LEFT GENERIC/RSD	1
555430003	CAPTIVE SCREW ASSEMBLY	1
560256005	SCREW PHILIPS 2-56X5/16	4
560440003	SCREW PHILIPS 4-40X3/16	4
560440004	SCREW PHILIPS 4-40X1/4	2
567440006	SCREW FLAT PHIL 4-40X3/8	2
568256002	SCREW FLAT PHIL 2-56X1/8	4
704208001	RAIL CAMAC TOP 4208	1
712277000	PC BD PREASS'Y 2277	1
722277001	FRONT PNL PREASS'Y 2277	1
MTD132	IC MULTI-HIT TDC U41 U42 U43 U44 DO NOT SEND WITH KIT	4
SM185457102	RES VARI CERMET 1 K R50	1
SM185457502	RES VARI CERMET 5 K R11 R14 R21 R27	4
SM190242471	RES NETWORK 470 OHMS R111 R112 R113	3
SM190342221	RES NETWORK 220 OHMS RN5 RN9 RN13 RN17	4
SM190342560	RES NETWORK 56 OHMS RN21 RN22 RN23 RN24 RN25 RN26 RN27 RN28	8
SM190362101	RES NETWORK 2% 100 OHMS RN1 RN2 RN3 RN4 RN6 RN7 RN8 RN10 RN11 RN12 RN14 RN15 RN16 RN18 RN19 RN20 RN29	17
SM200142273	IC OCTAL D-TYPE FLOP 74F273 U25 U31	2
SM200167131	IC M-S TYP D FLOP 10H131 U45	1
SM200167211	IC 3-IN/3-OUT NOR 10H211 U9 U18	2
SM200170020	IC QUAD OR GATE 74F02D U27	1
SM200172000	IC 2-INPUT NAND 74F00 U12 U17	2
SM200172030	IC 8-IN NAND GATE 74LS30D U89 U90	2
SM200172074	IC D-TYP FLOP 74F74 U21 U23	2
SM200174008	IC 2-INPUT AND 74LS08 U15 U22	2
SM200174032	IC 2-IN POS OR 74LS32 U11 U16 U28	4

PART NUMBER	DESCRIPTION REMARK	QTY PER
SM200174032	IC 2-IN POS OR 74LS32 U29	4
SM200174038	IC 2-IN NAND 74LS38 U26	1
SM200267136	IC HEX COUNTER 10H136 U4	1
SM200270393	IC BIN COUNTER 74LS393 U30	1
SM200272161	IC 4-BIT SYNCHR COUNTER 74F161 U6 U10	2
SM200274123	IC MONOST MULTIVIBR LS123 U1 U2	2
SM200278040	IC COUNTER HCT4040 U7	1
SM200467130	IC LATCH 10H130 U49 U50 U51 U52 U61 U62 U63 U64 U67 U68 U69 U70 U79 U80 U81 U82	16
SM200470279	IC QUAD F-F LATCH 27LS279 U13	1
SM201164113	IC 4X EXL-OR W/EN 10113 U55 U56 U57 U58 U73 U74 U75 U76	8
SM204042015	IC LINE RECEIVER 10114 U48 U53 U54 U59 U60 U65 U66 U71 U72 U77 U78 U83 U84	13
SM205728210	IC PAL C 22V10-25 U5 U19 U20 U24 DO NOT SEND WITH KIT MUST BE PROGRAMMED.	4
SM206376641	IC 8X BUS XCEIVER 74LS641 U33 U35	2
SM206550425	IC 1K X 9 FIFO MEM CY7C425 U34 U38 U39	3
SM206876642	IC 8X BUS XCEIVR 74ALS642A U32 U36 U37	3
SM207360124	IC TRANSLATOR MC10124 U46 U91 U92 U93 U94 U95	6
SM207360125	IC TRANSLATOR MC10125 U3 U47	2
SM207460116	IC LINE RECEIVER 10H116 U86	1
SM207974151	IC 8-IN MUX 74LS151 U8	1
SM208470347	IC J-FET OP AMP 347 U14	1
SM208470353	IC DUAL OP AMP 353 U96	1

PART NUMBER	DESCRIPTION REMARK	QTY PER
SM208881317	IC ADJ VOLT REG LM317 U40	1
SM236030099	DIODE SO-PKG BAV99 CR3 CR4 CR5 CR6 CR7	5
SM275132907	TRANSISTOR PNP 2907A Q1 Q2 Q3 Q4 Q5	5
SM400100028	SOCKET SMT TO SMT 28-PIN U5 U19 U20 U24	4
SM400100068	SOCKET SMT TO SMT 68-PIN U41 U42 U43 U44	4
SM653181273	RES THICK FILM 1% 56.2 OHMS R43 R44 R47 R48 R71 R72 R73 R74	8
SM653181314	RES THICK FILM 1% 150 OHMS R37 R38	2
SM653181326	RES THICK FILM 1% 200 OHMS R31	1
SM653181330	RES THICK FILM 1% 221 OHMS R36 R41 R42	3
SM653181365	RES THICK FILM 1% 511 OHMS R100 R101 R114	3
SM653181369	RES THICK FILM 1% 562 OHMS R103	1
SM653181393	RES THICK FILM 1% 1.00 K R65 R66 R67 R68 R69 R70 R107 R110	8
SM653181401	RES THICK FILM 1% 1.21 K R109	1
SM653181403	RES THICK FILM 1% 1.27 K R108	1
SM653181410	RES THICK FILM 1% 1.50 K R51	1
SM653181422	RES THICK FILM 1% 2.00 K R61	1
SM653181426	RES THICK FILM 1% 2.21 K R30	1
SM653181439	RES THICK FILM 1% 3.01 K R62	1
SM653181449	RES THICK FILM 1% 3.83 K R105	1
SM653181450	RES THICK FILM 1% 3.92 K R5 R9 R24 R28	4
SM653181458	RES THICK FILM 1% 4.75 K R4	1
SM653181461	RES THICK FILM 1% 5.11 K R49 R106	2
SM653181481	RES THICK FILM 1% 8.25 K R102	1

PART NUMBER	DESCRIPTION REMARK	QTY PER
SM653181489	RES THICK FILM 1% 10.0 K R6 R7 R10 R12 R13 R15 R16 R17 R18 R19 R20 R22 R23 R25 R26 R29 R39 R40	18
SM653181542	RES THICK FILM 1% 35.7 K R104	1
SM653181614	RES THICK FILM 1% 200 K R1 R2 R3	3
SM661196103	CAP CERA CHIP 10% .01 UF C8 C72 C74 C75 C144 C153 C154 C155 C156 C157 C158 C159 C160 C161 C162 C163 C164 C165 C166 C167 C168 C169 C170 C171 C172 C173 C174 C175 C176 C177 C178 C179 C180 C181 C182 C183 C184 C188 C189 C190 C191 C192 C193 C194 C195 C196 C197 C198 C205 C206	50
SM661207102	CAP CERA CHIP 20% .001 UF C21 C22 C23 C187	4
SM661207104	CAP CERA CHIP 20% .1 UF C1 C3 C4 C6 C9 C10 C12 C13 C14 C15 C16 C17 C18 C19 C28 C29 C30 C31 C32 C33 C34 C35 C36 C37 C38 C40 C41 C43 C44 C45 C46 C47 C48 C49 C51 C52 C53 C54 C55 C56 C58 C64 C65 C66 C68 C69 C70 C71 C73 C76 C77 C78 C79 C80 C81 C82 C99 C100 C101 C102 C103 C104 C105 C106 C108 C126 C127 C128 C129 C131 C132 C133 C134 C135 C136 C137 C142 C146 C147 C148 C149 C150 C151 C152 C185	85
SM661255470	CAP CERA CHIP 5% 47 PF C83 C84 C85 C86	32

PART NUMBER	DESCRIPTION REMARK	QTY PER
SM661255470	CAP CERA CHIP 5% 47 PF C87 C88 C89 C90 C91 C92 C93 C94 C95 C96 C97 C98 C110 C111 C112 C113 C114 C115 C116 C117 C118 C119 C120 C121 C122 C123 C124 C125	32
SM661506684	CAP CERA CHIP 10% .68 UF C2 C5 C7	3
SM666227685	CAP MOLD TANT CHIP 6.8 UF C27 C61 C62	3
SM666247106	CAP MOLD TANT CHIP 10 UF C11 C24 C25 C26 C39 C42 C50 C57 C59 C60 C63 C67 C107 C109 C130 C186	16

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