Model 566
Time-to-Amplitude
Converter (TAC)
Operating and Service Manual

Printed in U.S.A.

EG&G ORTEC Part Number 678950
Manual Revision A

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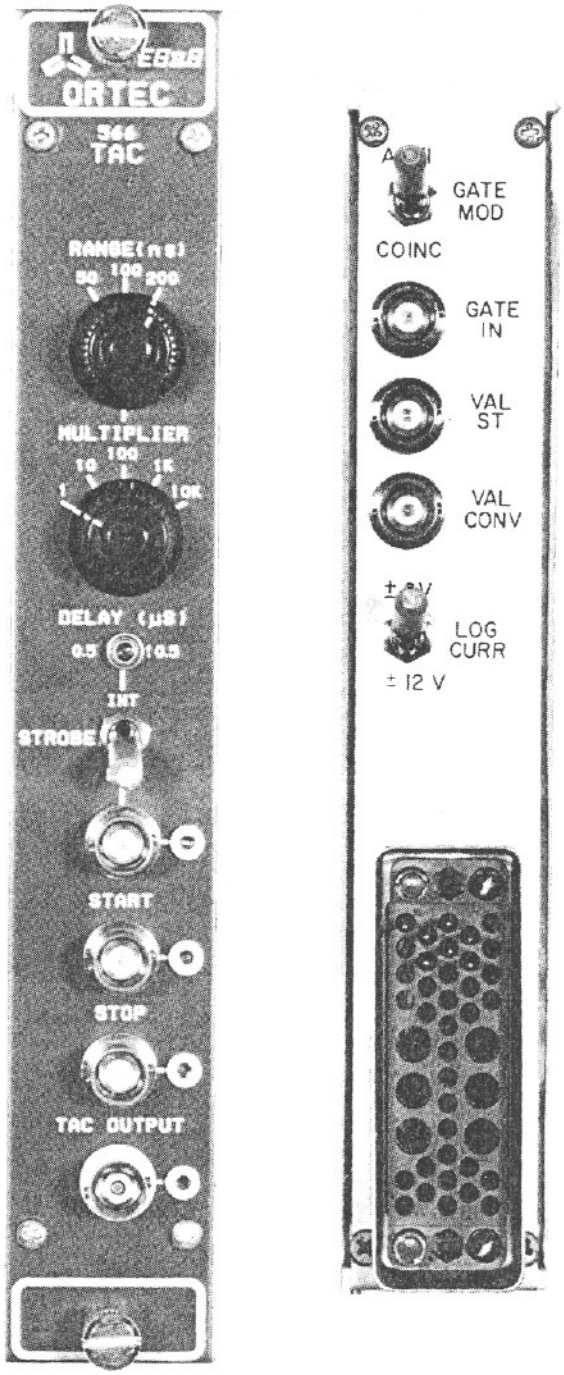
CONTENTS

ILLUSTRATIONS


ORTEC
366
TAC
RANGE (ns)
50
100
200
MULTIPLIER
10
100
1K
1
10K
DELAY (µs)
0.5
0.5
INT
STROBE
START
STOP
TAC OUTPUT
GATE
MOD
COINC
GATE
IN
VAL
ST
VAL
CONV
LOG
CURR
± 12 V

EG&G ORTEC MODEL 566 TIME-TO-AMPLITUDE CONVERTER

1. DESCRIPTION

1.1. PURPOSE AND FEATURES

The EG&G ORTEC 566 Time-to-Amplitude Converter (TAC) is a single-width NIM-standard module that measures the time interval between pulses to its start and stop inputs and generates an analog output pulse proportional to the measured time. Timing experiments requiring time ranges of 50 ns to 2 ms (10 ns to 2 ms usable time range) may be performed giving the experimenter flexibility in analyzing random nuclear events that occur within a selected time range. Time ranges from 50 ns to 2 ms are provided via the front panel controls.

The 566 Start input can be inhibited by a pulse or a dc level at the rear panel Gate In input connector.

Valid Start and Valid Conversion outputs are provided on the rear panel for each accepted start and stop input respectively. The duration of the Valid Start output indicates the interval from the accepted start until the end of reset. Valid Conversion occurs from the end of the internal delay after stop to the end of reset.

The selectable TAC output width and variable delay, which are easily adjustable, further serve to make the 566 a flexible instrument that can be easily adapted into many time spectroscopy systems. The output of the TAC may be synchronized with the stop signal or an external strobe signal to further enhance its versatility.

The 566 is dc-coupled and gated so that input count rates will not paralyze or otherwise hinder normal operation. The TAC output should be connected to the dc-coupled input of a multichannel analyzer (MCA) for optimum high-count-rate performance.

1.2. OPERATION

Start-to-stop time conversion is accomplished only after a valid start has been identified and after a stop pulse has arrived within the selected time range. The start input is disabled during the busy interval to prohibit pileup; the stop input is disabled after the first accepted stop signal. The input gate for the start circuit can be operated in either an anticoincidence or a coincidence mode.

Time ranges may be switch-selected for full-scale intervals from 50 ns to 2 ms. Each time measurement is analog-stored in a low-loss stretcher amplifier until a linear gate is opened by either an internal or an external strobe. The internal strobe can be obtained from either the start or the stop input pulse and in either case occurs automatically at a selected delay following the reference. An external strobe can be used for a prompt output at the strobe time provided that a time measurement has been completed and reset has not occurred. If reset occurs before a strobe, no TAC output signal is available. Reset also occurs if the start-to-stop time interval exceeds the range that is selected.

1.3. LOGIC

An input can be accepted through the Start input connector on the front panel unless the 566 is busy processing a previous set of information or the response is inhibited by a gate input condition. The acceptance of a start input is essential in order to initiate a response in the 566. When a start input is accepted, a positive logic signal is available through the rear panel Valid Start output connector and is continued until the leading edge of a subsequent reset. The reset can be caused by a TAC output or by the sensing of an overrange condition. The start signal permits the internal circuits to start measuring a time interval and enables the stop input circuit.

The Stop input BNC can accept an input signal after it has been enabled by the start condition. It may be enabled immediately after start. When a stop input signal is accepted, this indicates that an interval has been measured and its analog equivalent is stored and available. A signal is furnished through the Valid Converter output that continues until the leading edge of a subsequent reset. If no stop input is accepted before an overrange condition is sensed, the measurement will be aborted and no output signals for the TAC will be generated.

The TAC output must be strobed. The source of the strobe can be switch-selected from the internal signal or from an external signal. If internal is selected, the strobe occurs after a delay that has been adjusted with the front panel TAC Output delay control, 0.5 μs to 10.5 μs after the leading edge of the signal. If the Strobe switch is set at Ext, a signal must be furnished through the Strobe Ext BNC connector to strobe the output promptly.

2. SPECIFICATIONS

2.1. PERFORMANCE

TIME RESOLUTION FWHM ≤0.01% of full scale plus 5 ps for all ranges.

TEMPERATURE INSTABILITY ≤±0.01%/°C (±100 ppm/°C) of full scale or 10 ps/°C (whichever is greater), 0 to 50°C.

DIFFERENTIAL NONLINEARITY ≤±2% from 10 ns to 2% of full scale (whichever is greater) to 100% of full scale.

INTEGRAL NONLINEARITY ≤±0.1% from 10 ns to 2% of full scale (whichever is greater) to 100% of full scale.

RESET CYCLE Fixed 1.0 μs for X1 and X10 Multipliers; fixed 5 μs for X100 Multiplier; and fixed 50 μs for X1k and X10k Multipliers. Occurs after Overrange, Strobe cycle, or Ext Strobe Reset cycle.

START-TO-STOP CONVERSION TIME Minimum ≤5 ns.

2.2. FRONT PANEL CONTROLS

RANGE (ns) Three-position rotary switch selects full scale time interval of 50, 100, or 200 ns between accepted Start and Stop input signals.

MULTIPLIER Five-position rotary switch extends time range by a multiplying factor of 1, 10, 100, 1k, or 10k.

DELAY (μs) 20-turn screwdriver-adjustable potentiometer varies the delay of the TAC output from 0.5 μs to 10.5 μs, relative to an accepted Stop input signal; operable in the Int Strobe mode only.

STROBE MODE Two-position locking toggle switch selects either Internal or External source for initiating the strobe cycle to strobe valid information from the TAC output.

2.3. REAR PANEL CONTROLS

GATE MODE Two-position locking toggle switch selects Coincidence or Anticoincidence mode of operation for the Start circuitry. Start circuitry is enabled in the Coinc position or inhibited in the Anti position during the interval of a Gate input signal.

LOG CURR Two-position locking toggle switch selects the use of ±6 V or ±12 V bin lines to provide current for the internal logic circuitry.

In the ±6 V position the 566 is within the current allotment for a single NIM width when using a NIM-standard Class V power supply. In the ±12 V position the 566 exceeds the current allotment for a single NIM width on the +12 V and −12 V bin lines. However, this position allows the 566 to be used with power supplies not providing +6 V and −6 V.

2.4. INPUTS

All four inputs listed below are dc-coupled, edge-triggered, and printed wiring board (PWB) jumper selectable to accept either negative or positive NIM-standard signals. Input impedance is 50 Ω in the negative position and >1 kΩ in the positive position. The threshold is ~=400 mV in the negative position and ~+2 V in the positive position.

STROBE Front panel BNC connector provides an external means to strobe a valid output signal from the TAC in the Ext Strobe mode. The input signal, exceeding threshold within the Ext Strobe reset interval after the Stop input, initiates the read cycle for the linear gate to the TAC output. Factory-set in the positive input position. Ext Strobe reset interval has a minimum value of ~0.5 μs and a maximum value of nominally 10 μs.

START Front panel BNC connector initiates time conversion when Start input signal exceeds threshold. Factory-set in negative input position.

STOP Front panel BNC connector terminates time conversion when Stop input signal exceeds threshold. Factory-set in negative input position.

GATE IN Rear panel BNC connector provides an external means of gating the Start circuitry in either Coincidence or Anticoincidence with the Start input signal. Gate input signal must cross threshold ≥10 ns prior to the Start input signal and must overlap the trigger edge of the Start input signal. Factory-set in the positive input position.

2.5. OUTPUTS

TAC OUTPUT Front panel BNC connector provides unipolar pulse.

Amplitude 0 V to +10 V proportional to Start/Stop input time difference.

Time End of delay period in Int Strobe mode; prompt with Strobe input in Ext Strobe mode.

Width Adjustable by PWB potentiometer from ≤1 μs to ≥3 μs.
Impedance $Z_o < 1\ \Omega$.
Rise Time ~250 ns.
Fall Time ~250 ns.

VAL ST Rear panel BNC connector provides NIM-standard slow-positive logic level signal.
Amplitude Nominally +5 V. Complement signal selectable by PWB jumper.
Time and Width From accepted Start input to end of reset.
Impedance $Z_o < 10\ \Omega$.
Rise Time ≤50 ns.
Fall Time ≤50 ns.

VAL CONV Rear panel BNC connector provides NIM-standard slow-positive logic level signal to indicate a Valid Conversion.
Amplitude Nominally +5 V. Complement signal selectable by PWB jumper.
Time and Width From end of internal delay after Stop to end of reset.
Impedance $Z_o < 1\ \Omega$.
Rise Time ~250 ns.
Fall Time ~250 ns.

2.6. ELECTRICAL AND MECHANICAL

POWER REQUIRED (Log Switch)
±6 V +24 V, 35 mA; −24 V, 50 mA; +12 V, 70 mA; −12 V, 105 mA; +6 V, 140 mA; −6 V, 300 mA.
±12 V +24 V, 35 mA; −24 V, 50 mA; +12 V, 210 mA; −12 V, 405 mA.

WEIGHT
Net 1.5 kg (3.3 lb).
Shipping 3.0 kg (7.0 lb).
DIMENSIONS NIM-standard single-width module 3.43 x 22.13 cm (1.35 x 8.714 in.) per TID-20893 (Rev).

3. INSTALLATION

3.1. GENERAL

The EG&G ORTEC 4001A/4002A, 4001A/402D, or 4001C/402D Bin and Power Supply (or equivalent), in which the 566 will be installed, is intended for rack mounting. If vacuum tube equipment is operated in the same rack, there must be sufficient cool air circulating to prevent localized heating of the all-transistor circuits in the 566 and in the other modules in the bin and power supply. Rack-mounted equipment subjected to the temperatures in vacuum tube equipment can exceed the maximum for which the transistorized circuits are designed unless this precaution is taken. The 566 should not be subjected to temperatures in excess of 120°F (50°C).

3.2. CONNECTION TO POWER

The 566 is designed per TID-20893 and accepts its operating power requirements through a mating power connector when it is installed in an EG&G ORTEC 4001A/4002A Bin and Power Supply. As a safety precaution, always turn off the power for the bin before inserting or removing any modules. Monitor the dc voltages at the test points on the control panel of the bin after all modules have been installed and the power is turned on in order to determine that none of the four power levels have been reduced by an overload.

3.3. CONNECTION INTO A SYSTEM

The 566 can accept both start and stop pulses from NIM modules that furnish NIM-standard positive and fast-negative logic signals or from the timing output of a photomultiplier tube base. Typical EG&G ORTEC instruments that provide compatible signals are the 583, 584, and 473A discriminators and the 265, 269, 270, and 271 photomultiplier tube bases. The start and stop inputs will properly terminate 50 Ω cable, and this type is recommended to ensure proper termination of the signals.

No input or output connectors need be terminated when they are not in use.

In any experiment in which it is reasonable to assume that the count rates for start and stop will be equal or nearly equal, use the signal furnished from the origin of events into the start input and the signal furnished from the response into the stop input. The 566 will then measure the time difference (T) from origin to response and furnish an output amplitude that is some fraction of the selected full-scale amplitude, proportional to the ratio of T, to the selected full-scale time range.

In any experiment in which the two count rates differ noticeably, such as one in which fewer responses than event origins can be expected, use the lower count rate as the start input to the 566. This assures that the 566 dead time will be minimized because it analyzes the time difference only after a start signal is accepted. When the response is used as a start signal, furnish the signals from the origin of events through a delay line into the stop input, and adjust the delay to match the selected full-scale time of the 566. At each start input signal the 566 will analyze the time until its related origin signal is furnished to the stop input. The time measured is then delay time minus T, and produces a so-called inverted time spectrum. The purpose of this type of system connection is to reduce the number of conversions and the corresponding dead time during the experiment. For each signal accepted through the start input there must be a conversion, but for each signal through the stop input there need not be a conversion. For each start signal that is not followed by a stop signal within the selected time full range, the converter measures a time equal to the total range, even though no output pulse is generated.

3.4. LINEAR OUTPUT SIGNAL CONNECTIONS AND TERMINATING IMPEDANCE

The source of impedance of the standard TAC output, with the 0 to 10 V linear range, is about 1 Ω through the connector on the front panel.

For the front panel circuit, the interconnection to other modules does not usually require any special considerations, especially if the interconnecting cable is shorter than 4-ft in length. Paralleling several loads on a single output will still not reduce the 0 to 10 V signal span significantly unless the combined load is <100 Ω.

As with any analog instrument, oscillations may be observed occasionally when unterminated lengths of cable are used. Short cable lengths (up to 4 ft) need not be terminated. When longer cable lengths are required for transfer of a linear signal, the cable should be terminated in a resistive load equal to the cable impedance to prevent reflections and oscillations in the cable. Oscillation suppression can be effected by either a series termination at the sending end of the cable or by a shunt termination at the receiving end. For convenience a BNC tee can usually accommodate both the cable and a mating terminator at the input of the receiving instrument. These units are available commercially, including BNC terminators with nominal values of 50, 100, and 1000 Ω. EG&G ORTEC stocks a limited quantity of all but the 1000 Ω terminators for your convenience, as listed below:

BNC Tee Connector	C-29
50 Ω Terminator	C-28
100 Ω Terminator	C-27

When a shunt termination at the receiving end of the cable is impractical, consider series termination at the sending end. For a series termination the full signal amplitude

span is available at the receiving end only if the input impedance is many times the characteristic impedance of the cable. For series termination install the correct resistance between the actual amplifier output on the etched circuit board and the output connector. Effectively, the terminating resistance is in series with the input impedance of the receiving instrument, and may result in some loss in signal amplitude. For example, if the series terminator is 93 Ω and the driven load is 900 Ω, the available signal span will be only about 90% of the maximum signal amplitude for each pulse. The termination of a 93 Ω cable in a 93 Ω load will cause ~50% loss for the signal.

3.5. LOGIC SIGNAL CONNECTIONS

The start and stop input circuits accept positive or negative NIM-standard signals. Each of these input circuits is jumper selectable. Input impedance of 50 Ω for negative signals or >1 kΩ for positive signals is intended as the proper termination for the signals.

Impedance considerations for each of the remaining logic inputs and output for the 566 are noncritical and 93 Ω cable is usually used. They can be terminated with 100 Ω to prevent ringing if the signal is used to drive a high-impedance load.

4. OPERATING INSTRUCTIONS

4.1. TIME-TO-AMPLITUDE CONVERSION

There are four front panel controls and two rear panel controls on the 566. Of these, four are directly associated with the conversion of a start-to-stop interval into an analog equivalent TAC output pulse. These controls are Range (ns), Multiplier, Delay (μs), and Anti/Coinc.

The Range (ns) and Multiplier switches determine the full-scale limit for time conversion. Any of 15 combinations may be selected as follows:

Switch Settings		Full-Scale Time Limit
Range (ns)	Multiplier	
50	X1	50 ns
100	X1	100 ns
200	X1	200 ns
50	X10	500 ns
100	X10	1 μs
200	X10	2 μs
50	X100	5 μs
100	X100	10 μs
200	X100	20 μs
50	X1k	50 μs
100	X1k	0.1 ms
200	X1k	0.2 ms
50	X10k	0.5 ms
100	X10k	1 ms
200	X10k	2 ms

For example, with the Range switch set at 50 and the Multiplier switch at X100, the full-scale time range is 5 μs. Any stop input signal that occurs within 5 μs after a valid-start signal will initiate the gating of an output pulse through the TAC Output connector. The output pulse will not be furnished through this connector unless it is strobed. The strobe condition is selected by a front panel switch. When the output does occur, its peak amplitude will be proportional to the ratio of the measured start-to-stop interval to the selected full-scale time in a 0 to 10 V range.

Internal logic eliminates any pulse ambiguity. No output pulse is furnished unless a stop signal is accepted within the selected full-range time. A stop signal is not effective unless it is preceded by a valid-start signal. For further logical control either a coincidence or anticoincidence mode can be selected for gating control of the start input circuit. To eliminate gating for the start input, set the Gate Mod switch at Anti/Coinc and leave the gate input circuit without any connection. When the same switch setting is used and an input signal is furnished, start signals are not accepted when the gate signal is +2 V or more.

For coincidence gating of the start input circuit, set the Gate switch at Coinc and furnish a signal of +2 V or more through the Gate logic Input connector when start signals are to be accepted.

The front panel Strobe switch selects the source for the strobe signal for the TAC output. When the switch is set at Int, the strobe is generated by a delayed, valid-start signal, and the delay is fixed at a time that is longer than the selected full range time.

5. CIRCUIT DESCRIPTION

A schematic and PWB component layout are included in the back of this manual. Please refer to these figures in the circuit description given below.

5.1. START CIRCUITRY

The start circuitry is used to generate a logic signal which begins the time-to-amplitude conversion in the 566. Two inputs, the START (front-panel) and the GATE IN (rear-panel) are used to control the start circuitry. The GATE IN allows START signals to be blocked by a user supplied logic signal. The user can select blocking in coincidence or anticoincidence mode via a rear-panel switch. Also, PWB jumpers allow the selection of either positive or negative NIM logic signals for both the START and the GATE IN.

The input circuitry for the START and the GATE IN provide for the proper termination of the input signals, level-shifting, and buffering. The START input circuitry consists of Q1, Q2, 1/2 of U1, J3, D4–D6, and associated passive components, while the GATE IN input circuitry includes Q3, Q4, 1/2 of U1, J4, D1–D3, and associated passive components.

If the GATE IN signal meets the proper coincidence/anticoincidence condition selected by the user, an ECL logic true level is set on U2(7), the D input of a dual ECL flip-flop, allowing a START signal to set this flip-flop. The Q output of this flip-flop [U2(2)] sets the other 1/2 of U2, place U2(15) in the ECL true state and U2(14) in the ECL false state. These two signals go through level-shifting transistors Q10, Q11, and Q15, and turn transistor Q17 off. Then, the current which was flowing through Q17 discharges C38 and any other capacitor selected by the front panel MULTIPLIER switch. This discharging will continue until halted by the stop circuitry.

The discharge rate of C38 is set by the precision current source comprised of U7, Q29, D19, and associated passive components. Both the RANGE switch and the MULTIPLIER switch control the magnitude of this current source.

A logic signal is generated on the VALID START output by each start signal which is enabled by the GATE IN. This signal extends from the beginning of the start pulse until the TAC is reset.

5.2. STOP CIRCUITRY

The stop circuitry generates a logic signal which ends the time-to-amplitude conversion in the 566. This circuitry is controlled by the front-panel STOP input, and a PWB jumper allows the selection of either a positive or negative NIM logic signal for STOP.

The STOP input circuitry is identical to the START input circuitry.

When the STOP input becomes active, an ECL flip-flop (1/2 of U4) is set. The Q output of this flip-flop sets the other 1/2 of U4 if a valid START signal has previously set U2(2) to the ECL true state, causing U4(15) to switch to the ECL true state and U4(14) to switch to the ECL false state. These signals propagate through level-shifting transistors Q12, Q13, and Q19 to turn off transistor Q20, terminating the current flow out of C38 and ending the time-to-amplitude conversion cycle.

5.3. GATED BASELINE RESTORER

The voltage on C38 is buffered by Q21–Q23. The voltage on the emitter of Q23 is held to a quiescent value of 0 V by a gated baseline restorer (BLR) consisting of U8, C29, Q26, Q31, Q32, U5, and associated passive components. In the quiescent state, the gated BLR acts as a high-gain feedback circuit which maintains the output of Q23 at 0 V. However, when a valid START signal is received, an ECL false signal on U5(13) disables U8 which opens the feedback path. The proper dc voltage is maintained throughout the loop, though, since the output voltage of U8 is held on C29. After the START flip-flop is cleared, the BLR circuit is again enabled.

5.4. STROBE CIRCUITRY

When the INT position is selected on the STROBE switch, the output signal is gated out by the buffered STOP signal [U5(12)], after a user selected delay time. This delay time is set by the front-panel DELAY potentiometer, which controls the width of the negative-going, TTL logic signal on U10(4). The rising edge of this signal triggers one-shot U15(13), which fires Q41, which opens the linear gate, A4, allowing the output signal to appear at the TAC output.

If the EXT position is selected on the STROBE switch, the logic signal supplied by the user on the STROBE input will control the timing of the TAC output. Either positive or negative NIM logic can be selected for this input via a PWB jumper. If the EXT mode is selected, the STROBE input triggers one-shot U15(13), which opens the linear gate. The user may allow a time window for the STROBE signal of 10 μs or 100 μs. If a strobe signal does not occur in this time window (time window begins with the STOP signal), the TAC output is not enabled, and the 566 is reset.

6. MAINTENANCE

6.1. TESTING PERFORMANCE

The following test procedures are furnished as a guide during installation and checkout of the 566 TAC.

TEST EQUIPMENT The following test equipment is recommended. Each test procedure refers to this list by the unit identification number for the required item(s) of test equipment. An equivalent unit may be substituted for any item in the list, providing that it furnishes the function required for each specific application.

1. Hewlett-Packard 215A Pulse Generator
2. EG&G ORTEC 436 100 MHz Discriminator
3. EG&G ORTEC 416A Gate and Delay Generator
4. EG&G ORTEC 425A Nanosecond Delay
5. Photomultiplier tube with scintillator and radiation source
6. EG&G ORTEC 449 Log/Lin Ratemeter
7. Tektronix Type 475 Oscilloscope
8. EG&G ORTEC 7100, 7150, 7450 Multichannel Analyzer or 918 Multichannel Buffer
9. EG&G ORTEC 414A Fast Coincidence
10. EG&G ORTEC 444 Gated Biased Amplifier

PRELIMINARY PROCEDURES Take the following preliminary steps when the 566 is installed:

1. Check the module visually for possible damage.
2. With the power turned off, install the 566 into a NIM-standard bin and power supply such as the EG&G ORTEC 4001C/4002A.
3. Check the installation for proper mechanical alignment.
4. Switch on ac power and check the dc power voltage levels at test points on the 4001C.

BASIC SWITCH SETTINGS Set the 566 controls as follows:

Range	50 ns
Multiplier	1
Logic Input	Anti/Coinc
Strobe	Int.

CONVERSION TESTS Use the typical test setup shown in Fig. 6.1 and supply a start and stop pair of input signals with known time difference into the 566. Observe the TAC output. Then use the following procedures:

1. Adjust the delay for the stop input to 50 ns.
2. Check to see that the full-scale time range is 50 ns x 1.
3. Measure the signal through the TAC Output connector. It should be about 10 V for a 50 ns delay or 5 V for a 25 ns delay.
4. Turn the Range (ns) switch through its 50, 100, and 200 settings and observe the pulse amplitude at each setting; each successive switch position should decrease the pulse amplitude to about 1/2 of the amplitude for the previous setting.
5. Return the Range (ns) switch to 50 and set the Multiplier switch at 10. The output amplitude should be reduced to about 1/10 of the reading for step 3.

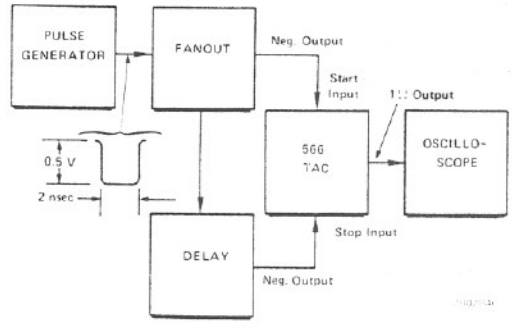


Fig. 6.1. Test System for Checking Conversion.

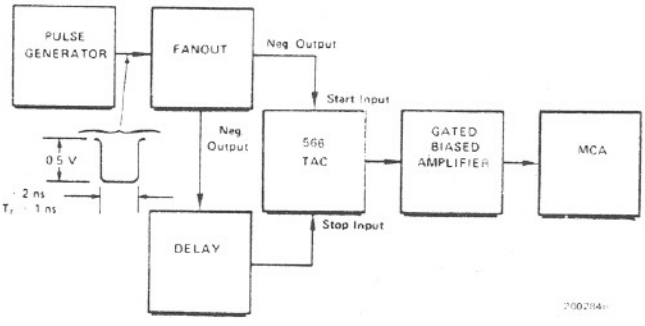


Fig. 6.2. Test System for Checking Converter Resolution.

RESOLUTION TESTS See Fig. 6.2 for the typical test setup used for resolution checks. The start and stop pulses used for this test must have fast rise time and be jitter-free. The minimum delay recommended for the stop pulses is 15 ns. The resolution of any scale can be measured with this setup, and the main consideration is that each stop signal delay be within the linear region of the selected time range. The testing procedure consists of the following:

1. Adjust the delay for the stop input to a basic setting of 30% to 80% of the selected time range.

2. Operate the system and obtain a timing spectrum. Normalize the output amplitude full range for the normally digitized full range of the ADC in the analyzer.

3. After you have accumulated an adequate spectrum to assure statistical accuracy of photopeak measurements (~1000 counts in the peak channel), identify the peak channel number and measure the FWHM channel number limits. Log for reference.

4. Increase the delay for the stop signal by a fixed and known amount. This may be done by switching in a fixed delay line cable (EG&G ORTEC 425A) or by careful adjustment of the delay unit controls. The total delay for the stop signal must still be <100% of the selected time full range.

5. Accumulate a spectrum for this measurement of increased time intervals.

6. Observe the relocated photopeak in the timing spectrum and record its peak channel number and its FWHM channel number limits.

7. Subtract the peak channel number in step 3 from the peak channel number in step 6. This is the number of channels that represents the time variation injected at step 4.

8. Using the formula below, calculate time resolution effective for the established system calibration:

$$\Delta t \text{ per channel} = \text{stop delay increase} \div \text{channel shift.}$$

9. With the equation below, calculate the converter resolution using the FWHM channel width from either step 3 or step 7. These widths should be the same at either peak location.

$$\text{Time resolution (FWHM)} = \text{FWHM channel width} \times \Delta t \text{ per channel.}$$

This resolution is affected adversely by any jitter that may be present in the discriminator and by the resolution of the amplifier. Allowances should be made for these contributions.

COUNT RATE TESTS In many applications it is important for a time-to-amplitude converter to handle high count rates, both external and internal. Since the start input is gated internally and the conversion circuits are all direct-coupled, the limit for its external count rate capability is determined solely by the input pulse width, and there are no pileup effects. The limit on the internal count rate is imposed by the conversion and reset process, where the start input is disabled through a converter busy interval following each accepted start signal. A converter busy interval is the measured time plus ~7 μs for start-stop intervals within the selected time range or is the selected time range plus 4 μs if no stop signal is furnished within the time range.

The following test, based on the system connection shown in Fig. 6.3, permits accumulation of a basic timing spectrum for the start-stop input pulses at 60 Hz. As the external count rate for start only is increased by regulating the random pulse generator, the internal pulse rate in the 566 is increased, and a ratemeter will monitor the resulting rate at which the internal capability is impaired.

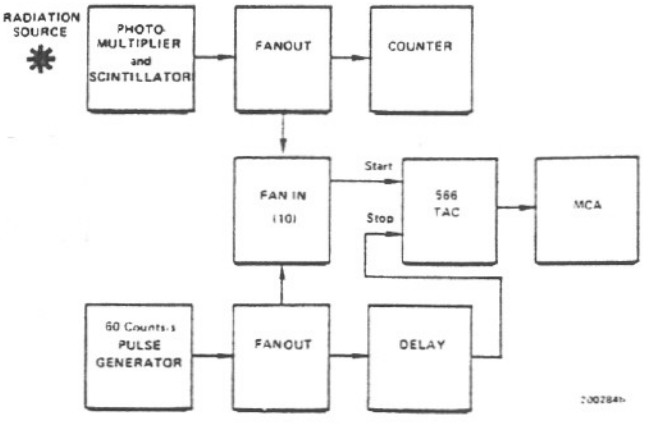


Fig. 6.3. Test System for Checking Count Rate.

1. The photomultiplier may be used as a random pulse generator, triggered by a radiation source. Use an initial sensitivity setting above the energy level for a zero output pulse rate.

2. Adjust the delay for the stop input to ~0.4 μs.

3. Select the 0.5 μs time range with the 566.

4. Adjust the system for a timing spectrum accumulated for the 60-Hz input pulses.

5. Decrease the threshold of the discriminator to generate random start signals with no corresponding stop signals. Monitor the random rate with the ratemeter.

6. Observe the timing spectrum as the random input rate is gradually increased. Watch for interference in the accumulated spectrum.

DIFFERENTIAL LINEARITY MEASUREMENTS A system for testing differential linearity of the 566 is shown in the block diagram in Fig. 6.4. In this system the random pulse generator is used as the source for start signals, and a pulse generator with a fixed rate is used for stop signals. The measurable time interval between a start and stop is a random value, with equal probability that it will be any time difference up to the periods between the regular stop signals. For an infinite number of TAC outputs the count levels for each channel of the MCA should be equal. After the test has been run long enough to assure statistical accuracy (e.g., >25,000 counts/channel), the spectrum should be similar to those illustrated in Fig. 6.5. Any deviation from a straight line represents a differential nonlinearity, and the percent of deviation is the difference between this count level and the average divided by the average count level.

1. Select the 566 time range to be tested.

2. Calculate the maximum stop pulse repetition rate for the selected time range. This should be slightly lower than the reciprocal of the time range. For example, for the 1 μs

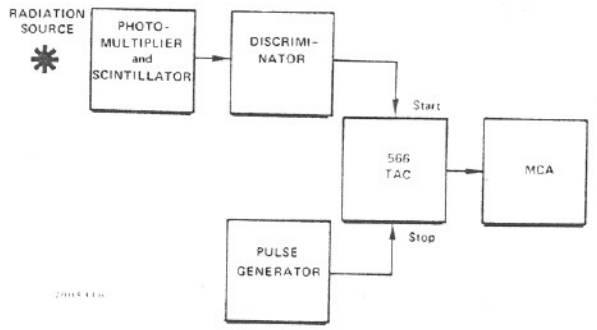


Fig. 6.4. Test System for Checking Differential Linearity.

time range the reciprocal is 1 × 10⁷, and a pulse generator rate of 4 to 5 times 10⁶ should be satisfactory. A lower rate increases the time required to run the test, while a faster rate will reduce the response because of MCA dead time.

3. Operate the system and monitor the dead-time meter on the MCA. Regulate the random start rate to cause the MCA dead time to be ~10%.

4. Clear the analyzer to zero and operate the system until the average count level stored in each channel is sufficient to ensure statistical accuracy.

5. Compare any nonlinearity indications to the specifications listed in Section 2. Some nonlinearity can be expected in channels in the lower 5% of the MCA range as shown in Fig. 6.5 because of the stop pulse width and the TAC gating time.

CHECKING EXTERNAL STROBING MODE The system for checking the external strobing mode is shown in Fig. 6.6. This system can be used to verify the principles of operation of the 566.

1. Set the delay for the stop signal at about 400 ns.

2. Set the 566 time range for 500 ns.

3. Use the internal strobe mode for the 566. Adjust the oscilloscope sweep as required to identify the TAC output pulses.

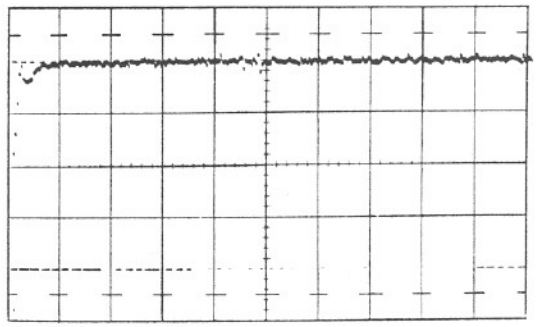
4. Adjust the delay for the strobe signal >500 ns to ensure that it will occur later than the full time range.

5. Switch the 566 to its external strobe mode and observe the TAC output pulse. It should be identical to the pulse observed in step 3 except for the time at which it occurs.

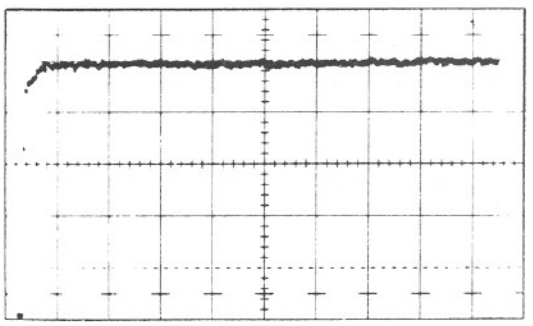
6. Vary the front panel Delay (μs) and observe that there is no change in the TAC output amplitude but that the output delay follows the strobe delay.

6.2. CORRECTIVE MAINTENANCE

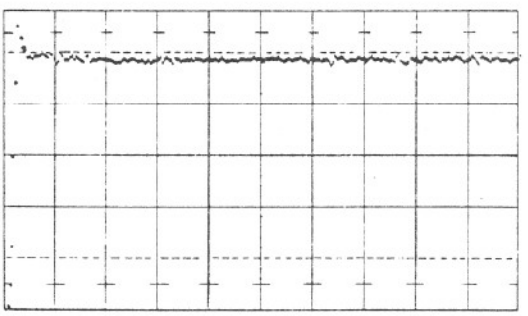
Clean the surfaces of the printed circuits, the connectors, and all chassis parts periodically to prevent accumulated dust from forming leakage paths between the circuit components.



Range = .1
Multiplier = X1 } 100 ns
(Vert): Full Scale 5 x 10^4 counts
(Horiz): Full Scale = 105% range



Range = .1
Multiplier = X10 } 1 μs
(Vert): Full Scale = 5 x 10^4 counts
(Horiz): Full Scale = 105% range



Range = .1
Multiplier = X100 } 10 μs
(Vert): Full Scale = 5 x 10^4 counts
(Horiz): Full Scale = 105% range

Fig. 6.5. Differential Linearity for the Indicated Ranges.

If the instrument is suspected of malfunctioning, use the performance tests of Section 6.1 to aid verification. When incorrect operation is identified, disconnect the 566 from its position in the system and perform routine diagnostic tests with a pulse generator and an oscilloscope. Use the timing chart in Fig. 6.7 to isolate the problem, and use schematic diagram 640400 at the back of this manual to localize the malfunctioning.

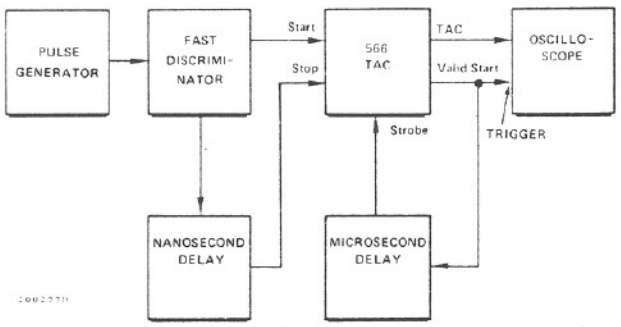


Fig. 6.6. Test System for Checking External Strobing Mode.

CALIBRATION There is one critical calibration and three adjustments that may need to be made.

CONVERSION CURRENT ADJUST Potentiometer R128, located on the PWB adjusts the conversion current.

Using the typical setup shown in Fig. 6.1, follow the setup procedures outlined in "Conversion Tests" steps 1 through 3. Adjust potentiometer R128 counterclockwise to minimum. If the TAC is functioning properly, a pulse output of ~8.5 to 9.8 V should be present on the oscilloscope. If this voltage is not present on the oscilloscope, refer to Section 6.3, "Troubleshooting," or return the unit to the EG&G ORTEC factory for repair as outlined in Section 6.4. If a pulse is present at the TAC output, the conversion current can be calibrated by adjusting R128 clockwise (slowly) until the output pulse obtains an amplitude of +10 V and begins to half-fire. Adjust R128 counterclockwise (slightly) until the pulse is solid or full-firing.

OUTPUT WIDTH ADJUSTMENT Potentiometer R163, located on the PWB, adjusts the TAC output pulse width. The potentiometer should vary the output pulse width from 1 μs to 3 μs. The width can be adjusted to customer requirements; factory-set at ~2 μs.

OUTPUT OFFSET CALIBRATION Potentiometer R223, located on the PWB, adjusts the TAC output offset from −−100 mV to +100 mV. Remove the start and stop signals from the TAC input. Measure the offset voltage at the TAC output connector with a voltmeter. Adjust potentiometer R223 until the offset voltage is 0 mV ± 1 mV.

Capacitor C93, located on the PWB, is used to filter out any linear gate signals from the TAC output pulse. This is factory-set and should not need further adjustment.

6.3. TROUBLESHOOTING

Use the tests in Section 6.1, the circuit description in Section 5, and refer to schematic 640400 to locate the faulty part or parts.

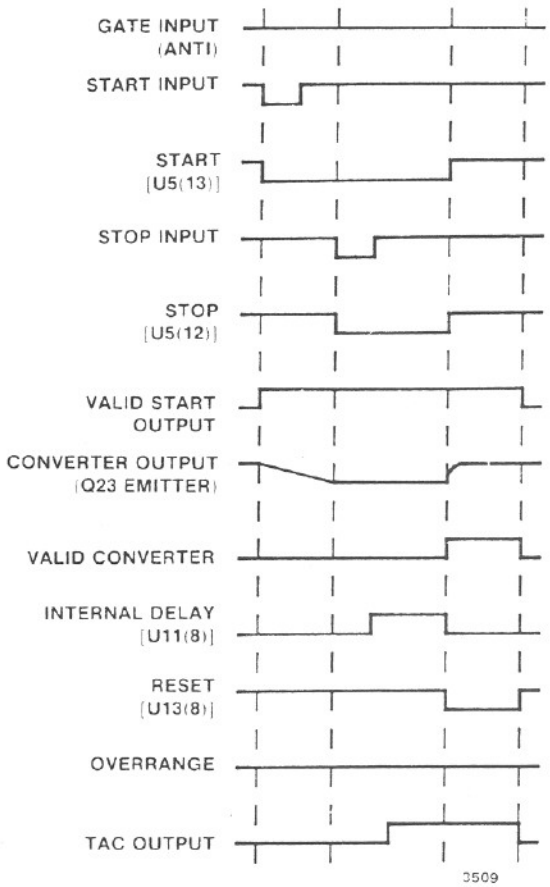
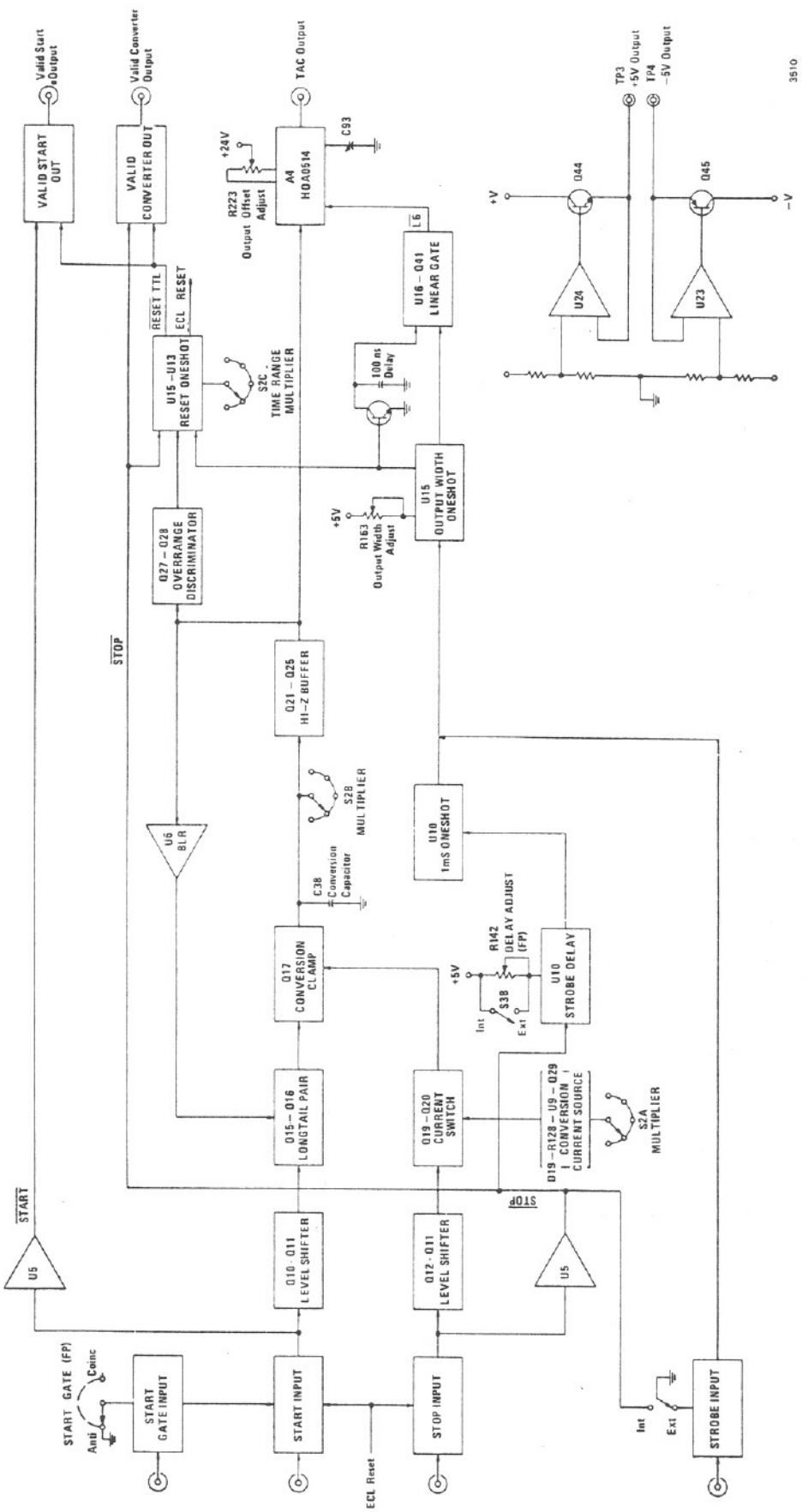


Fig. 6.7.

6.4. FACTORY REPAIR

This instrument can be returned to the EG&G ORTEC factory for service and repair at a nominal cost. Our standard procedure for repair ensures the same quality control and checkout that are used for a new instrument. Always contact the Customer Service Department at EG&G ORTEC, (615) 482-4411, before sending in an instrument for repair to obtain shipping instructions and so that the required Return Authorization Number can be assigned to the unit. Write this number on the address label and on the package to ensure prompt attention when it reaches the EG&G ORTEC factory.



Block diagram of Model 566 Time-to-Amplitude Converter.

BIN/MODULE CONNECTOR PIN ASSIGNMENTS FOR STANDARD NUCLEAR INSTRUMENT MODULES PER DOE/ER-0457T

Pin	Function	Pin	Function
1	+3 volts	23	Reserved
2	-3 volts	24	Reserved
3	Spare Bus	25	Reserved
4	Reserved Bus	26	Spare
5	Coaxial	27	Spare
6	Coaxial	*28	+24 volts
7	Coaxial	*29	-24 volts
8	200 volts dc	30	Spare Bus
9	Spare	31	Spare
*10	+6 volts	32	Spare
*11	-6 volts	*33	117 volts ac (Hot)
12	Reserved Bus	*34	Power Return Ground
13	Spare	35	Reset (Scaler)
14	Spare	36	Gate
15	Reserved	37	Reset (Auxiliary)
*16	+12 volts	38	Coaxial
*17	-12 volts	39	Coaxial
18	Spare Bus	40	Coaxial
19	Reserved Bus	*41	117 volts ac (Neut.)
20	Spare	*42	High Quality Ground
21	Spare	G	Ground Guide Pin
22	Reserved		

Pins marked (*) are installed and wired in EG&G ORTEC's 4001A and 4001C Modular System Bins.