CF 8000

OCTAL CONSTANT FRACTION DISCRIMINATOR

10/86

EG&G-ESN

CF 8000

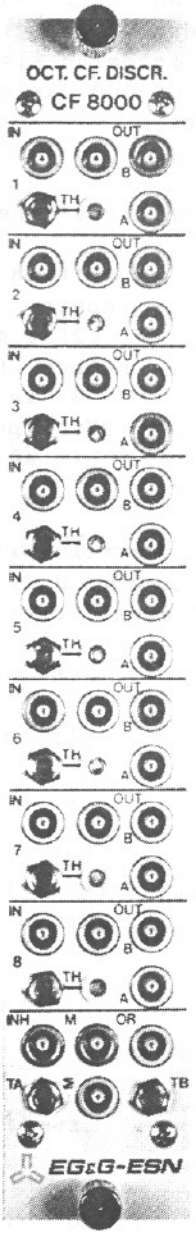
OCTAL CONSTANT FRACTION DISCRIMINATOR

FEATURES:

* 8 independent CFD channels
* Automatic walk adjustment
* Multiplicity output
* OR logic output
* Analog sum output
* Inhibit input
* ECL Outputs
* Energy Outputs
* Internal delay

APPLICATIONS:

* High-density timing experiments
* PMT or solid-state detectors
* Time-of-flight measurements



The powerful Model CF8000 Octal Constant Fraction Discriminator has the performance and features necessary for even the most demanding experiments. It contains 8 constant fraction discriminators in a single-width NIM module.

Exclusive features of the Model CF8000 include internal shaping delay, automatic walk adjustment, an analog summation output, and built-in logic functions to minimize external logic requirements.

The input signals can range from 0 to -5 V. Each input has a separate threshold adjustment, with front-panel monitor, which may range from -10 mV to -1 V.

For each channel there are 3 Fast NIM logic outputs - 1- "A" and 2- "B" outputs. The "A" output is an updating output with adjustable deadtime. There is a single deadtime adjustment for all 8 "A" outputs, and a single width adjustment for all 16 "B" logic outputs. There are also 8 rear-panel ECL outputs which have the same width as the "B" outputs.

Each channel has a rear-panel "E" output which buffers the input signal.

External delay cables are not necessary on the Model CF8000. Each channel has an internal shaping-delay circuit which can be set for 2, 4, 6, 8, or 10 ns. Optional delay line plug-ins are available for shaping delay ranges of 5 ns, 30 ns, or 50 ns. For all delay plug-in there are 5 possible delay settings. (See accessories section.)

The automatic walk adjustment of the CF8000 not only saves the trouble of experimental set-up, it also reduces the effects of ground-loop input noise on the incoming signal. Compared to other models with manual walk adjustments, the CF8000 can give better timing resolution in cases where ground loops are a problem.

Other front-panel connections include :

1) an analog sum output (Σ), which provides an attenuated summation of all inputs,
2) a multiplicity output (M), which provides a voltage proportional to the number of valid "B" outputs,
3) an OR logic output, which provides a logic output for every active "B" output, and
4) an inhibit input (INH), which disables all "B" outputs.

The constant fraction ratio is set by a plug-in hybrid circuit. The factory setting is 0.2. The hybrid modules can easily be changed on each channel for different fractions or functions.

The following special hybrids may be ordered:

1) constant fraction of 0.4,

2) leading edge·discriminator hybrid, and

3) zero-crossing discriminator hybrid.

(Please refer to accessories section.)

1. INTRODUCTION

Constant fraction timing makes use of the knowledge that, for a given pulse shape from a detector/preamplifier combination, there is an optimum triggering or discrimination to minimize walk. This optimum fraction varies for pulses of different risetimes; but for pulses of constant risetime, it does exist.

The technique operates by inverting and attenuating the pulse from which a time signal is to be derived and adding it back to the delayed (non-inverted, non-attenuated) signal itself. Fig. 1 illustrates this process.

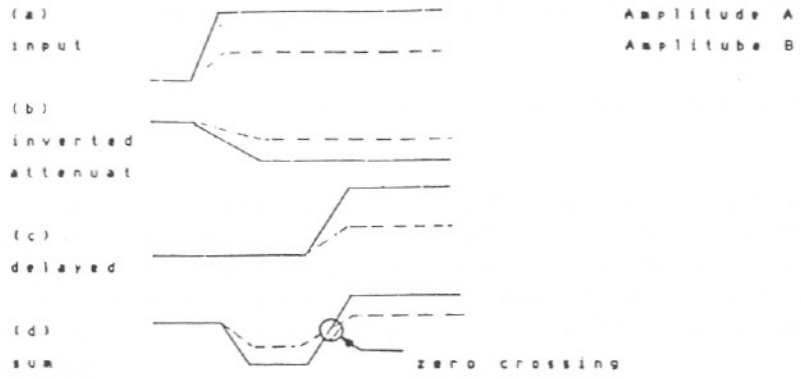


Fig. 1. Constant fraction pulse shaping

This technique essentially eliminates the "walk" errors caused by signals of constant risetime, but varying amplitudes.

The technique described above does not compensate for detector risetime variation. See fig. 2 which illustrates the result with two pulses of equal amplitude, but varying risetime.

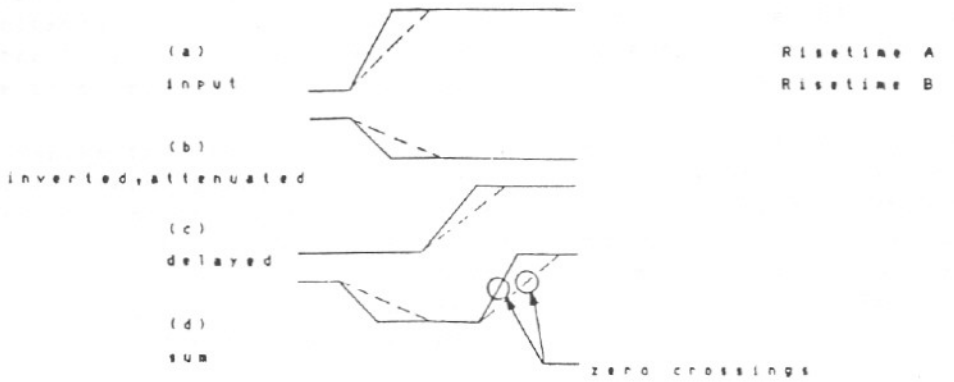


Fig. 2. Constant fraction pulse shaping with varying risetimes.

To compensate for varying risetimes requires a further elaboration of the timing system. The elaboration is to modify the delay time of the non-attenuated, non-inverted signal shown in fig. 1(c) to a value less than the shortest risetime that will be encountered. Fig. 3 illustrates the result for two signals of the same amplitude, but differing risetimes, when the delay is set to less than this critical value.

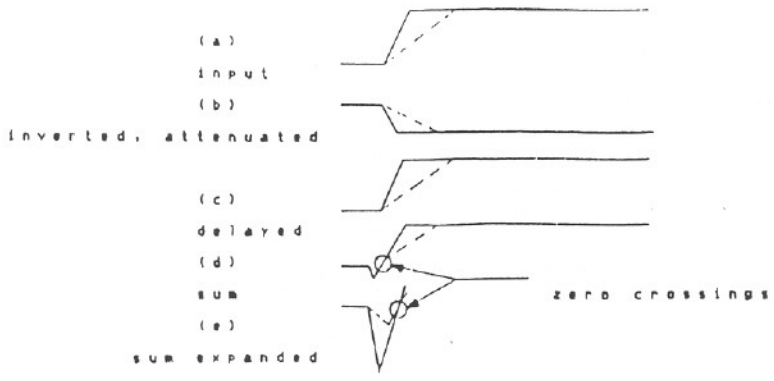


Fig. 3. Pulse shaping for constant fraction timing with risetime compensation.

Use of this technique does require that certain restrictions upon minimum and maximum signal inputs must be observed.

Constant fraction timing yields greatly improved time resolution with large Ge(Li) detectors. As an example, one detector timing curve, as measured by the FWHM of the time peak width for known coincident events, was reduced from 6.3ns to 4.2ns by using constant fraction timing instead of leading edge timing with a very low energy acceptance range. The improvement is much greater for wide energy range.

2. PRINCIPLES OF OPERATION

The input pulse (labeled c_1 in fig. 4) is split into two parts. One part (labeled A in fig. 4) is attenuated and applied to the inverting input of a fast differential discriminator. The other part (labeled B in fig. 4) is delayed and then applied to the non-inverting input of the same discriminator.

The output voltage of this discriminator is determined by the difference of the input voltages. This pulse (labeled AB in fig. 4) crosses the threshold voltage of the following gate at V_{BB}*, if the voltages at the inputs are equal. From this crossing the timing information is derived.

In order to derive the timing information from a fraction of the maximum amplitude of the input pulse, the timing has to be done at the time of occurrence of this maximum i.e. one has to wait with the timing until the maximum amplitude is known. Thus one has the condition that the maximum of the attenuated pulse - which corresponds to the maximum of the input pulse - has to cross the delayed pulse at the particular selected fraction. This condition leads immediately to the following relation: -

$$t_{delay} = t_{rise}(1 - \text{fraction})$$

using the idealized pulse shapes of fig. 4.

The validity of the approximations made by assuming such idealized pulse shapes has been checked for various values of fraction and the delay time.

*Nominally, $V_H = -0.8V$, $V_{BB} = -1.2V$, $V_L = -1.8V$, see also the data sheets.

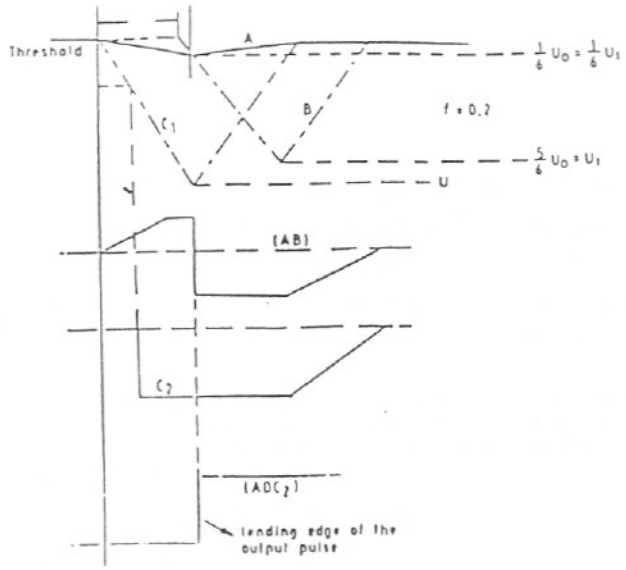


Fig. 4. Pulse shapes at the specified points in the electronic circuit of fig. 5 The propagation delays of the I.C's are not included in order to display the time resolutions more clearly.

He have varied indepently the fraction from 0.1 to 0.5 and the ratio of the delay time to the risetime from 0.4 to 1.0 He found that the time resolution remains essentially constant for fractions betHeen 0.1 & 0.3 For higher fraction (e.g. f = 0.5) the resolution deteriorates someHhat.

The variation of the delay time does not affect time resolution, as long as it satisfied the given relation Hithin a factor of 2. This seems plausible, since the actual pulse shape is not as pointed as our idealization, but varies more smoothly Hith time.

3. TIMING DISCRIMINATOR

This circuit is fulfilled by applying ECL integrated circuits Hith a propogation delay of 4ns.

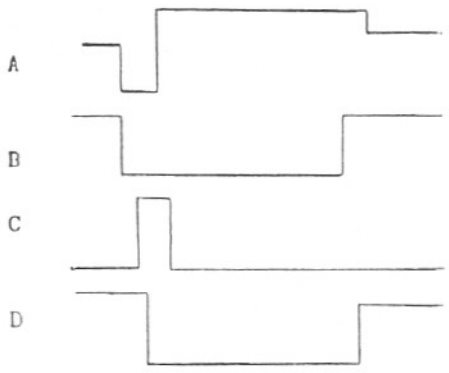


Fig. 6. Timing diagram of the timing discriminator pulses.

A - signal after the main differential amplifier tract.
B - signal at output of leading edge discriminator.
C - signal from the coincidence gate.
D - signal from the RS-trigger.

Fig. 6 explains the principle of the timing discriminator operation. The differential amplifier in the main stage of the timing discriminator shapes a bi-polar signal from the input signal as already described. Thus, uniform logic signal (A) Hill be formed at the output due to the high amplification (10^3) and the limitation.

Performance of the GSI Constant Fraction Discriminators CF4000 and CF8000

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Since 1980 constant fraction discriminators (CFD) have been built at GSI, following the design of M.M. Maier, Marburg-LBL-Berkeley. The number of channels built has been doubled every year resulting in more than 1000 channles in 1983. In 1982, the new 8-channel version with internal delay hybrids, gated baseline restores, inhibit input, and outputs for energy, time (ECL), common multiplicity, sum-energy, and logical OR was produced first for the GSI/LBL Plastic-Ball collaboration. This CF8000 has become available for experiments at the UNILAC in 1983 and has been added to the GSI NIM-pool. During the GSI student program, intensive tests had been made with constant fraction discriminators.

The purpose of a discriminator in nuclear electronics is to produce a standard output signal from an analog input signal to define the time of an event. The constant fraction discriminator gives an output signal at a fixed delay after a constant fraction of the pulse's rise-time. This guarantees good time informations for pulses of constant shapes within a wide range of amplitudes.

For the measurement of the delay as a function of the dynamic range of input signals, a pulser signal has been fed into the CFD via a variable attenuator. The CFD time output stopped a time-to-amplitude converter (TAC) that was started by a reference signal. The time differences have been measured using a multi-channel analyzer (MCA). The delay of the attenuator has been taken into account. The correction factors have been determined by measuring the phase differences at different attenuation factors at 200 MHz with a vector voltmeter. The systematic errors of this correction have been ±8.5 ps. Fig. 1 shows the delay as a function of the amplitude of the input signal (log-scale) for different constant fraction discriminators. The test pulses have had a rise-time of 5 ns and a decay-time of 15 ns. The walk adjustments for the CF4000, TC 454, and ORTEC 934 have been done by optimizing the performance curves. The resulting walk has been about 2 mV more positive than the well known equal brightness recipe for CF4000 and TC 454. The bigger shift of the CF8000 is due to the symmetric walk adjust, done by the automatic baseline restorer instead of the better asymmetric adjust.

Fig. 2 shows the performance of the CFDs at a faster rise-time of the test pulses. The large time shift at high pulse amplitudes for CF4000, CF8000, and TC 454 are a property of the fast discriminator-IC SP9687, used in these modules. The ORTEC 934 using the older AM687 IC does not show that behavior. An improvement of the rise at large amplitudes might be possible, using the already announced new IC AM9687.

For longer decay time pulses the delay of the CFD is rather insensitive as soon as it is long enough (0.8 - 1.0 times the rise time). The coarse setting of the delay possible in the CF8000 is thus sufficient. The threshold setting has no influence on the performance above the threshold.

The temperature stability of the CF4000 has been measured to be less than 3 ps/°C. Due to reduce the power consumption by the circuit design, the count rate capability is not higher than 15 MHz for the CF4000 and 40 MHz for the CF8000 depending on the dead time setting. There is no decline of the performance with increasing count rate.

For a 5 V input signal there is no triggering of other channels as long as the threshold is higher than 3-4 mV for both the CF4000 and the CF8000.

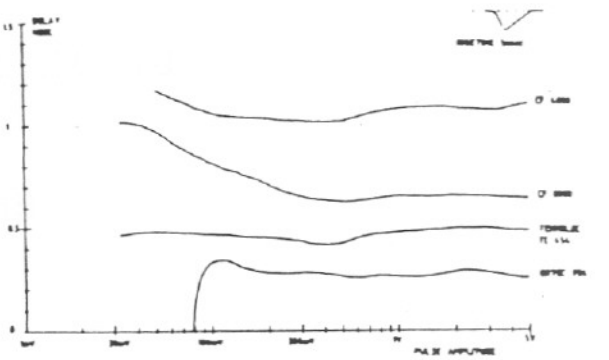


Fig. 1: Delay as a function of the amplitude of the input signal for differnet constant fraction discriminators. CF4000: fraction f=0.25, delay t=5 ns (1 m), threshold u=10 mV; CF8000: f=0.4, t=6 ns, u=10 mV, TC 454: f=0.2, t=5 ns (1 m), u=30 mV, 1.2 internal attenuation; ORTEC 934: f=0.2, t=5 ns (1 m), u=30 mV.

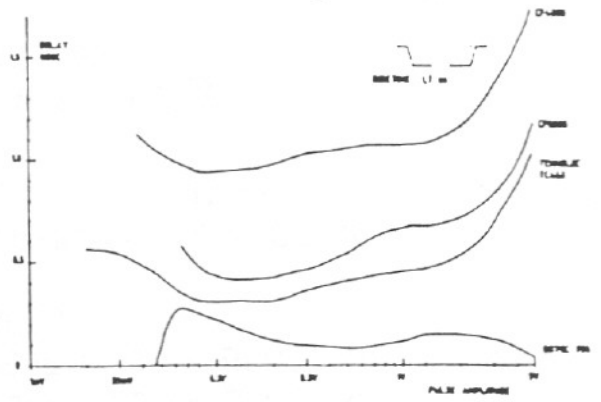
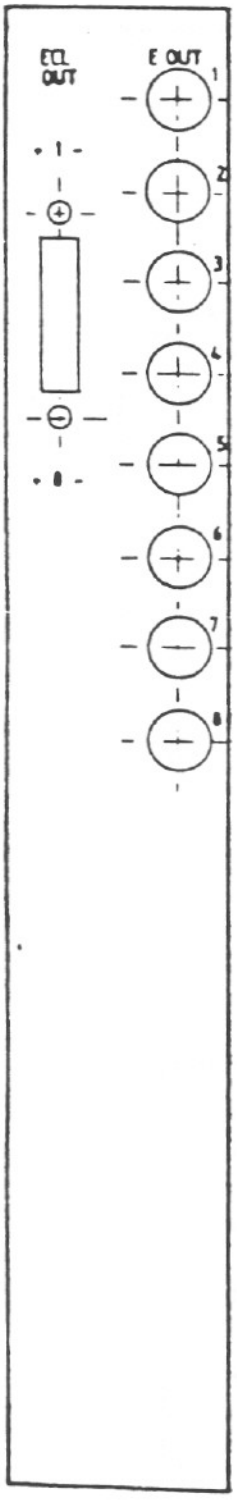


Fig. 2: Same as Fig. 1 besides rise time of input signal is now 1.7 ns.

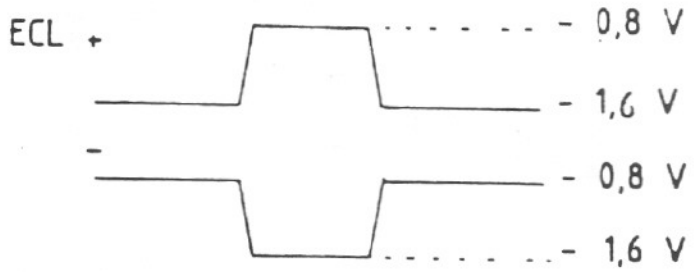
CF 8000

(REAR PANEL)



ANALOG OUT (AC COUPLED)

OUT B ; WIDTH= TB

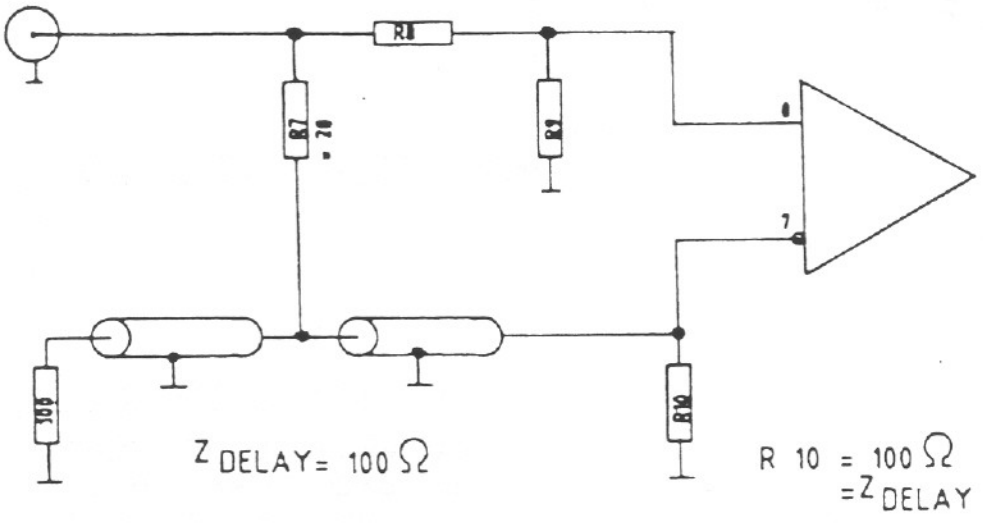


DIFFERENTIAL LINE
LINE IMPEDANCE : 112. Ω

DELAY TIME : 2,4, ... 10 ns
USING 10 ns HYBRID DELAY PLUG IN
bestücken
AVAILABLE ALSO :
6,12, ... 30ns (30 ns PLUG IN)
10,20,..... 50ns (50 ns PLUG IN)

CF 8000

SELECTING FRACTION



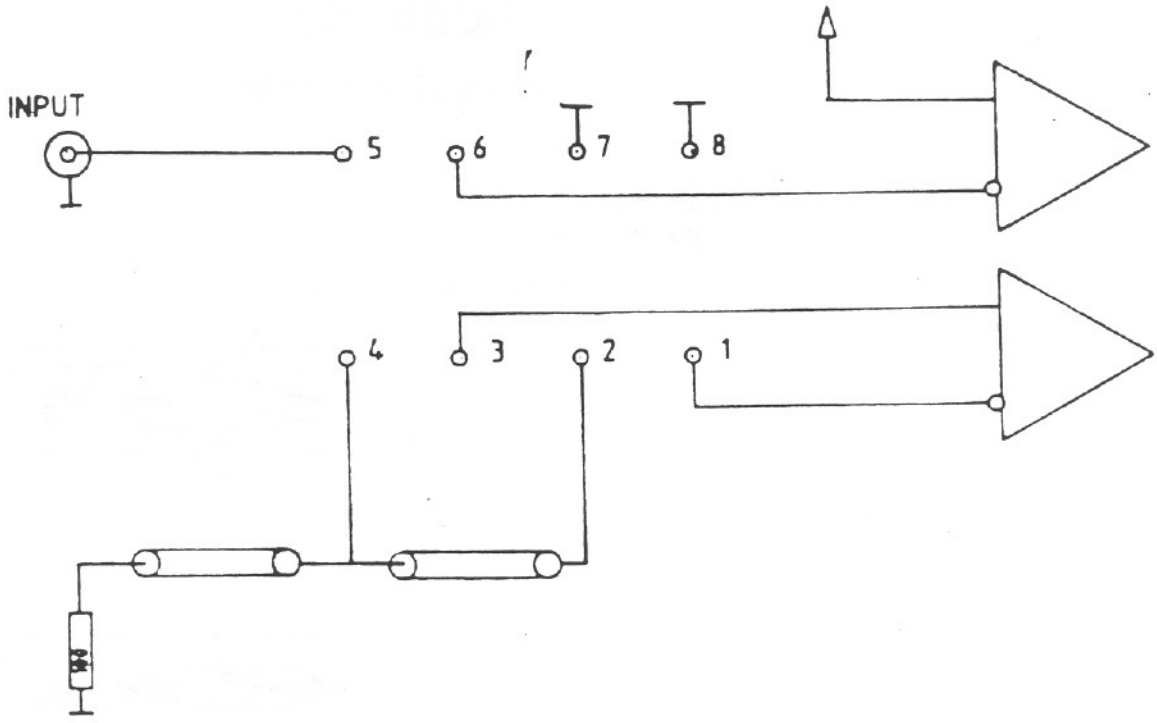
1.) $70\,\Omega \,||\, (R8 + R9) = 50\,\Omega$

$R8 + R9 = 175\,\Omega$

2.) $R9 = 175\,\Omega \cdot \frac{50\,\Omega}{70\,\Omega} \cdot f = 125 \times f$

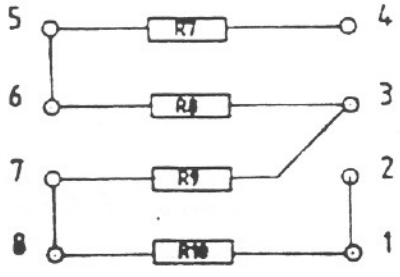
$R8 = 175 - R9$

		f = 0,2	f = 0,4
R7 =	20 Ω	20 Ω	20 Ω
R8 =	175 Ω - R9	150 Ω	125 Ω
R9 =	125 Ω x f	25 Ω	50 Ω
R10 =	100 Ω	100 Ω	100 Ω



A. TO CHANGE THE FRACTION

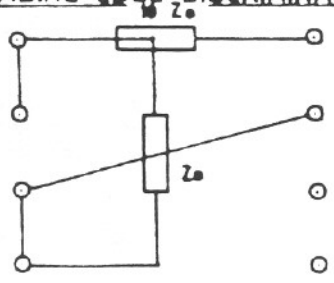
RESISTORS R3 AND R4 HAVE TO BE CHANGED USING THE FOLLOWING RELATION



CF

FRACTION= f
R7 = 20 Ω
R10= 100 Ω
R8 = 175 Ω - R9
R9 = 125 Ω · f

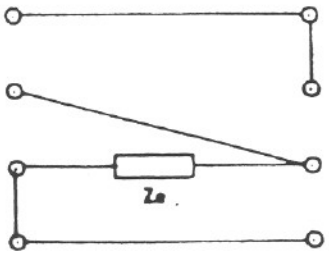
B. USING CF 8000 AS A LEADING EDGE DISCRIMINATOR



LE

Zo = 50 Ω

C. USING CF 8000 AS A ZERO CROSSING DISCRIMINATOR



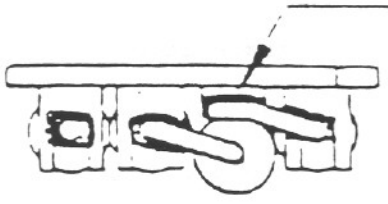
Z/C

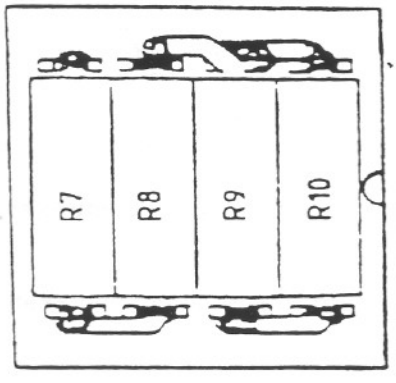
Zo = 50 Ω

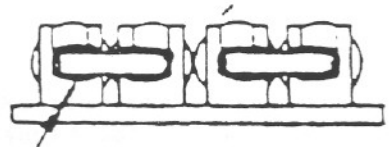
CF 8000

FRACTION PLUG IN

SOLDER RESISTORS
AS SHOWN







SOLDER RESISTORS
AS SHOWN.

DETAIL A

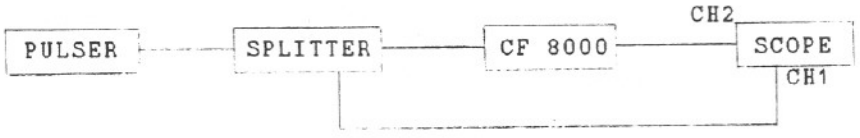
SCALE: 4:1
TYP. 8 PLCS

TEST PROCEDURES FOR CF 8000

1. Test equipment required.

   - NIM bin with ± 6 V
   - Signal generator: 2ns rise time, 200mV amplitude, 30ns width.
   - Oscilloscope
   - ECL test box

   Test setup.



2. Measure current on -6V power line.
   Should be 1.0 A ±10%

   Measure current on +6V power line.
   Should be 250mA ±10%

   Measure current on -12V power line.
   Should be 40mA ±15%

   Measure current on +12V power line.
   Should be 40mA ±15%

3. Monitor the ch.1 front panel test point (white connector) and adjust the threshold pot. (TH) over its full range. The adjustment range should be from 0V to ≥1.0V
Set voltage to 100 mV.

4. Repeat step 3 for all channels.

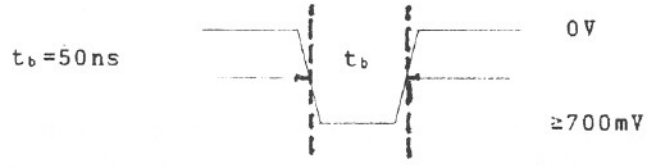
5. Using the pulse generator, input a signal as follows:-

   - 2ns rise time
   - 200mV amplitude
   - 10ns width
   - approx. 1MHz

6. Adjust "TA" potentiometer over full range. Monitor channel 1 output "A". The width of output pulse should vary from 20ns to ≥200ns. Check all "A" outputs for full range of adjustment. Set width to 100ns.

7. Adjust "TB" potentiometer over full range. Monitor channel 1 output "B". The width of output pulse should vary from 20ns to ≥200ns. Check all "B" outputs for full range of adjustment. Set width to 50ns.

N.B. second "B" output must also be terminated with 50 ohm.



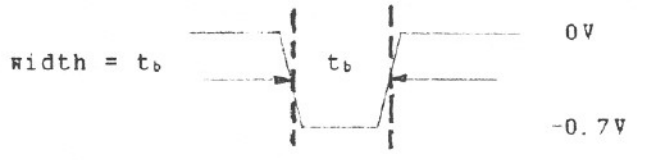
8. Test Σ Out.

Apply test signal to channel 1 input connector. Monitor connector, ensure that cable is terminated with 50 Ohm. The input signal, attenuated 16:1, should be present.
The output signal always represents 1/16 of the accumulated input signals.

9. Continue to monitor the connector whilst applying the input signal to input connectors channels 2 - 8 in turn.

10. Test "OR" out.

Apply test signal to channel 1 input connector. Monitor "OR" output connector. Following signal should be present: -



11. Continue to monitor the "OR" connector whilst applying the input signal to input connectors channels 2 - 8 in turn.

12. Test "M" out.

Apply test signal to channel 1 input connector. Monitor "M" output connector. An attenuated negative signal (100 mV) with width = t_B should be present.

13. Continue to monitor the "M" connector whilst applying the input signal to input connectors channels 2 - 8 in turn.

14. Test "INH" input.

Apply test signal to channel 1 input connector. Output signal should be present at channel 1 "B" output connector.
Apply -0.8V dc level to "INH" connector (e.g. inverted $\overline{OUT}$ O/P from LF 4000). Output signal at "B" should disappear.

15. Repeat step 15 for channels 2 - 8.

16. Test "E" analog signal outputs.

Apply test signal to channel 1 input connector. Monitor channel 1 "E" output on rear panel. Output signal should be 2:1 attenuated input signal.

17. Repeat step 17, applying input signal to the remaining channels 2 - 8 and verifying the "E" outputs 2 - 8.

18. Test of delays.

Apply standard signal to ch.1 input connector and observe the signal at "A" output. Transmission delay of the circuit is delay time between leading edges of input and output signals. Should be 17 ns ±10%.
Repeat for "B" output. delay should be 20 ns ±10%

Repeat for remaining channels.

Apply test signal to channel 1 input connector. Monitor and display both channel 1 input and output signals using oscilloscope. The delay between input and output signals can be observed and varied by changing the position of jumper J1 on jumper block for channel under test.

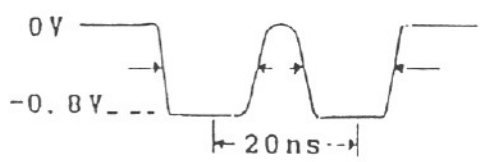
Total delay time of the standard installed delay line is 10 ns. Each jumper position represents a delay step of 2 ns. Absolute accuracy of delay at any jumper setting is 10% of total delay time.

Observe signal on scope and ensure that the total delay variation between first and last jumper positions represents 8 ns, and that each jumper step increases/decreases delay by approx. 2 ns.

19. Repeat step 19 for channels 2 - 8.

20. Pulse Pair Resolution.

Reduce the dead time adjustment pots TA & TB to minimum (fully counter clockwise).
Set pulse generator to double pulse mode.
Generate double pulses of 10 ns width, 1V amplitude.
Gradually reduce the pulse delay whilst observing O/P "B". Note the value of the pulse delay at the point where the "B" output degrades to a single pulse. The double pulse O/P at "B" must be present for values of I/P pulse delay ≥30ns.



21. Repeat step 21 for channels 2 - 8.

22. Minimum Input Pulse Width.

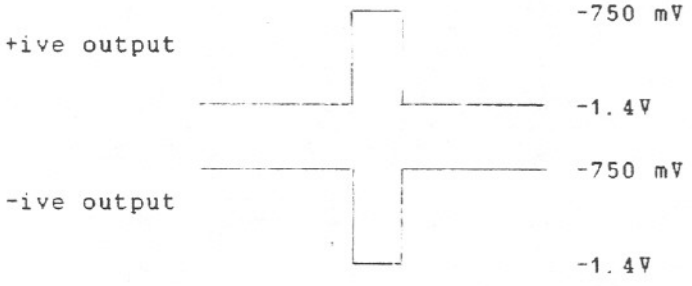
Set pulse generator to normal mode.
Generate pulses of 2 ns width (min. for HP 8082A), 1V amplitude.
Observe O/P "B" for valid output pulses.

N.B. CF 8000 will trigger on input pulse widths down to 1 ns.

23. Repeat step 23 for channels 2 - 8.

24. Test ECL outputs.

Apply test signal to channel 1 input connector. Connect
test box "output" connector to ECL connector on rear panel.
Set test box "output" rotary switch to channel 1 and monitor and display
complementary ECL output signals from test box.
Adjust "TB" potentiometer on front panel over full range and verify that ECL
signal width varies between 20 - 200ns.



25.
Repeat step 21 for channels 2 - 8, applying test pulse to each channel in
turn and advancing test box rotary switch to correspond to input channel
number.

!!IMPORTANT!!

26. Apply test signal to channel 1 input connector, monitor output connector
"B" and re-adjust potentiometer "TB" for output pulse width of 50ns.