1.14
VIC068A Signal List and Pinouts

Table 1-17. VMEbus Signals

Name	PGA Pin	QFP Pin	Type	Description
D07	H15	99	Three-State I/O	VMEbus Data
D06	H14	98	Three-State I/O	VMEbus Data
D05	J15	97	Three-State I/O	VMEbus Data
D04	K15	96	Three-State I/O	VMEbus Data
D03	J14	94	Three-State I/O	VMEbus Data
D02	L15	93	Three-State I/O	VMEbus Data
D01	K14	92	Three-State I/O	VMEbus Data
D00	K13	91	Three-State I/O	VMEbus Data
A07	N2	33	Three-State I/O	VMEbus Address
A06	L3	32	Three-State I/O	VMEbus Address
A05	M2	31	Three-State I/O	VMEbus Address
A04	M1	29	Three-State I/O	VMEbus Address
A03	L2	28	Three-State I/O	VMEbus Address
A02	L1	27	Three-State I/O	VMEbus Address
A01	K2	25	Three-State I/O	VMEbus Address
AM5	R10	63	Three-State I/O	VMEbus Address Modifier
AM4	R9	62	Three-State I/O	VMEbus Address Modifier
AM3	R8	59	Three-State I/O	VMEbus Address Modifier
AM2	P8	58	Three-State I/O	VMEbus Address Modifier
AM1	R7	57	Three-State I/O	VMEbus Address Modifier
AM0	R6	56	Three-State I/O	VMEbus Address Modifier
BG3IN*	N14	84	Input	VMEbus Bus Grant Input
BG3OUT*	M15	90	Output	VMEbus Bus Grant Output
BG2IN*	M13	83	Input	VMEbus Bus Grant Input
BG2OUT*	N15	88	Output	VMEbus Bus Grant Output
BG1IN*	P14	77	Input	VMEbus Bus Grant Input
BG1OUT*	L13	87	Output	VMEbus Bus Grant Output
BG0IN*	N13	76	Input	VMEbus Bus Grant Input
BG0OUT*	M14	86	Output	VMEbus Bus Grant Output

Table 1-17. VMEbus Signals (continued)

Name	PGA Pin	QFP Pin	Type	Description
BR3*	P13	73	Open Collector I/O	VMEbus Request
BR2*	N11	72	Open Collector I/O	VMEbus Request
BR1*	P12	71	Open Collector I/O	VMEbus Request
BR0*	R12	69	Open Collector I/O	VMEbus Request
IACK*	P6	52	Rescinding Three-State I/O	VMEbus Interrupt Acknowledge
IACKIN*	N6	51	Input	VMEbus Interrupt Acknowledge Input
IACKOUT*	R4	50	Output	VMEbus Interrupt Acknowledge Output
IRQ7*	R2	45	Open Collector I/O	VMEbus Interrupt Request
IRQ6*	P3	44	Open Collector I/O	VMEbus Interrupt Request
IRQ5*	N4	43	Open Collector I/O	VMEbus Interrupt Request
IRQ4*	R1	38	Open Collector I/O	VMEbus Interrupt Request
IRQ3*	P2	37	Open Collector I/O	VMEbus Interrupt Request
IRQ2*	N3	36	Open Collector I/O	VMEbus Interrupt Request
IRQ1*	M3	35	Open Collector I/O	VMEbus Interrupt Request
BBSY*	N12	75	Rescinding Three-State I/O	VMEbus Busy
BCLR*	R14	74	Three-State I/O	VMEbus Clear
AS*	P7	54	Rescinding Three-State I/O	VMEbus Address Strobe
DS1*	P11	68	Rescinding Three-State I/O	VMEbus DataStrobe
DS0*	R11	67	Rescinding Three-State I/O	VMEbus Data Strobe
DTACK*	R5	53	Rescinding Three-State I/O	VMEbus Data Transfer Acknowledge
BERR*	N10	66	Rescinding Three-State I/O	VMEbus Error
LWORD*	P9	64	Rescinding Three-State I/O	VMEbus Long-Word
WRITE*	P10	65	Rescinding Three-State I/O	VMEbus Data Direction
SYSCLK*	P15	85	Three-State Output	VMEbus Syatem Clock
SYSRESET*	P5	49	Open Collector I/O	VMEbus System Reset
ACFAIL*	R3	48	Input	VMEbus AC Fail
SYSFAIL*	N5	47	Open Collector I/O	VMEbus System Fail

Table 1-18. Local Signals

Name	PGA Pin	QFP Pin	Type	Description
LD7	C4	155	Three-State I/O	Local Data
LD6	A2	154	Three-State I/O	Local Data
LD5	B3	153	Three-State I/O	Local Data
LD4	C5	152	Three-State I/O	Local Data
LD3	B4	151	Three-State I/O	Local Data
LD2	A3	150	Three-State I/O	Local Data
LD1	A4	149	Three-State I/O	Local Data
LD0	B5	148	Three-State I/O	Local Data
LA7	A5	147	Three-State I/O	Local Address
LA6	C6	146	Three-State I/O	Local Address
LA5	B6	145	Three-State I/O	Local Address
LA4	B7	144	Three-State I/O	Local Address
LA3	A6	143	Three-State I/O	Local Address
LA2	A7	142	Three-State I/O	Local Address
LA1	A8	139	Three-State I/O	Local Address
LA0	B8	138	Three-State I/O	Local Address
SCON*	C13	116	Input	System Controller Enable
IRESET*	B14	117	Input	Internal Reset Input
RESET*	C10	131	Open Collector Output	Reset Output
HALT*	A12	130	Open Collector I/O	Halt Status
CLK64M	D13	115	Input	64-MHz Clock Input
PAS*	A10	136	Rescinding Three-State I/O	Physical/Processor Address Strobe
DS*	C9	135	Rescinding Three-State I/O	Processor Data Strobe
DSACK1*	B9	134	Three-State I/O	Data Size Acknowledge 1
DSACK0*	A11	133	Three-State I/O	Data Size Acknowledge 0
LBERR*	B10	132	Rescinding Three-State I/O	Local Bus Error
R/W*	B11	129	Rescinding Three-State I/O	Local Data Direction
RMC*	B12	126	Input	Read-Modify-Write
CS*	A9	137	Input	VIC068A Chip (Register) Select
SIZ1	A14	125	Rescinding Three-State I/O	Data Transfer Size 1
SIZ0	B13	124	Rescinding Three-State I/O	Data Transfer Size 0
FC2	A13	128	Rescinding Three-State I/O	Function Code 2
FC1	C11	127	Rescinding Three-State I/O	Function Code 1
LBG*	A15	118	Input	Local Bus Grant
LBR*	C12	123	Output	Local Bus Request

Table 1-18. Local Signals (continued)

Name	PGA Pin	QFP Pin	Type	Description
IPL2	B1	5	Output	Interrupt Priority Level 2
IPL1	C2	4	Output	Interrupt Priority Level 1
IPL0	D3	3	Three-State I/O	Interrupt Priority Level 0/Global Reset
BLT*	B2	157	Open Collector I/O	Block Transfer Status
DEDLK*	C3	156	Output	Deadlock Status
LIACKO*	C1	8	Output	Local Interrupt Autovector
LIRQ7*	G3	15	Input	Local Interrupt Request 7
LIRQ6*	G2	14	Input	Local Interrupt Request 6
LIRQ5*	E1	13	Input	Local Interrupt Request 5
LIRQ4*	F2	12	Input	Local Interrupt Request 4
LIRQ3*	F3	11	Input	Local Interrupt Request 3
LIRQ2*	D1	10	Three-State I/O (w/PU)	Local Interrupt Request 2
LIRQ1*	E2	9	Input	Local Interrupt Request 1
MWB*	J2	24	Input	Module Wants Bus
FCIACK*	K1	23	Input	Interrupt Acknowledge
WORD*	J1	22	Input	D16/D32 Control
SLSEL1*	H1	19	Input	Slave Select 1
SLSEL0*	J3	21	Input	Slave Select 0
ICFSEL*	H2	18	Input	ICF Select
ASIZ1	F1	16	Input	Address Size 1
ASIZ0	G1	17	Input	Address Size 0

Table 1-19. Buffer Control Signals

Name	PGA Pin	QFP Pin	Type	Description
ABEN*	B15	114	Output	VMEbus Address Buffer Enable
LADO	C14	113	Output	Latch Outgoing VMEbus Address
LADI	E13	112	Output	Latch Incomming VMEbus Address
LEDO	D15	109	Output	Latch Outgoing VMEbus Data
LEDI	D14	111	Output	Latch Incomming VMEbus Data
DDIR	E14	108	Output	Local Data Direction
DENIN1*	E15	107	Output	Local Data Enable In (Upper Word)
DENIN*	F14	105	Output	Local Data Enable In (Lower Word)
SWDEN*	F15	103	Output	Swap Local Data Enable
DENO*	G14	104	Output	VMEbus Data Buffer Enable
ISOBE*	G15	102	Output	Isolation Buffer Enable
LAEN	E3	7	Output	Local Address Buffer Enable

Table 1-20. Power Supplies[1]

Name	PGA Pin	Type	Description
V_{SS} Core	H3	Ground	Ground
V_{SS}	K3	Ground	Ground
V_{SS}	P1	Ground	Ground
V_{SS}	N7	Ground	Ground
V_{SS}	N8	Ground	Ground
V_{SS}	R13	Ground	Ground
V_{SS}	R15	Ground	Ground
V_{SS}	L14	Ground	Ground
V_{SS}	H13	Ground	Ground
V_{SS}	F13	Ground	Ground
V_{SS}	C7	Ground	Ground
V_{SS}	A1	Ground	Ground
V_{CC} Core	G13	Power	+5 Volts DC
V_{CC}	D2	Power	+5 Volts DC
V_{CC}	N1	Power	+5 Volts DC
V_{CC}	P4	Power	+5 Volts DC
V_{CC}	N9	Power	+5 Volts DC
V_{CC}	J13	Power	+5 Volts DC
V_{CC}	C15	Power	+5 Volts DC
V_{CC}	C8	Power	+5 Volts DC

Note:

1. For QFP power supply signals, see *Table 1-21*.

Table 1-21. Pinout for VIC068A Plastic and Ceramic Quad Flatpack (160-Pin): Cavity Up

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V_{SS}	32	A06	63	AM5	94	D03
2	V_{SS}	33	A07	64	LWORD*	95	V_{DD}
3	IPL0	34	V_{SS}	65	WRITE*	96	D04
4	IPL1	35	IRQ1*	66	BERR*	97	D05
5	IPL2	36	IRQ2*	67	DS0*	98	D06
6	V_{DD}	37	IRQ3*	68	DS1*	99	D07
7	LAEN	38	IRQ4*	69	BR0*	100	V_{SS}
8	LIACKO*	39	V_{SS}	70	V_{SS}	101	V_{DD} CORE
9	LIRQ1*	40	V_{SS}	71	BR1*	102	ISOBE*
10	LIRQ2*	41	V_{DD}	72	BR2*	103	SWDEN*
11	LIRQ3*	42	V_{DD}	73	BR3*	104	DENO*
12	LIRQ4*	43	IRQ5*	74	BCLR*	105	DENIN*
13	LIRQ5*	44	IRQ6*	75	BBSY*	106	V_{SS}
14	LIRQ6*	45	IRQ7*	76	BGIN0*	107	DENIN1*
15	LIRQ7*	46	V_{DD}	77	BGIN1*	108	DDIR
16	ASIZ1	47	SYSFAIL*	78	V_{SS}	109	LEDO
17	ASIZ0	48	ACFAIL*	79	V_{DD}	110	V_{DD}
18	ICFSEL*	49	SYSRESET*	80	V_{DD}	111	LEDI
19	SLSEL1*	50	IACKOUT*	81	V_{SS}	112	LADI
20	V_{SS} CORE	51	IACKIN*	82	V_{SS}	113	LADO
21	SLSEL0*	52	IACK*	83	BGIN2*	114	ABEN*
22	WORD*	53	DTACK*	84	BGIN3*	115	CLK64M
23	FCIACK*	54	AS*	85	SYSCLK	116	SCON*
24	MWB*	55	V_{SS}	86	BGOUT0*	117	IRESET*
25	A01	56	AM0	87	BGOUT1*	118	LBG*
26	V_{SS}	57	AM1	88	BGOUT2*	119	V_{SS}
27	A02	58	AM2	89	V_{SS}	120	V_{SS}
28	A03	59	AM3	90	BGOUT3*	121	V_{DD}
29	A04	60	V_{SS}	91	D00	122	V_{DD}
30	V_{DD}	61	V_{DD}	92	D01	123	LBR*
31	A05	62	AM4	93	D02	124	SIZ0
125	SIZ1	134	DSACK1*	143	LA3	152	LD4

Table 1-21. Pinout for VIC068A Plastic and Ceramic Quad Flatpack (160-Pin): Cavity Up (continued)

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
126	RMC*	135	DS*	144	LA4	153	LD5
127	FC1	136	PAS*	145	LA5	154	LD6
128	FC2	137	CS*	146	LA6	155	LD7
129	R/W*	138	LA0	147	LA7	156	DEDLK*
130	HALT*	139	LA1	148	LD0	157	BLT*
131	RESET*	140	V_{DD}	149	LD1	158	V_{SS}
132	LBERR*	141	V_{SS}	150	LD2	159	V_{DD}
133	DSACK0*	142	LA2	151	LD3	160	V_{DD}

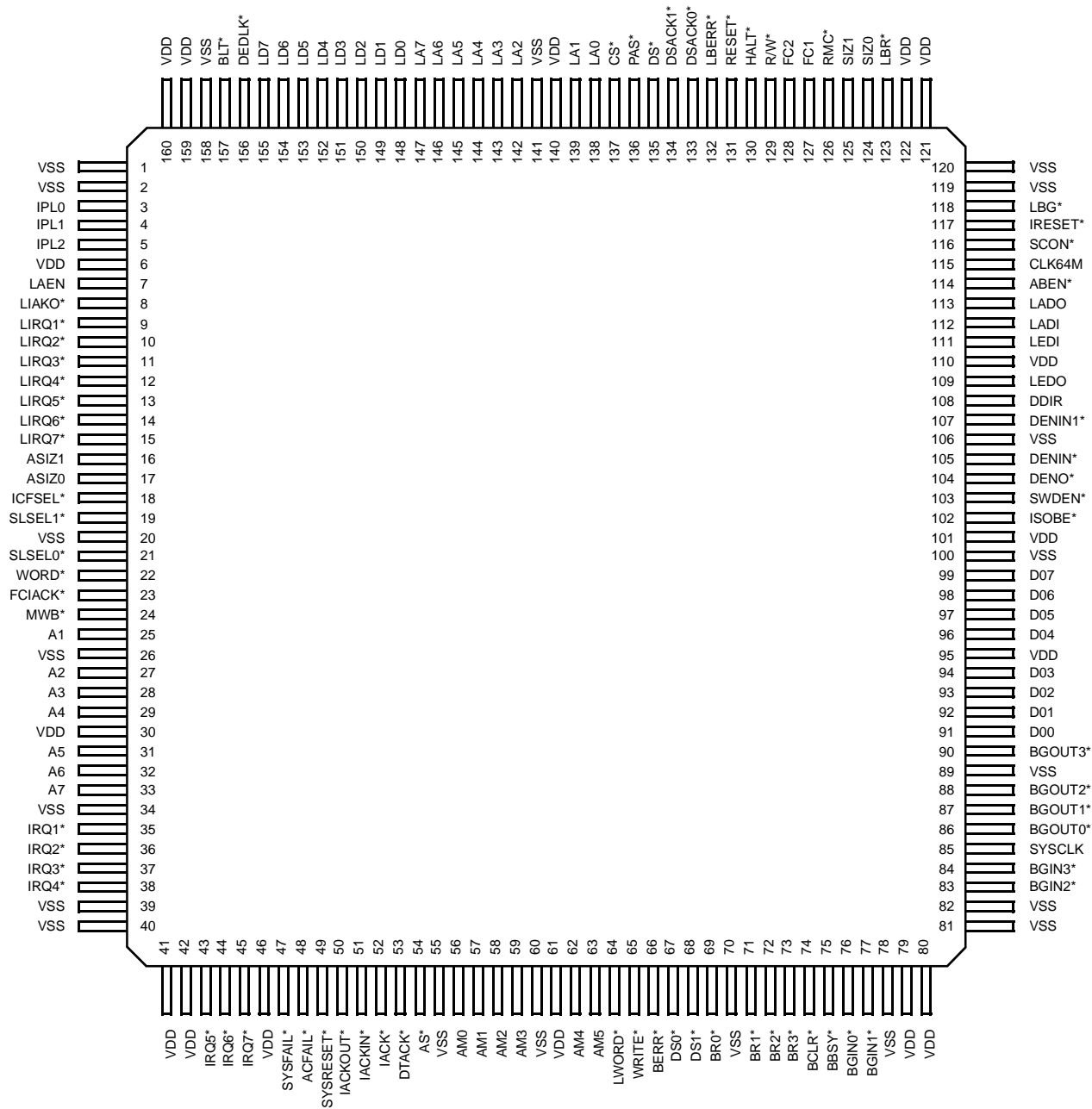|	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	
1	VSS	IPL2	LIACKO*	LIRQ2*	LIRQ5*	ASIZ1	ASIZ0	SLSEL1*	WORD*	FCIACK*	A02	A04	VDD	VSS	IRQ4*	1
2	LD6	BLT*	IPL1	VDD	LIRQ1*	LIRQ4*	LIRQ6*	ICFSEL*	MWB*	A01	A03	A05	A07	IRQ3*	IRQ7*	2
3	LD2	LD5	DEDLK*	IPL0	LAEN	LIRQ3*	LIRQ7*	VSS	SLSEL0*	VSS	A06	IRQ1*	IRQ2*	IRQ6*	ACFAIL*	3
4	LD1	LD3	LD7	LOCATOR PIN									IRQ5*	VDD	IACKOUT*	4
5	LA7	LD0	LD4										SYSFAIL*	SYSRESET*	DTACK*	5
6	LA3	LA5	LA6										IACKIN*	IACK*	AM0	6
7	LA2	LA4	VSS										VSS	AS*	AM1	7
8	LA1	LA0	VCC7										VSS	AM2	AM3	8
9	CS*	DSACK1*	DS*										VDD	LWORD*	AM4	9
10	PAS*	LBERR*	RESET*										BERR*	WRITE*	AM5	10
11	DSACK0*	R/W*	FC1										BR2*	DS1*	DS0*	11
12	HALT*	RMC*	LBR*										BBSY*	BR1*	BR0*	12
13	FC2	SIZ0	SCON*	CLK64M	LADI	VSS	VDD	VSS8	VCC5	D00	BG1OUT*	BG2IN*	BG0IN*	BR3*	VSS	13
14	SIZ1	IRESET*	LADO	LEDI	DDIR	DENIN*	DENO*	D06	D03	D01	VSS7	BG0OUT*	BG3IN*	BG1IN*	BCLR*	14
15	LBG*	ABEN*	VDD	LEDO	DENIN1*	SWDEN*	ISOBE*	D07	D05	D04	D02	BG3OUT*	BG2OUT*	SYSCLK	VSS	15

Figure 1-48. VIC068A Pin Grid Array (PGA), Bottom View

Figure 1-49. VIC068A Quad Flatpack (QFP), Top View