1.15

VIC068A Simulation Waveforms

Note: LWDENIN* is now called DENIN* and UWDENIN* is now called DENIN1*.

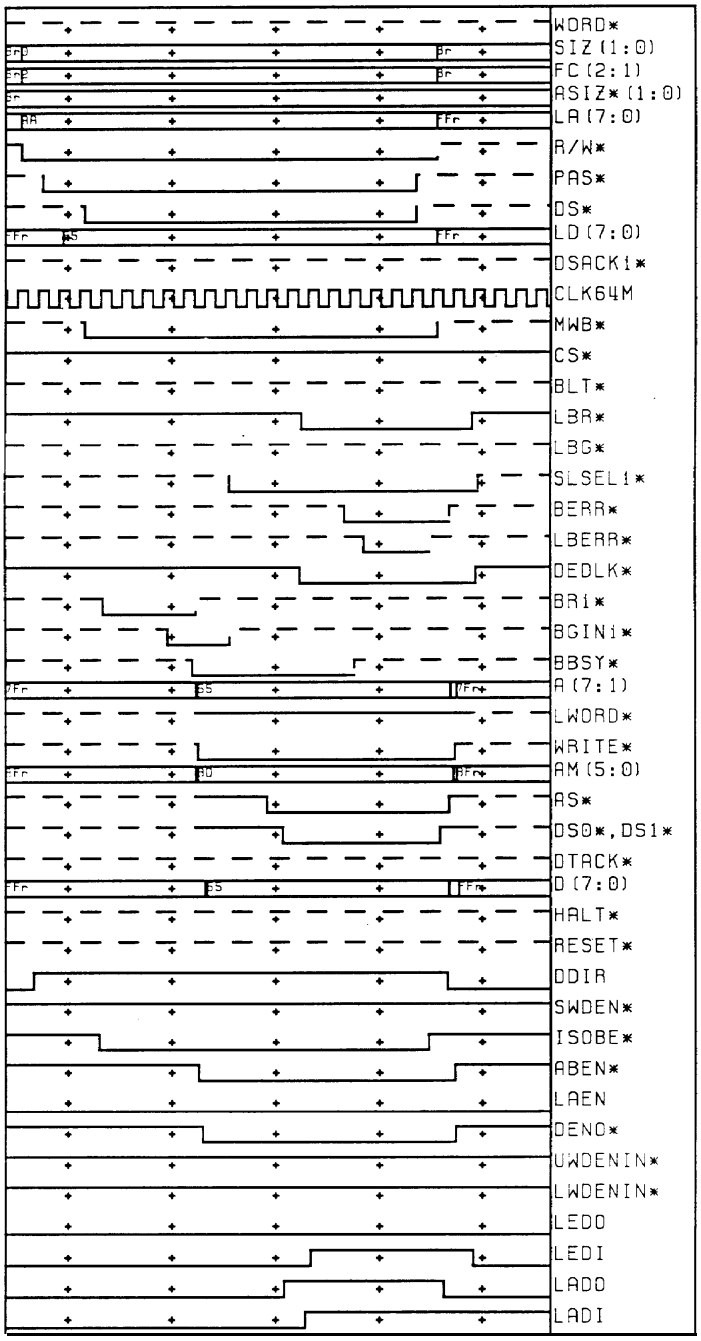

Figure 1-50. Master Self-Access

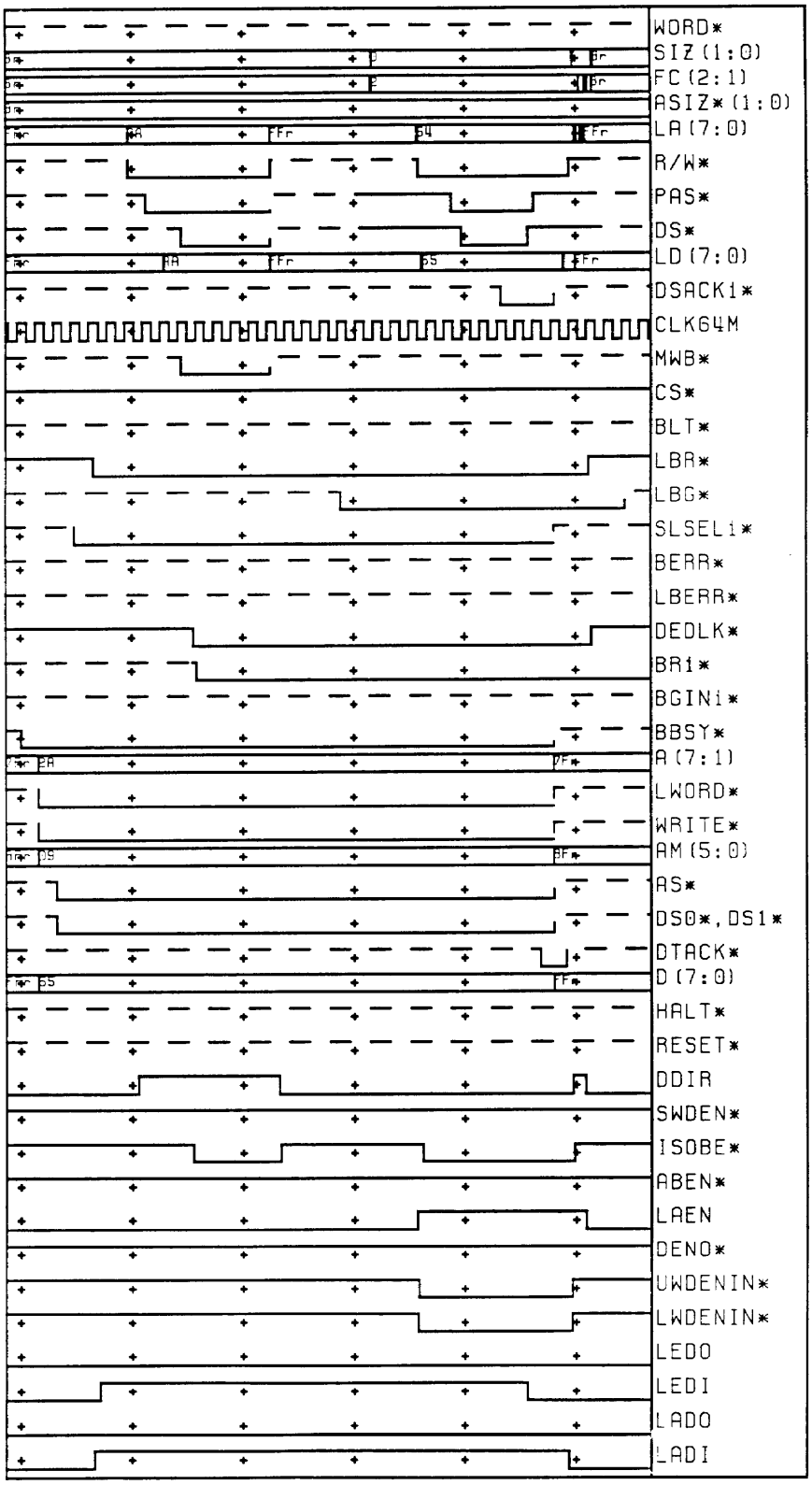

Figure 1-51. Master Deadlock Operation

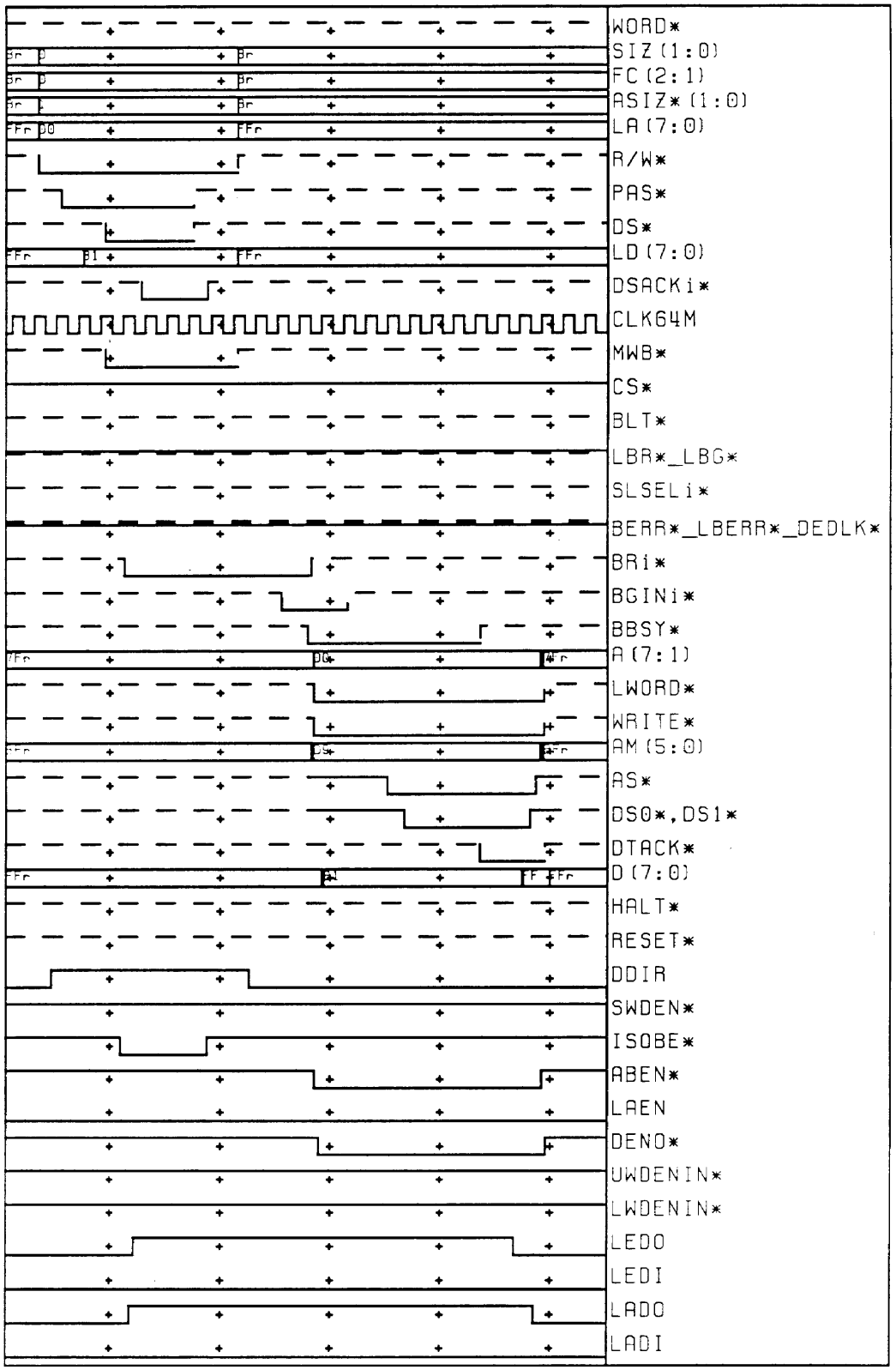

Figure 1-52. Master Write Post

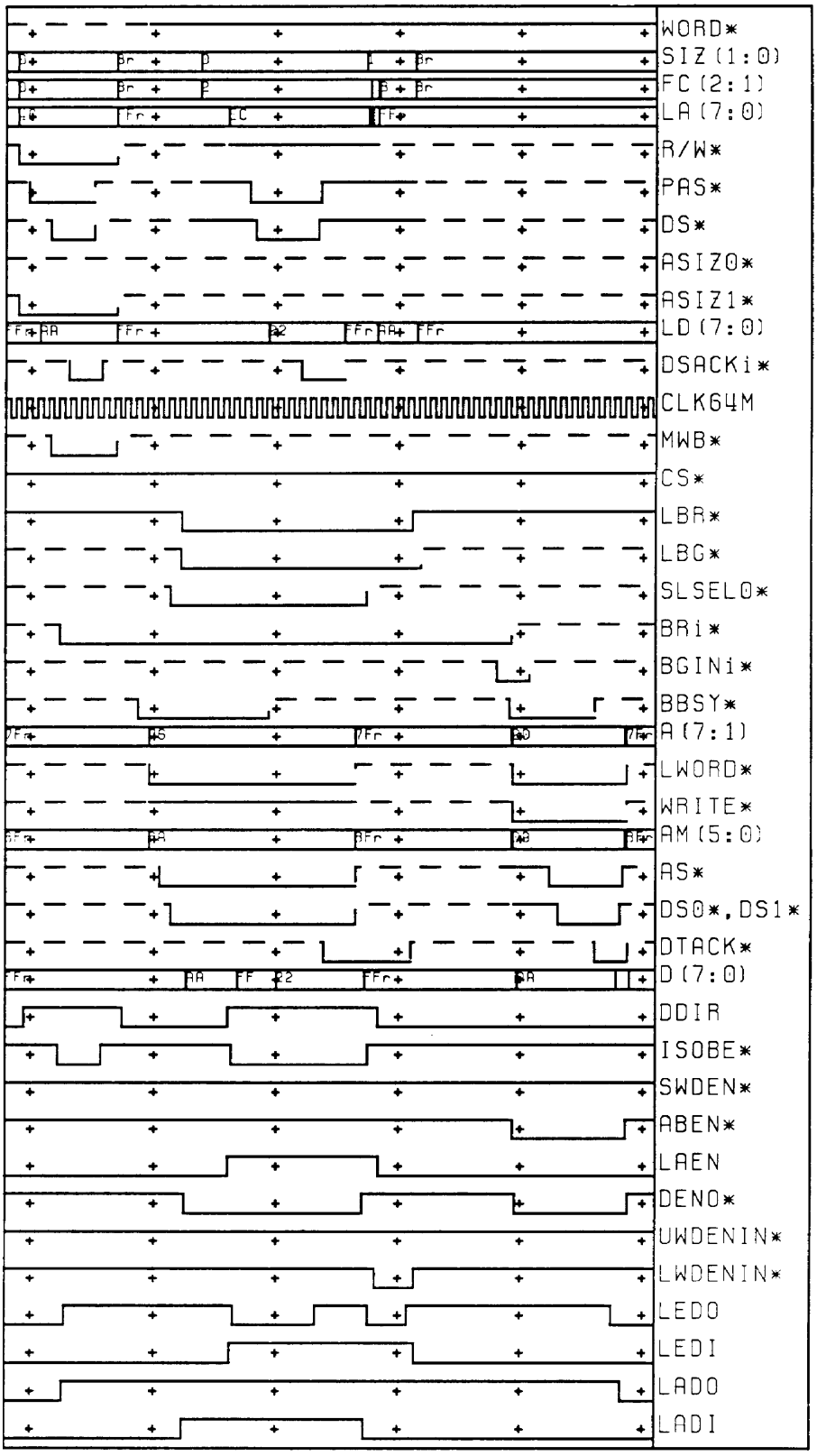

Figure 1-53. Master Write Post with Slave Read (shows data toggle)

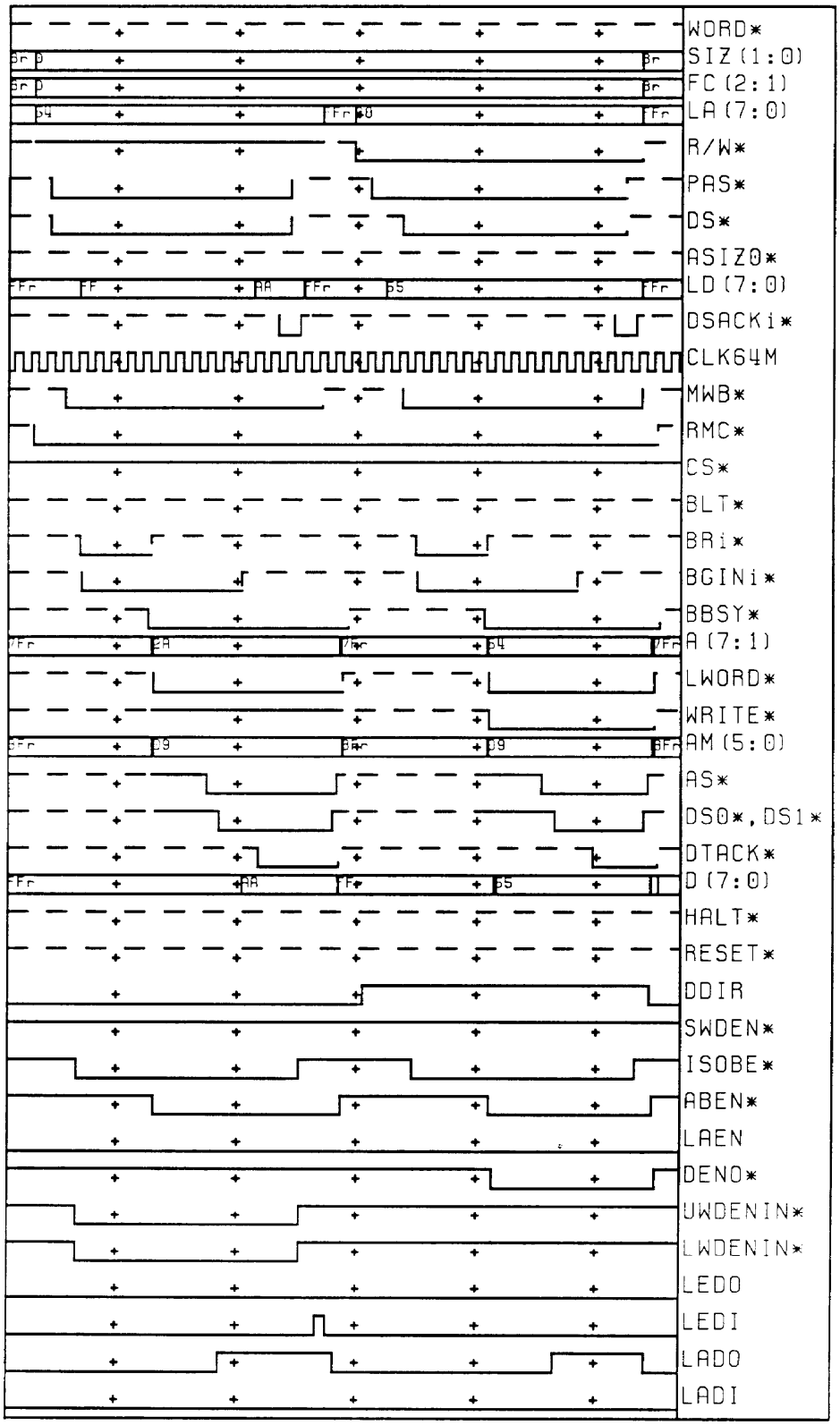

Figure 1-54. Master RMC1 ($AF[7:5] = 000)

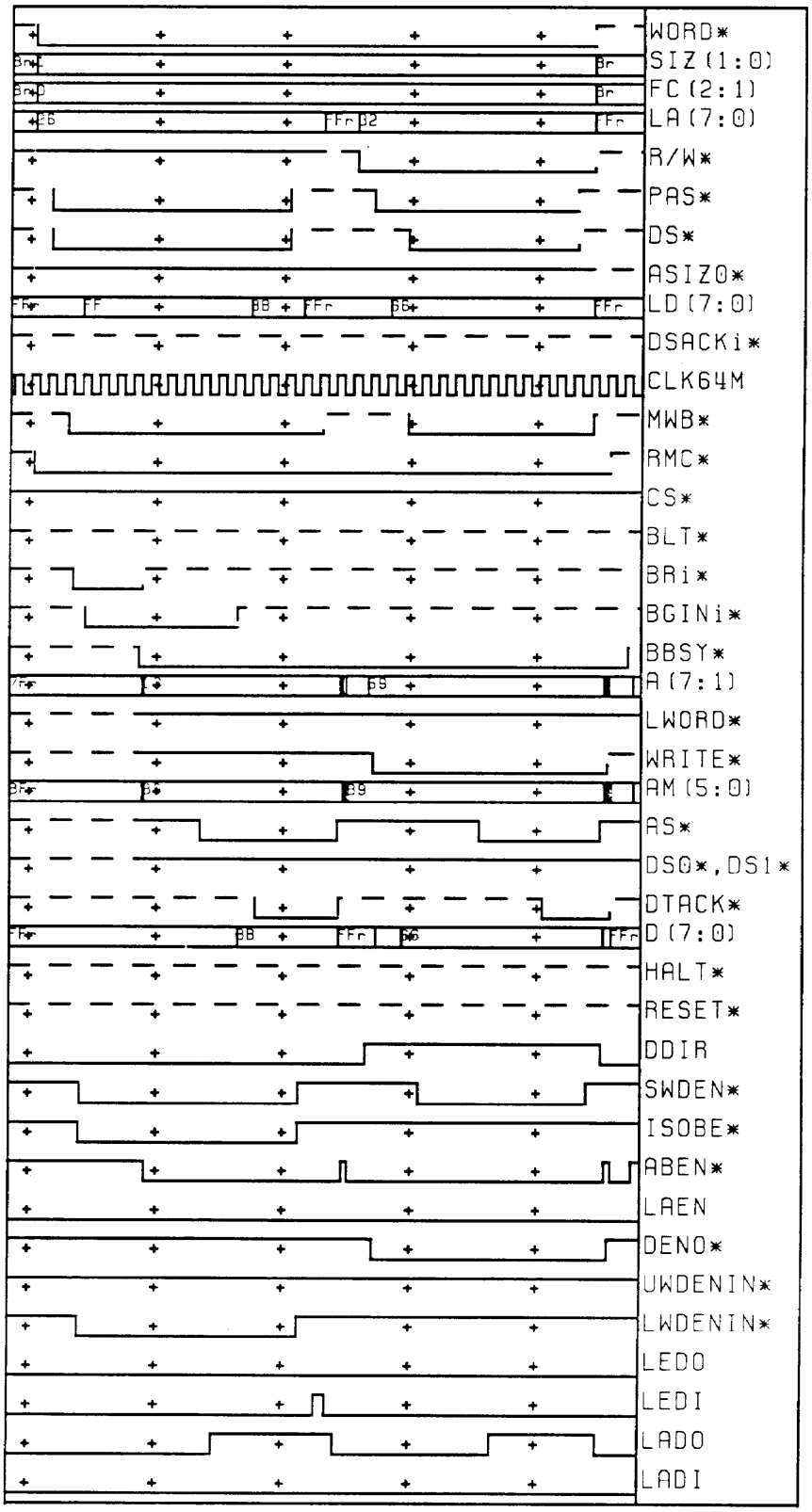

Figure 1-55. Master RMC2 ($AF[7:5] = 001)

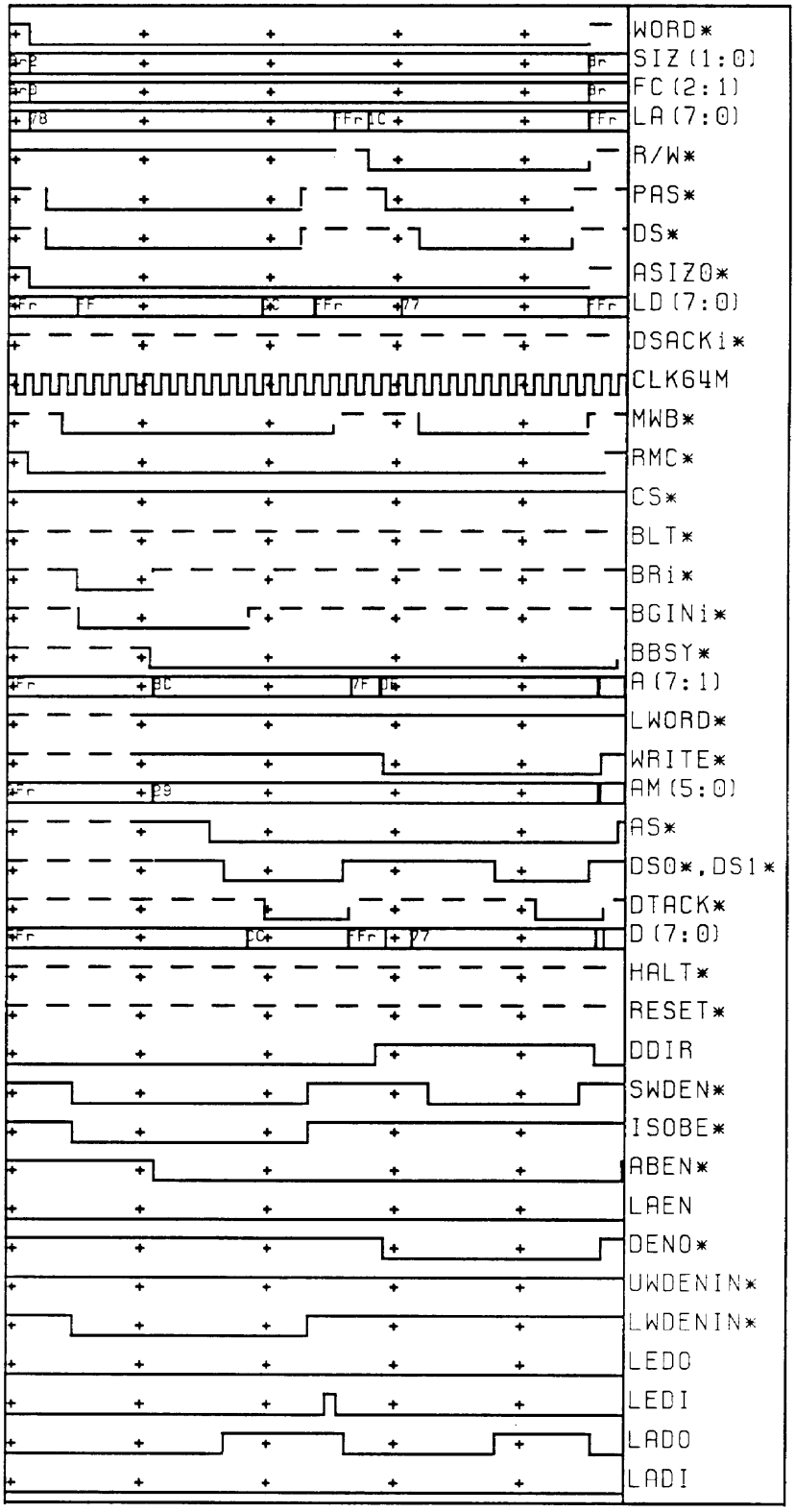

Figure 1-56. Master RMC3 ($AF[7:5] = 010)

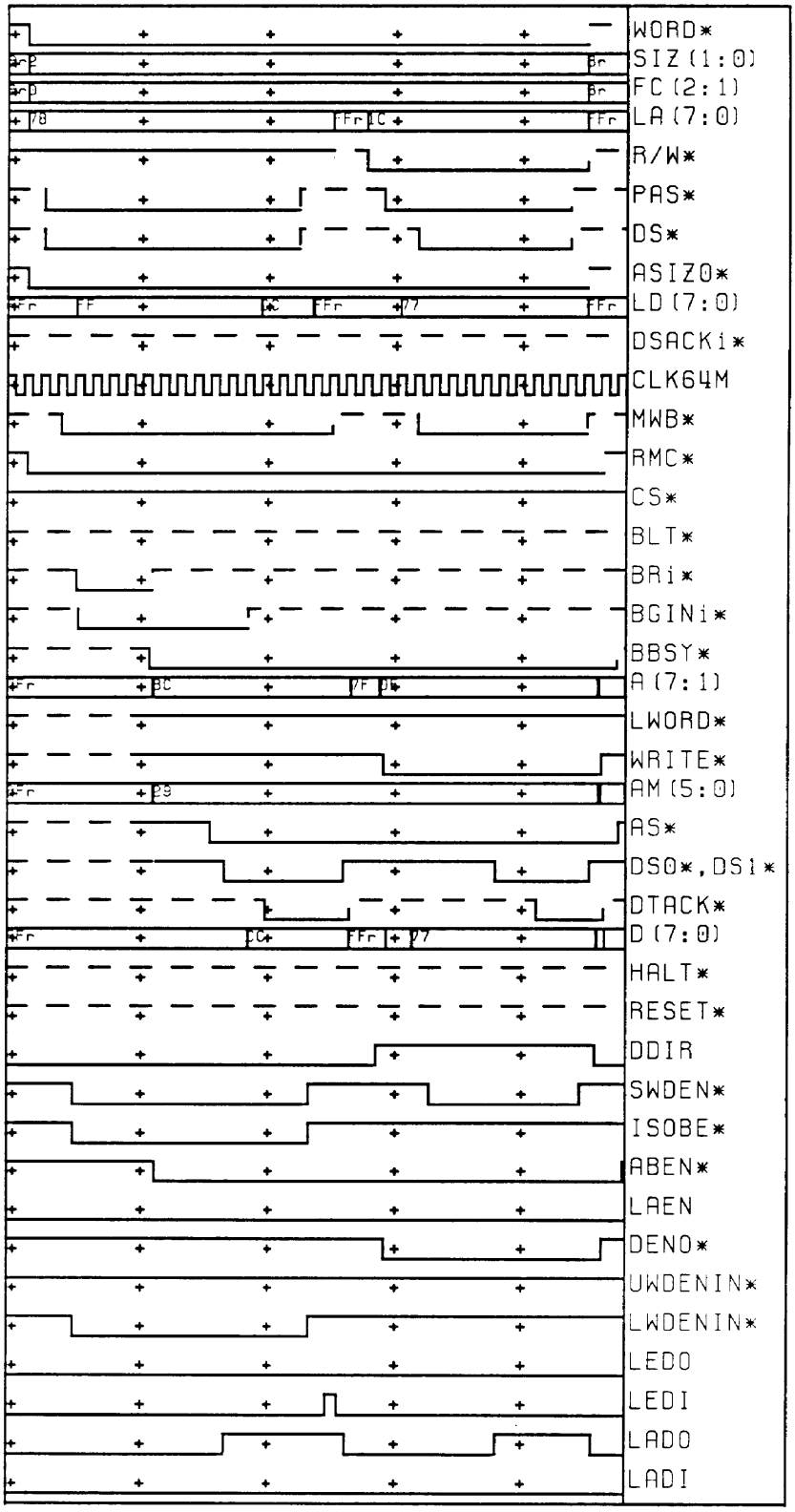

Figure 1-57. Master RMC4 ($AF[7:5] = 011)

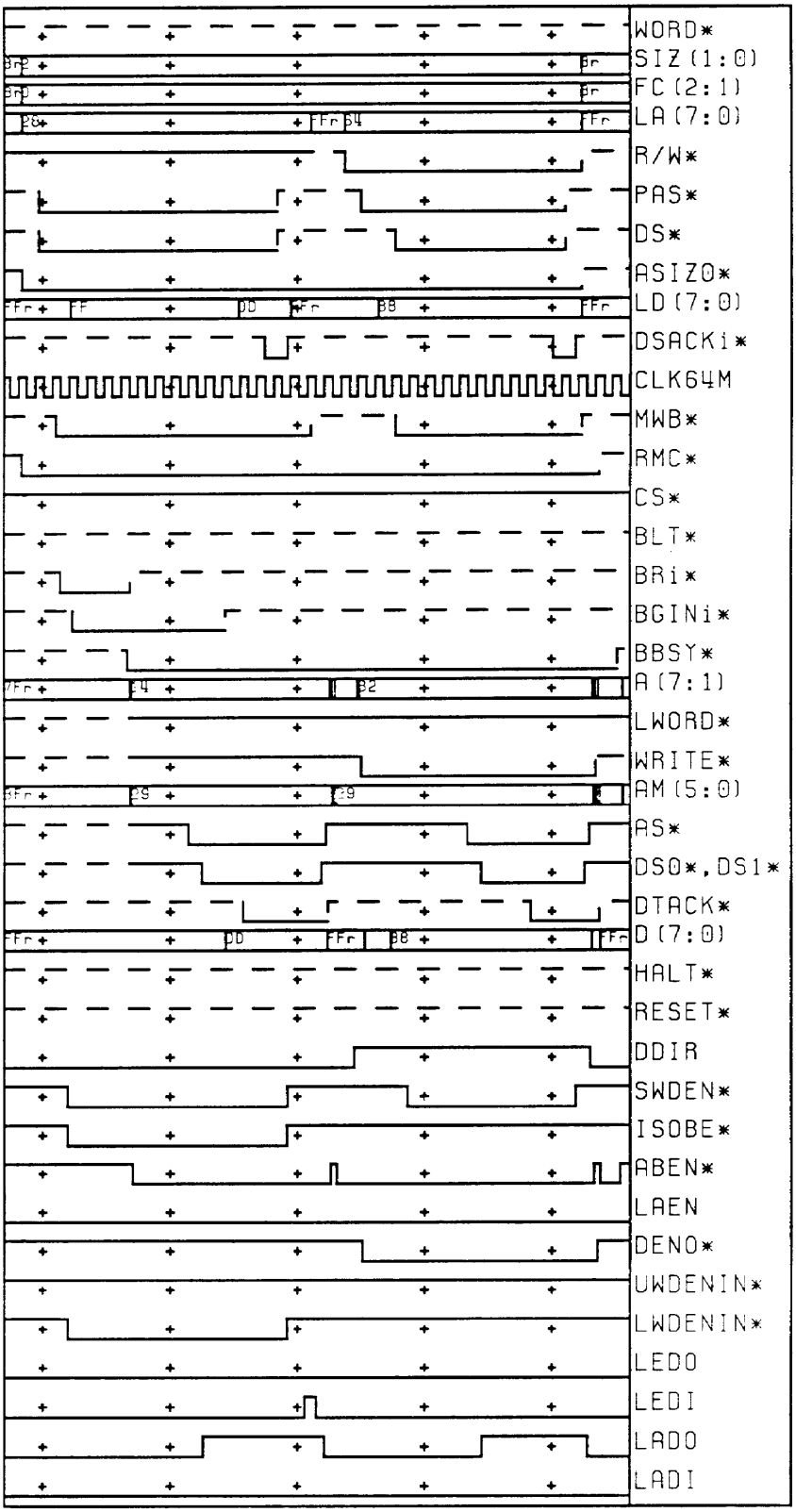

Figure 1-58. Master RMC5 ($AF[7:5] = 101)

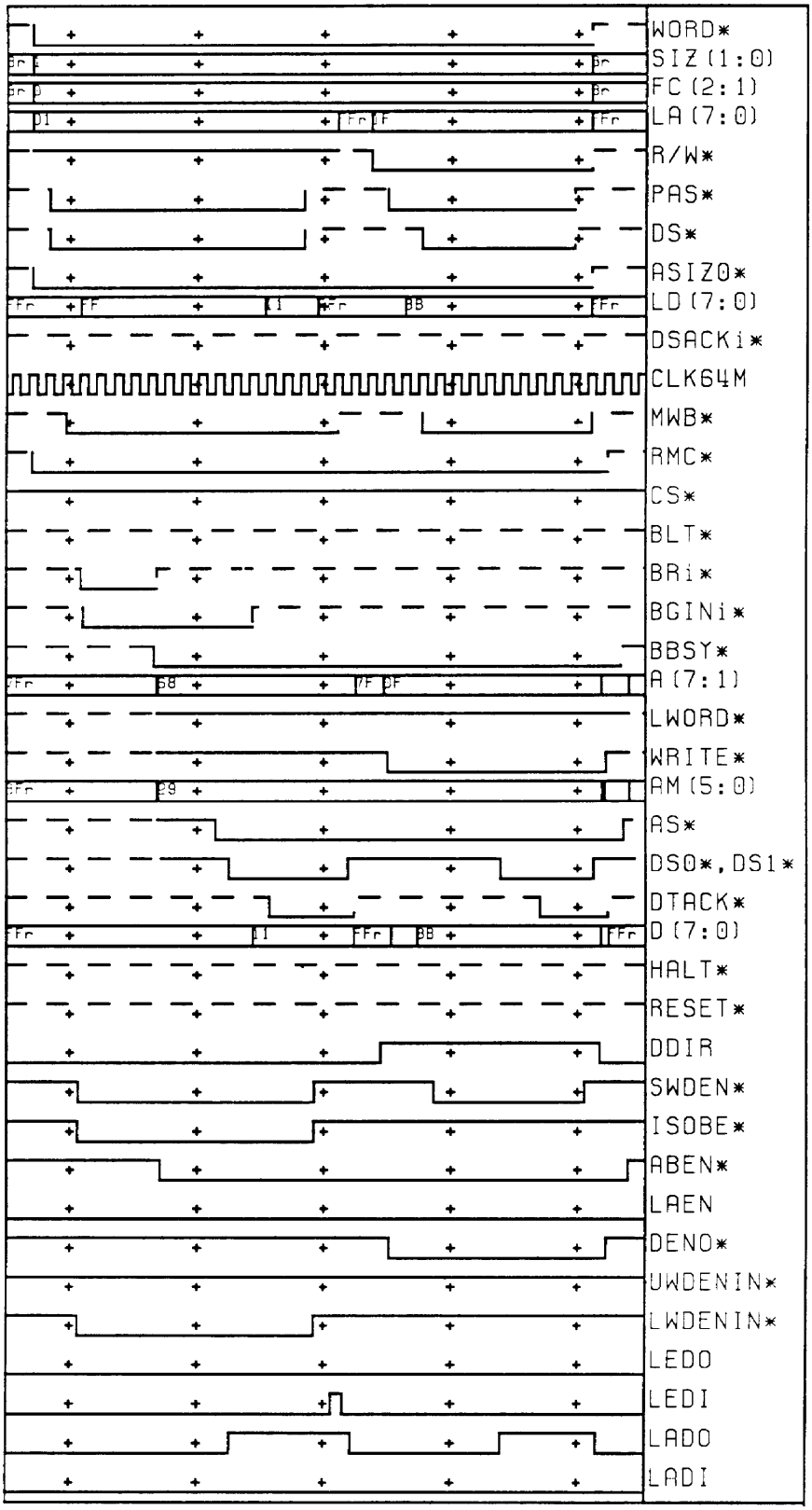

Figure 1-59. Master RMC6 Non-Byte ($AF[7:5] = 110)

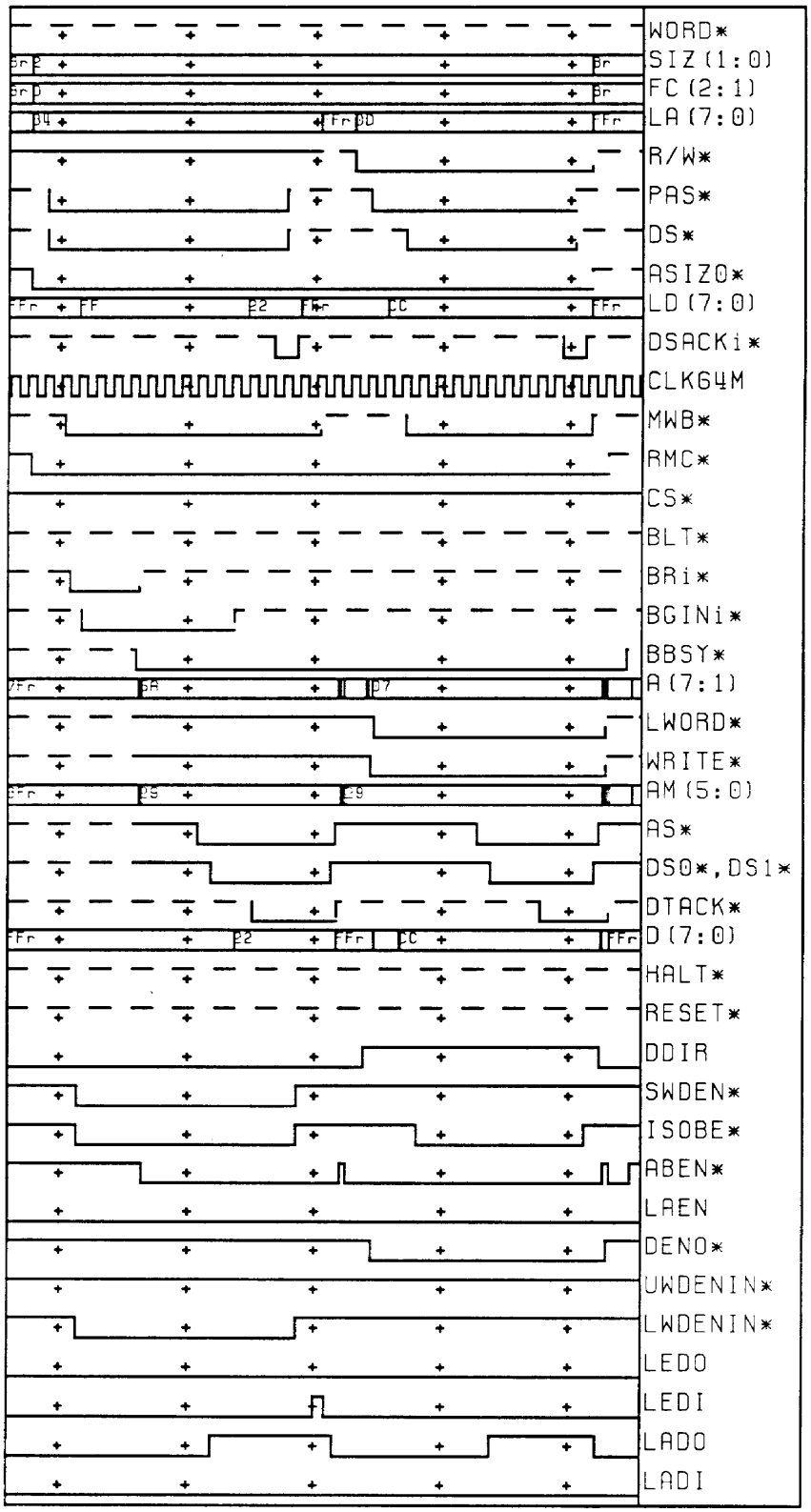

Figure 1-60. Master RMC7 ($AF[7:5] = 111)

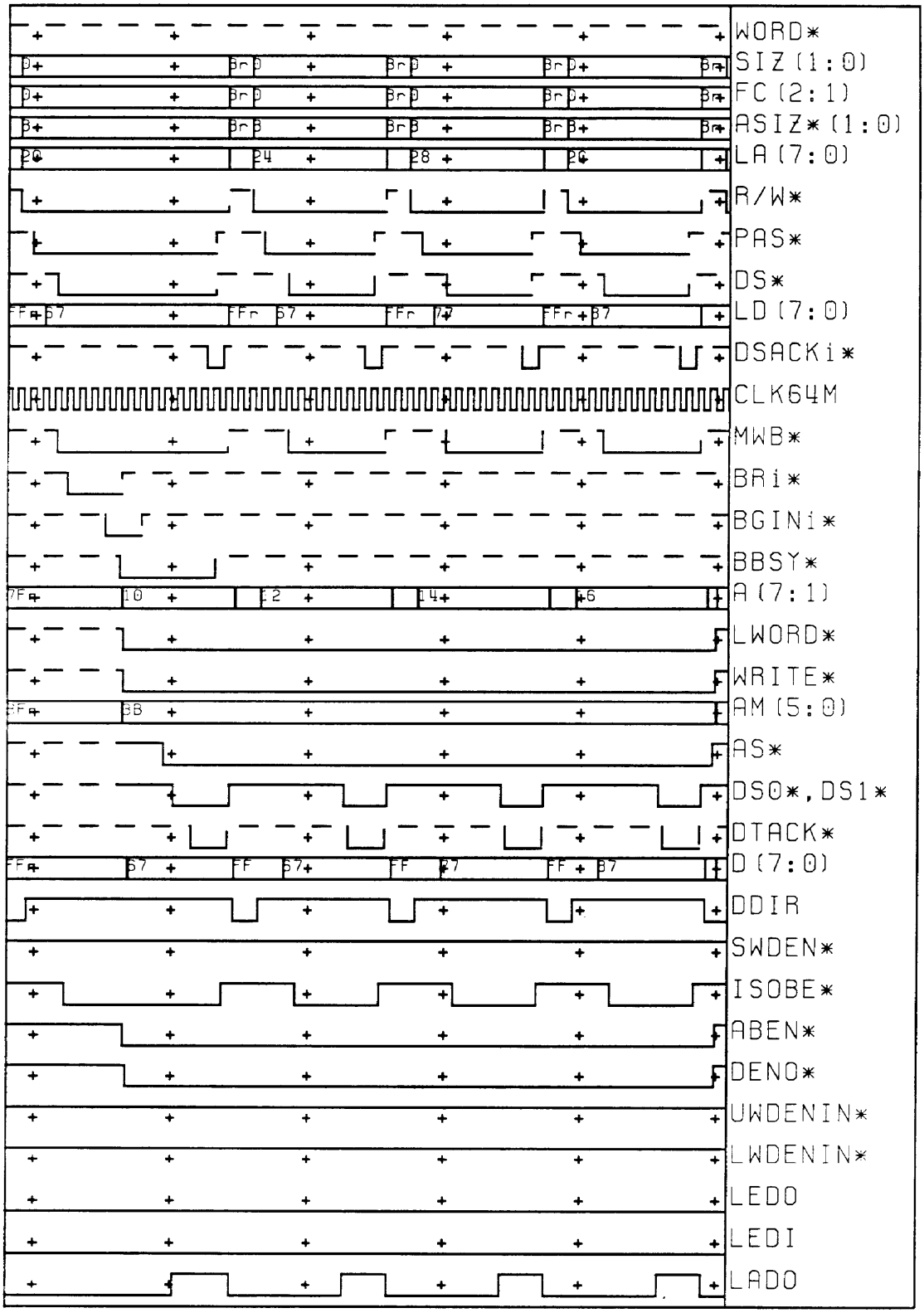

Figure 1-61. MOVEM Write Operation

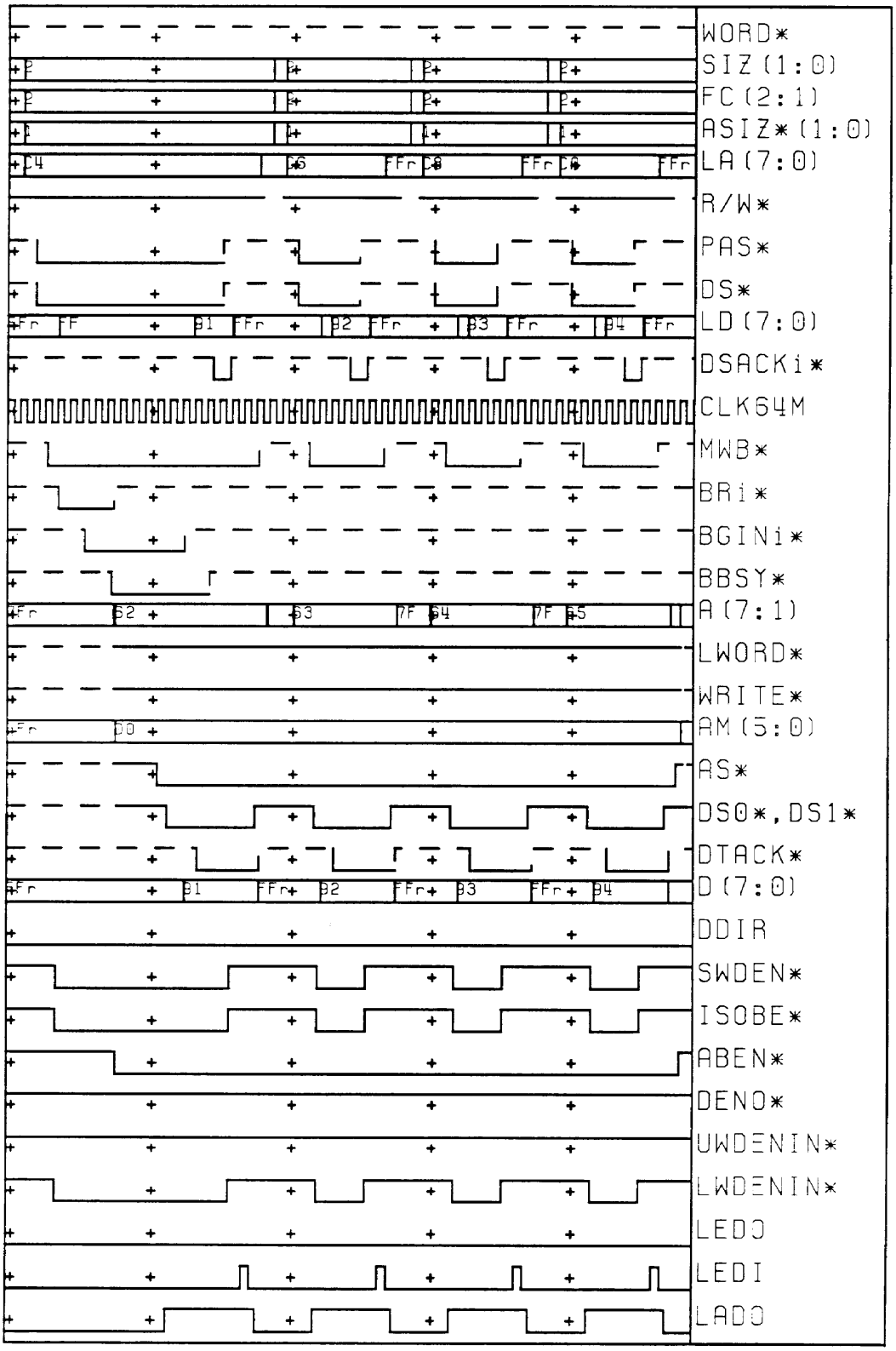

Figure 1-62. MOVEM Read Operation

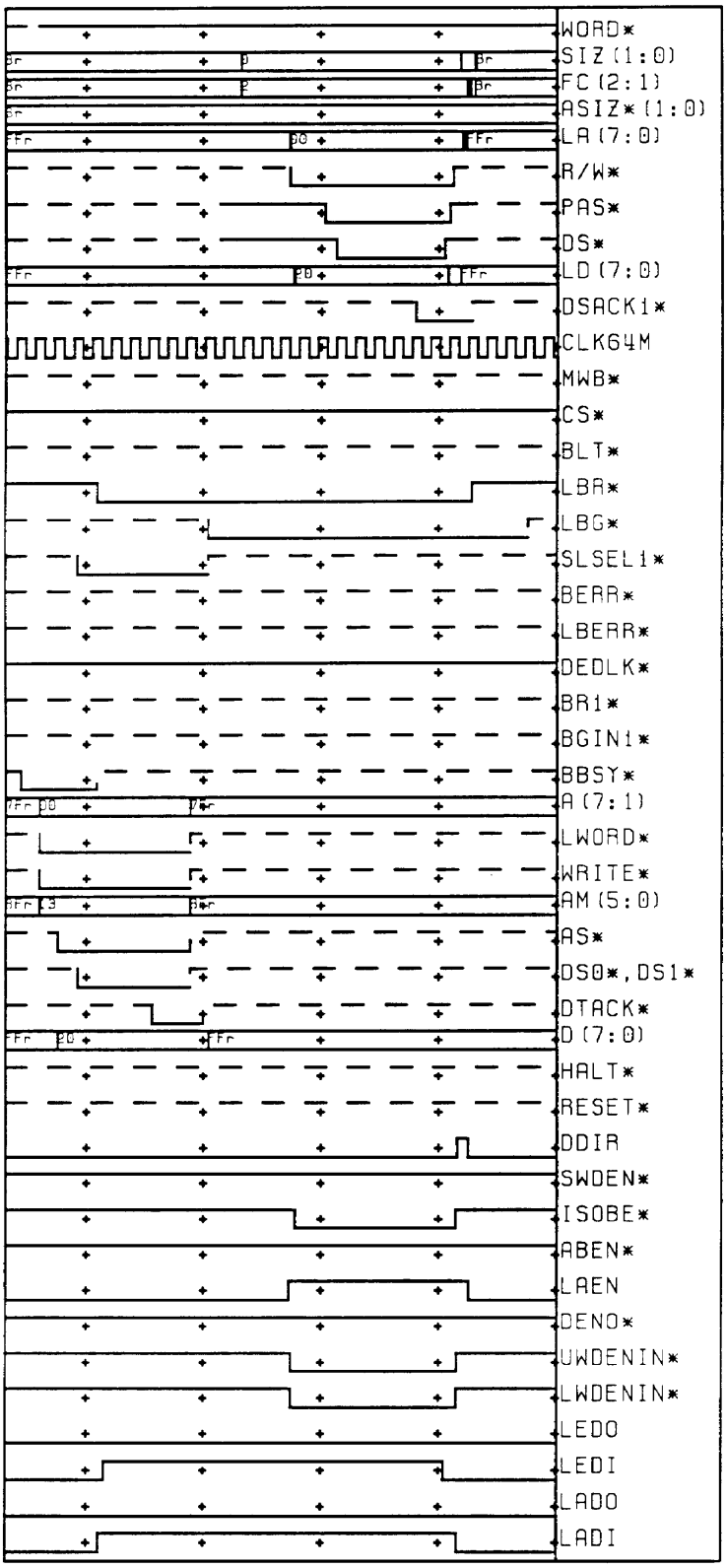

Figure 1-63. Slave Write Post

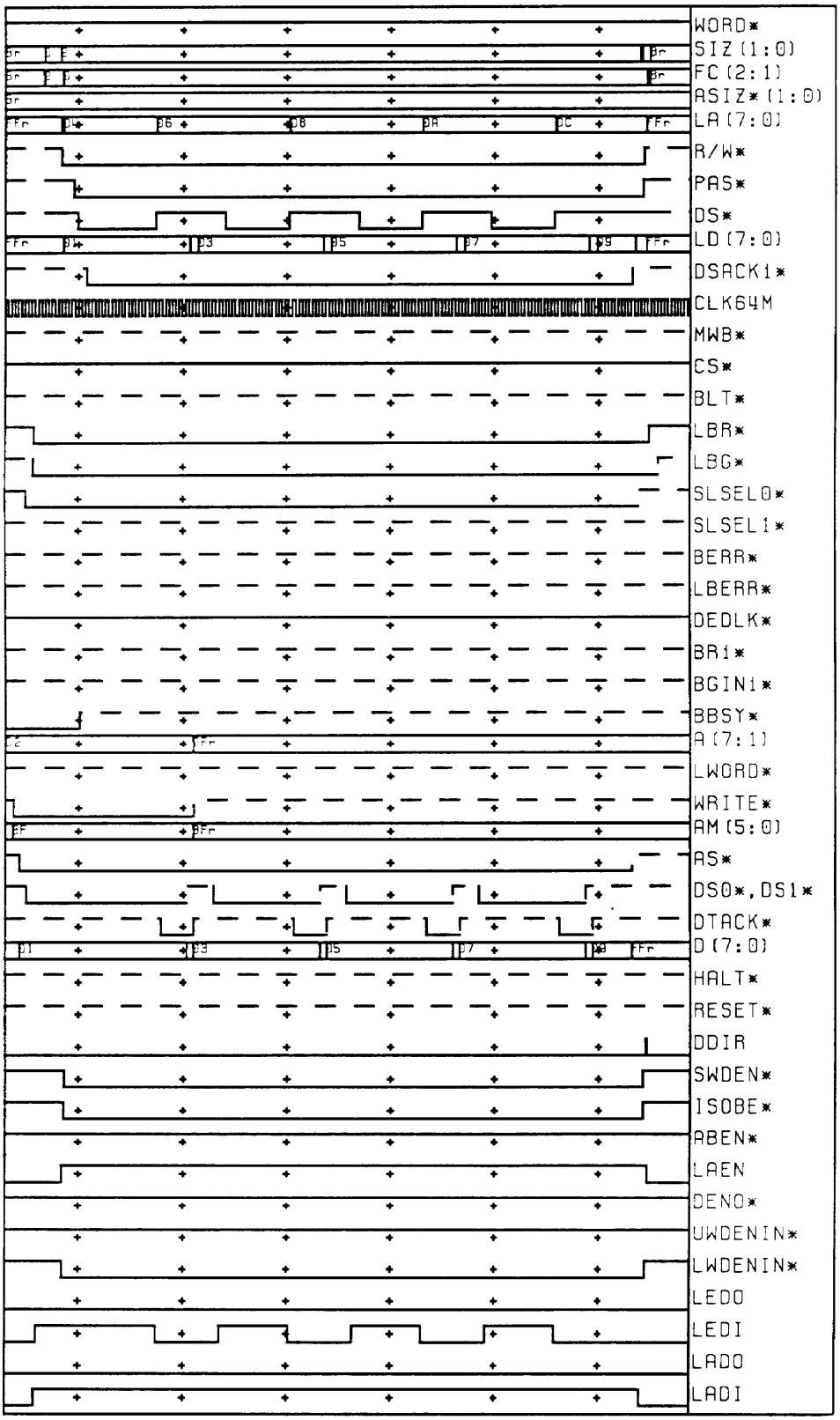

Figure 1-64. Slave Write Block Transfer Accelerated Mode ($C3[1:0]=10)

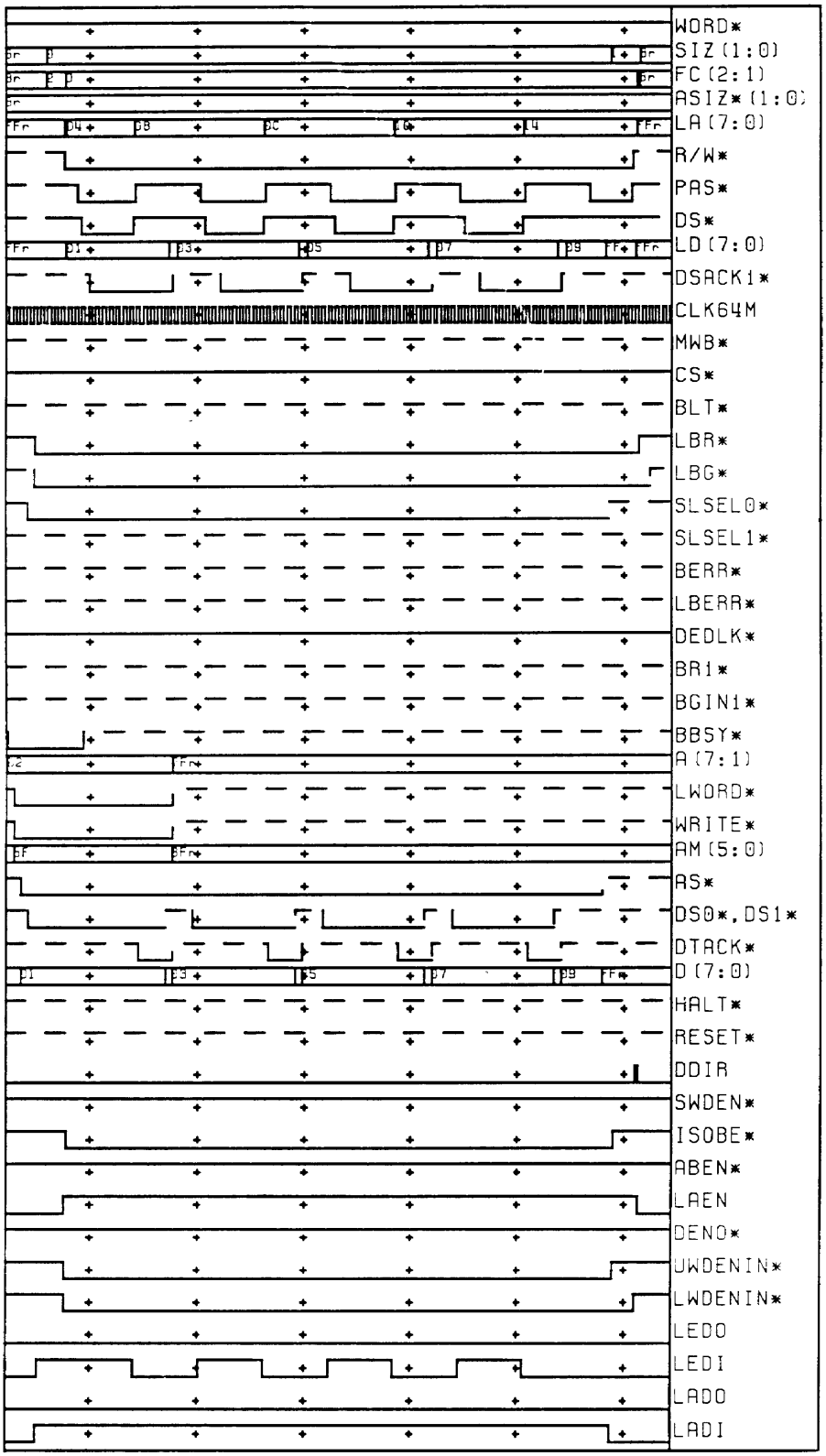

Figure 1-65. Slave Write Block Transfer Emulate Single-Cycle ($C3[1:0]=01)

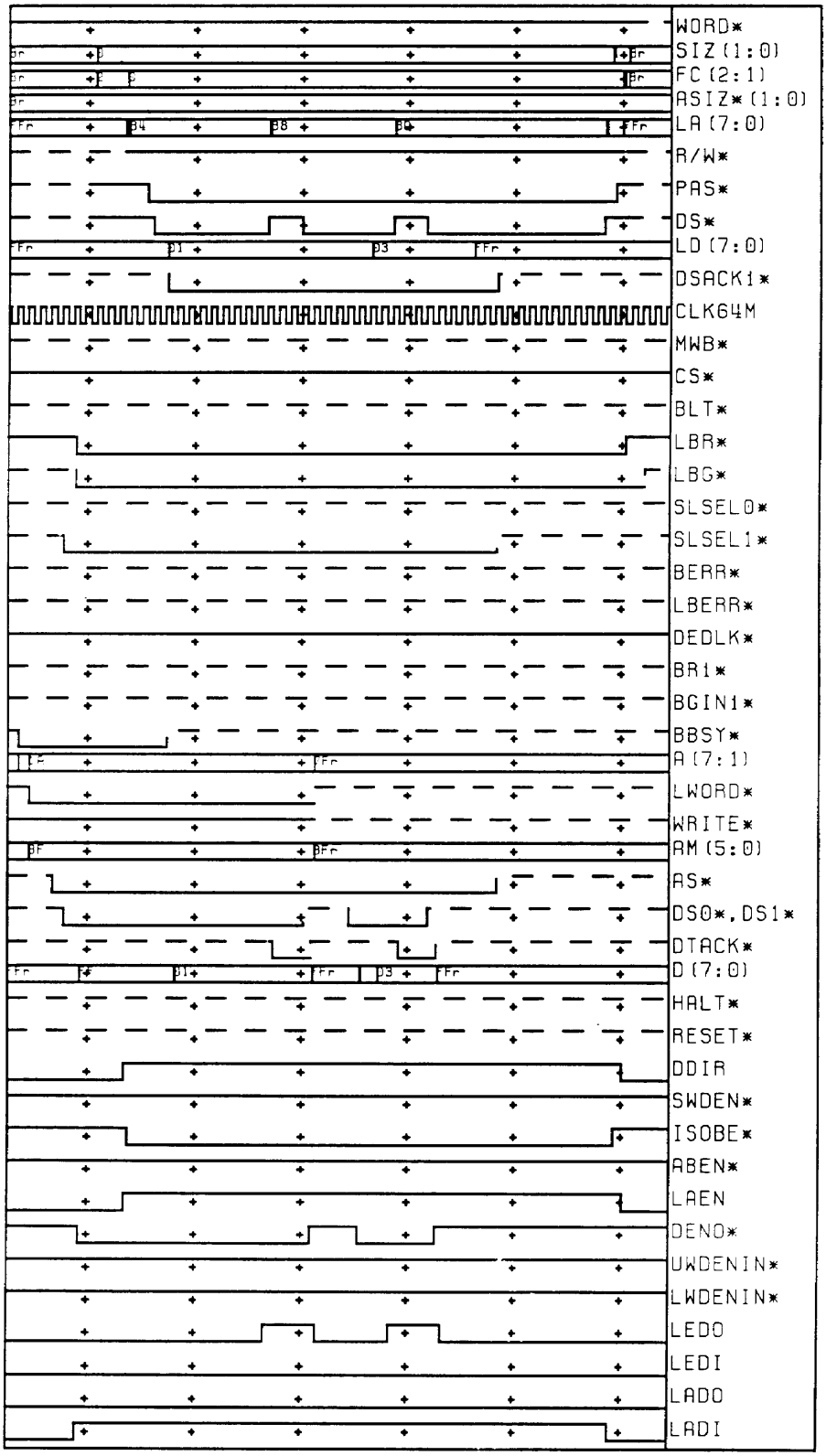

Figure 1-66. Slave Read Block Transfers Accelerated ($C3[1:0]=10)

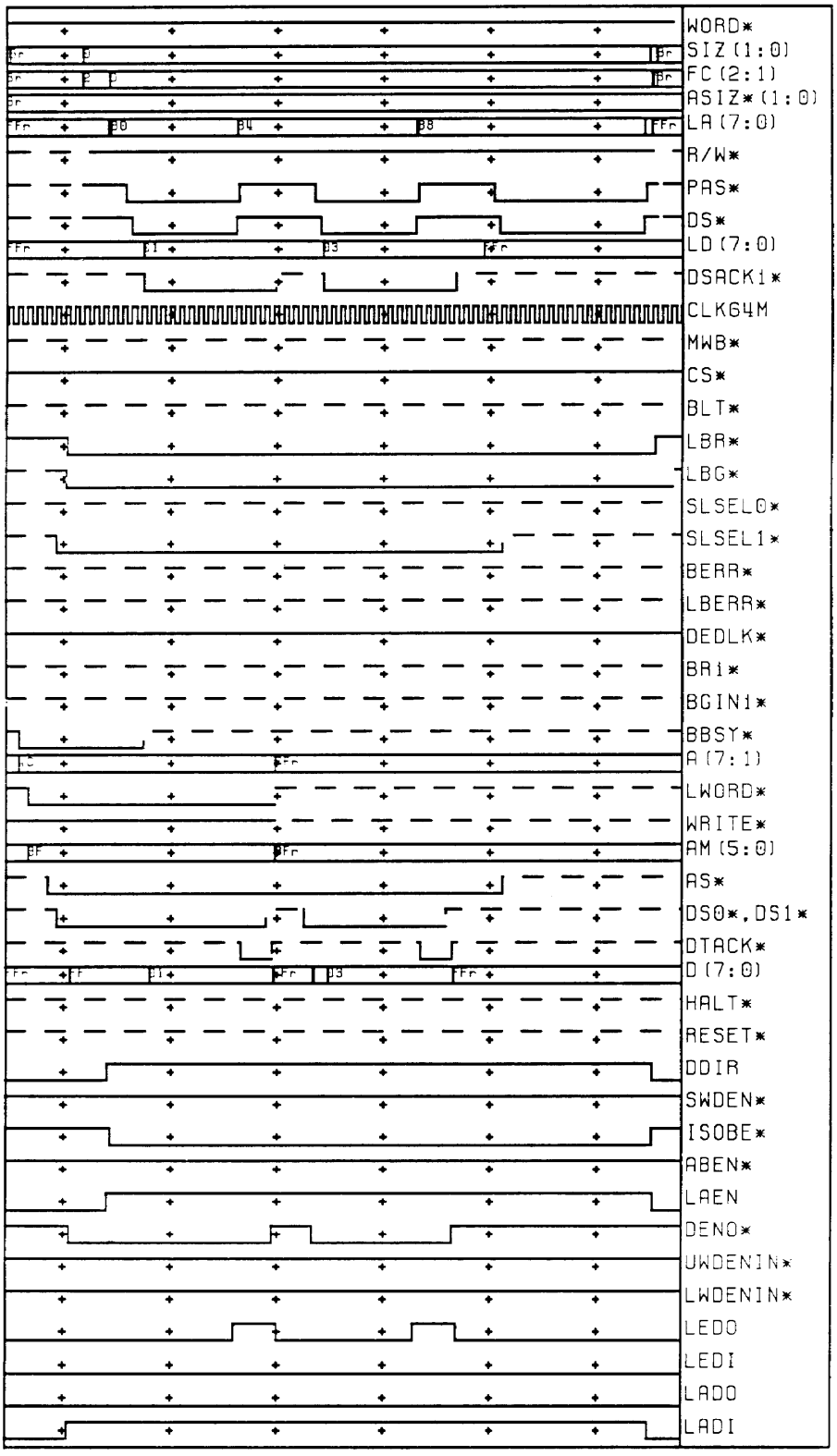

Figure 1-67. Slave Read Block Transfer Emulate Single-Cycle ($C3[1:0]=01)

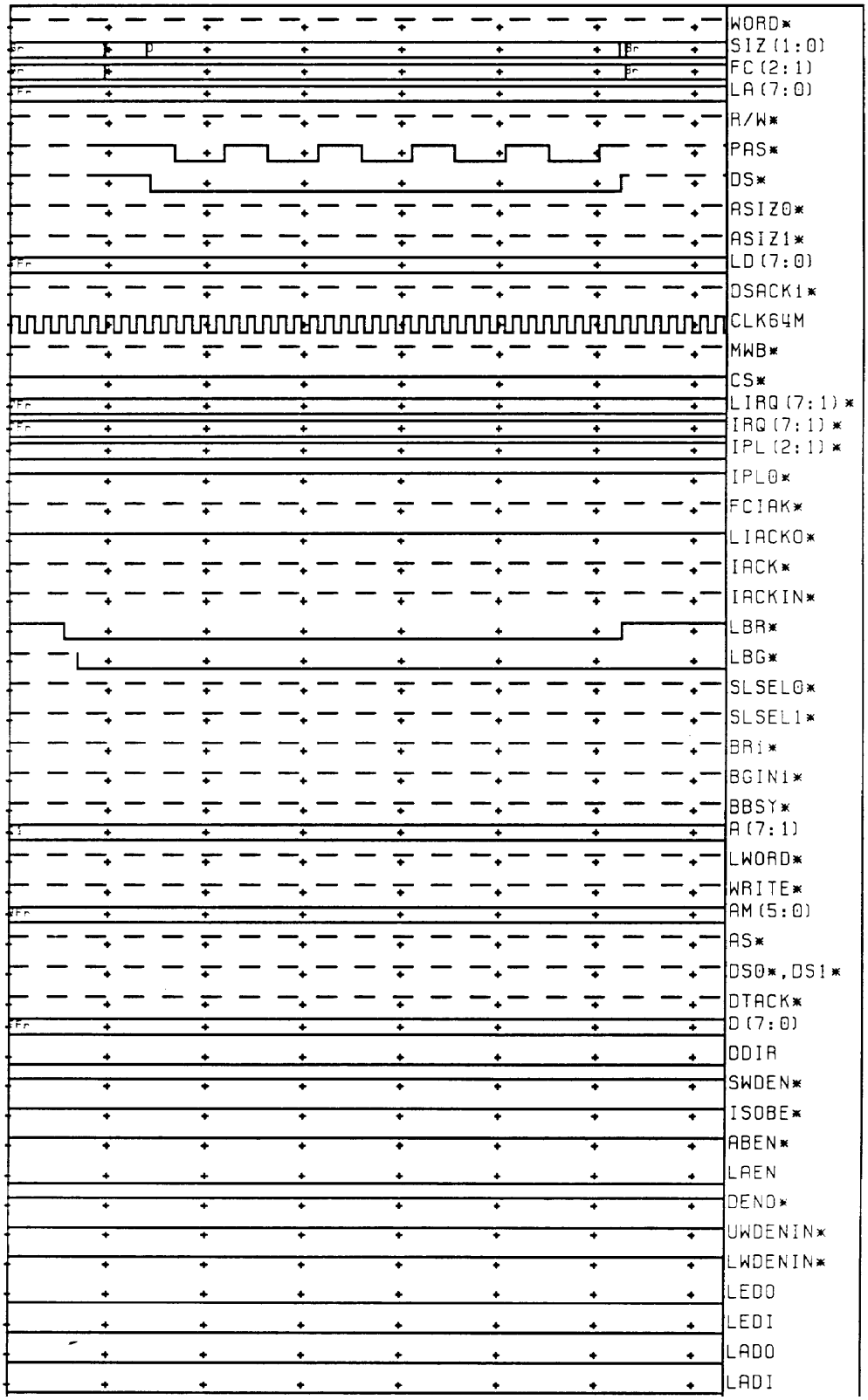

Figure 1-68. Refresh Timing

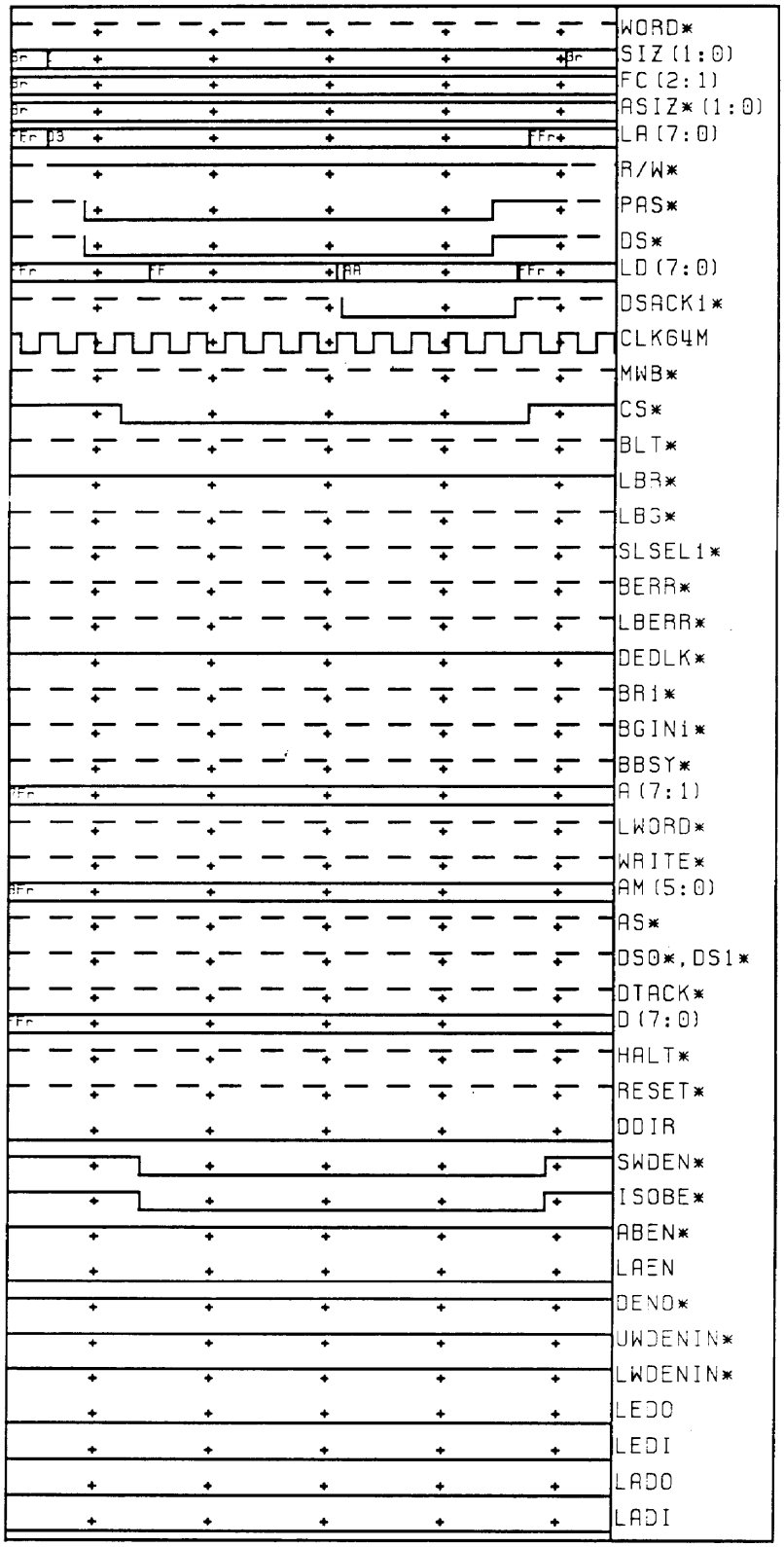

Figure 1-69. Register Read

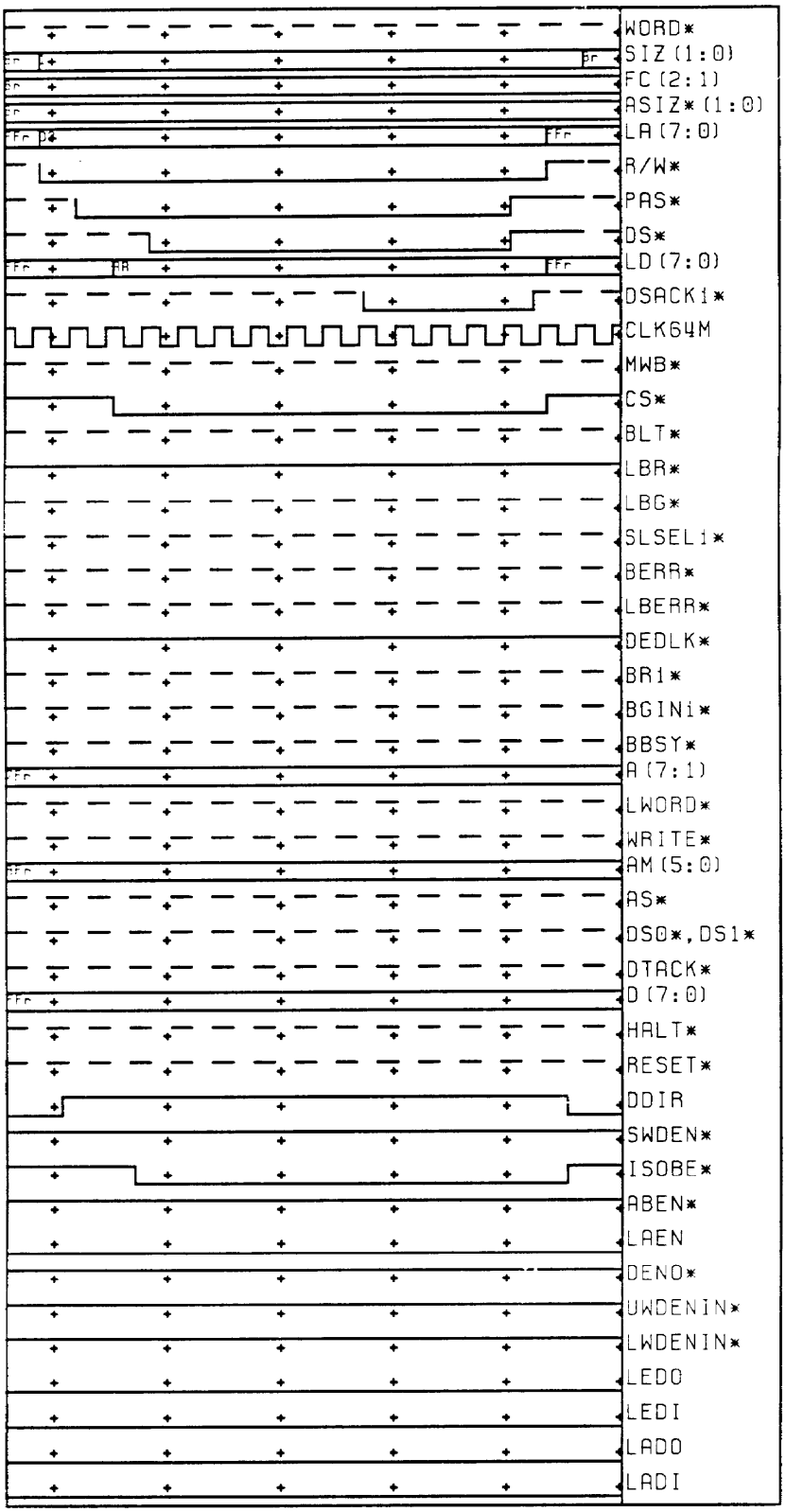

Figure 1-70. Register Write

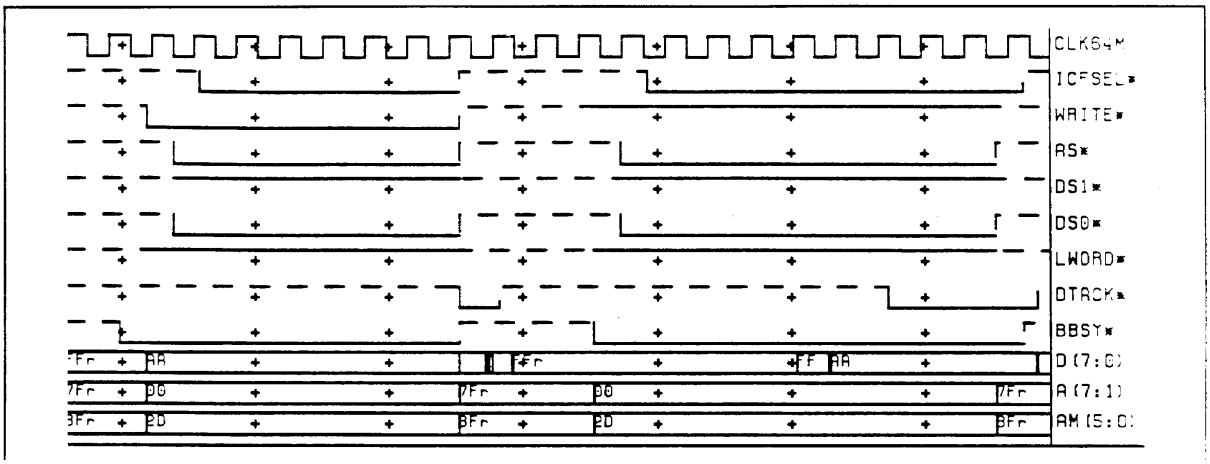

Figure 1-71. Interprocessor Communications Register Access Timing

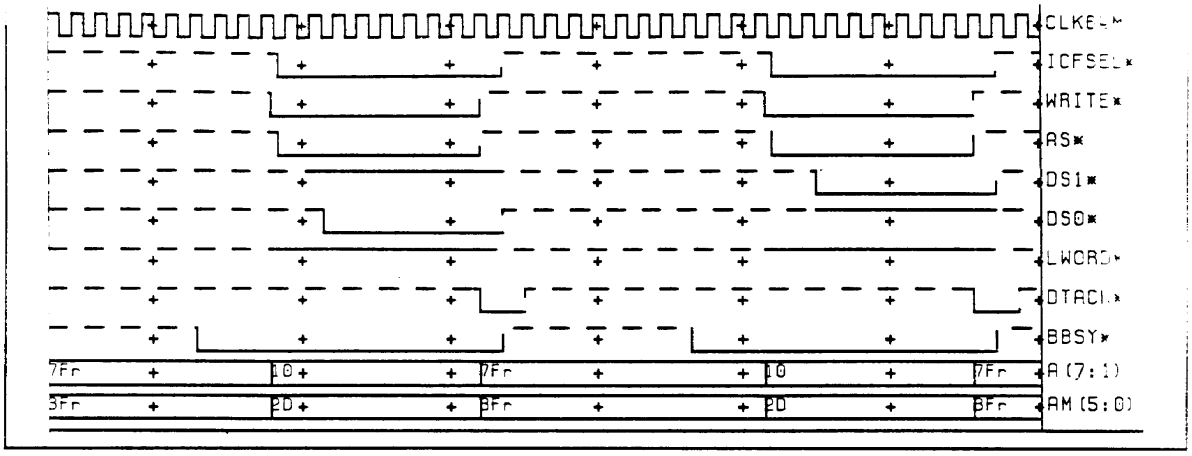

Figure 1-72. Interprocessor Communication Module Switch Access Timing

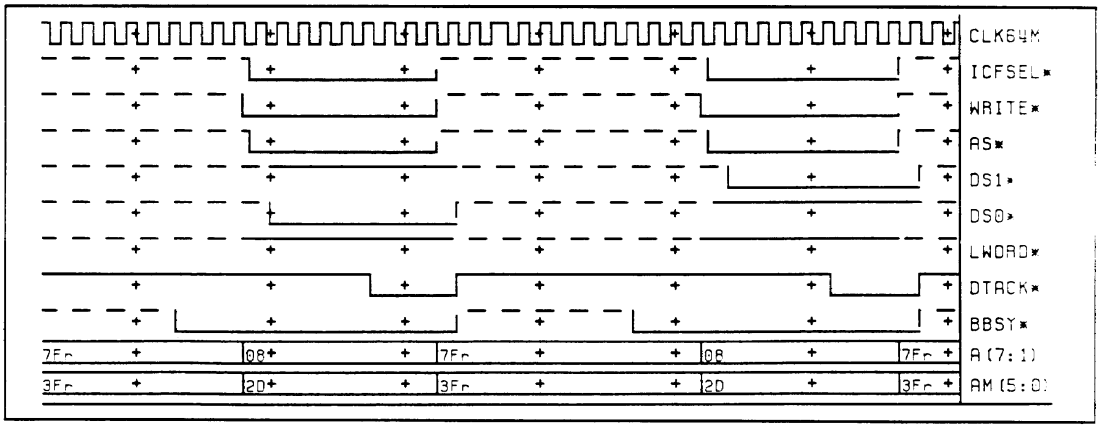

Figure 1-73. Interprocessor Communications Global Switch Access Timing

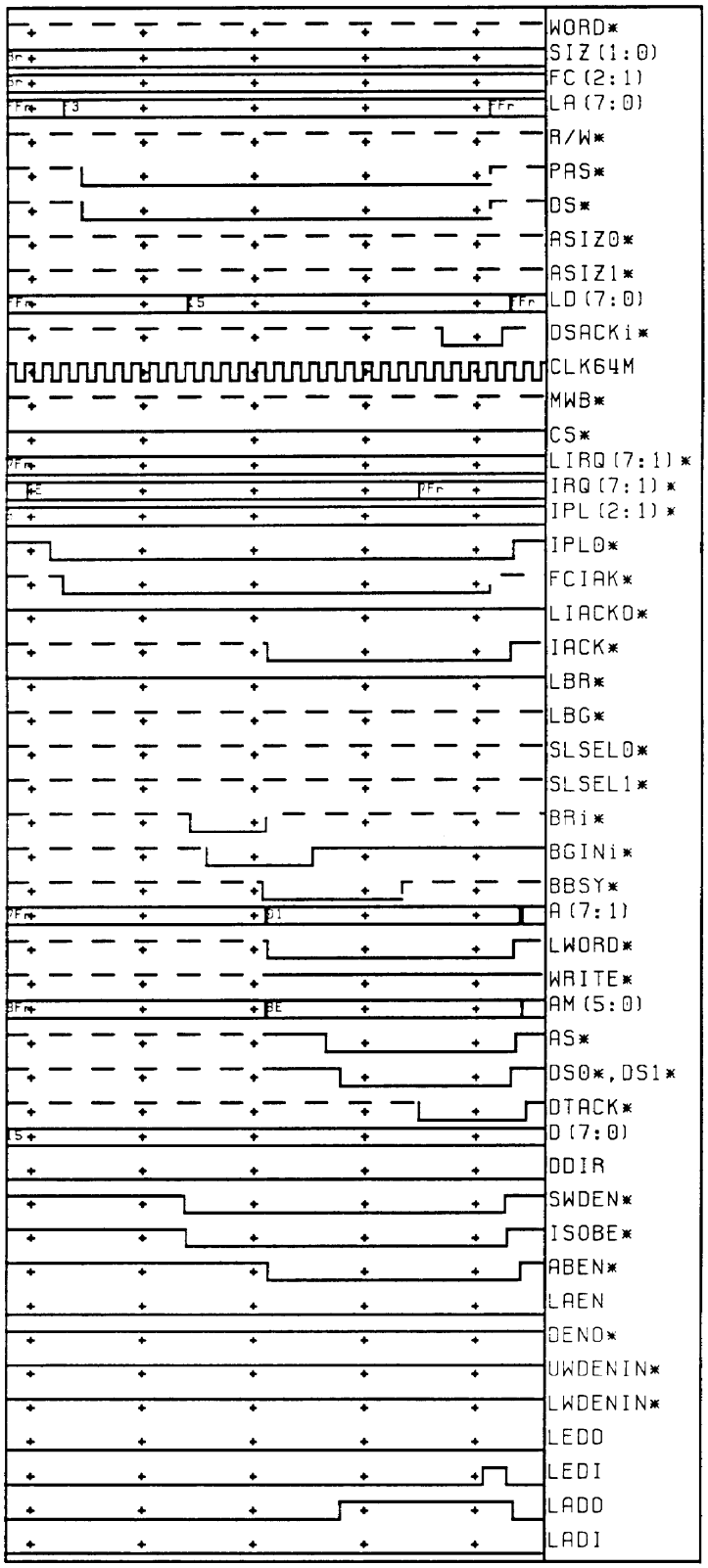

Figure 1-74. VMEbus Interrupt Acknowledge Cycle

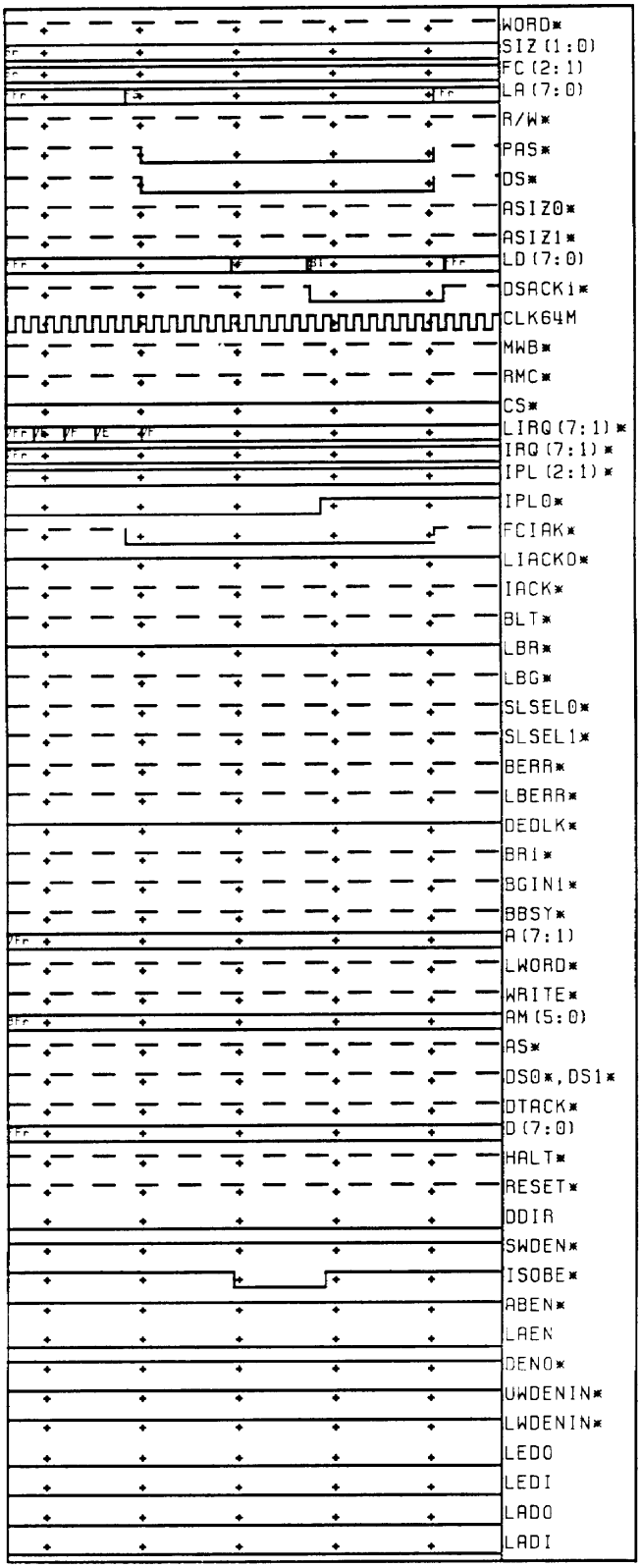

Figure 1-75. Local Interrupt Acknowledge Cycle

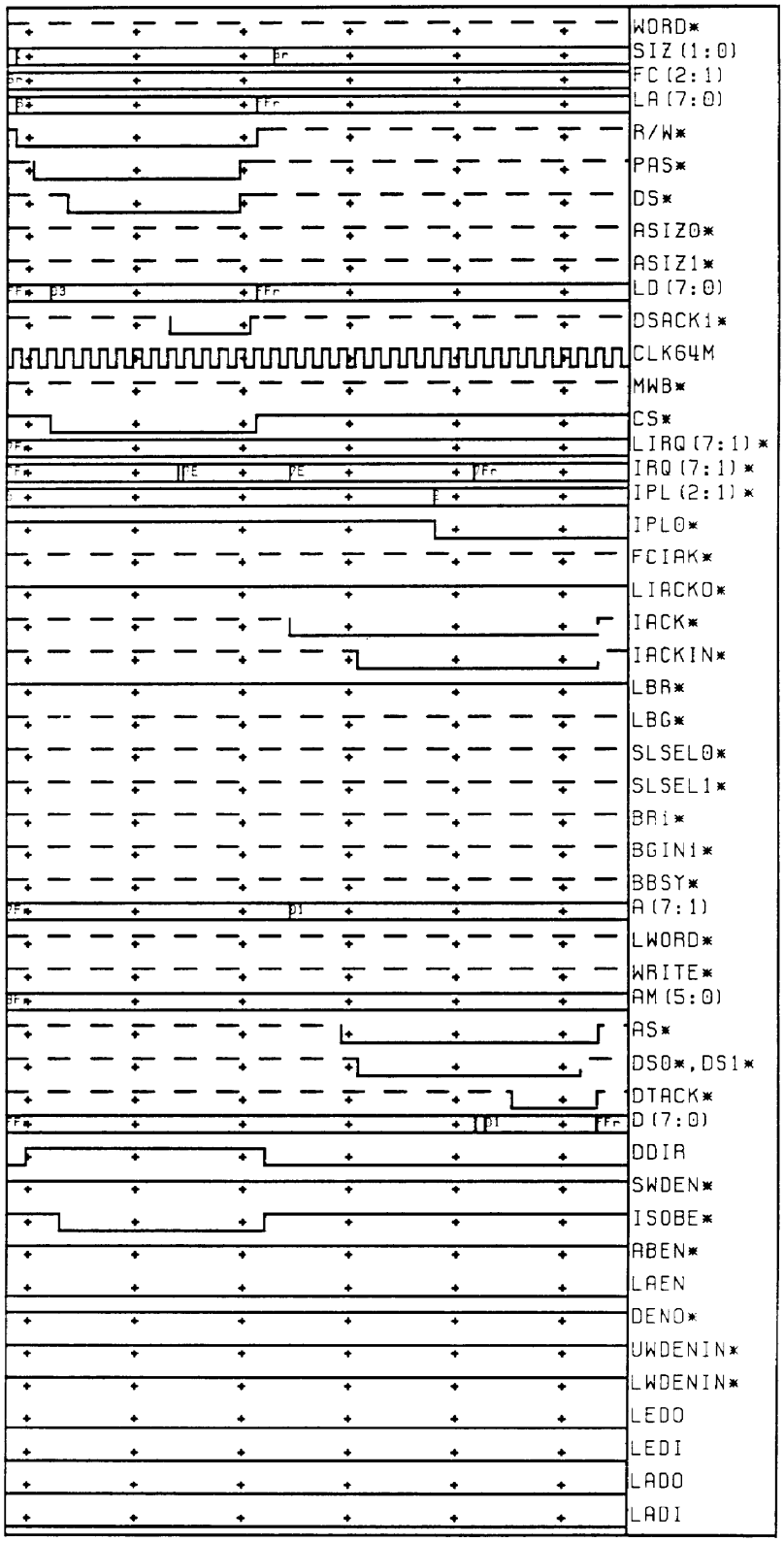

Figure 1-76. Interrupter Acknowledge Cycle

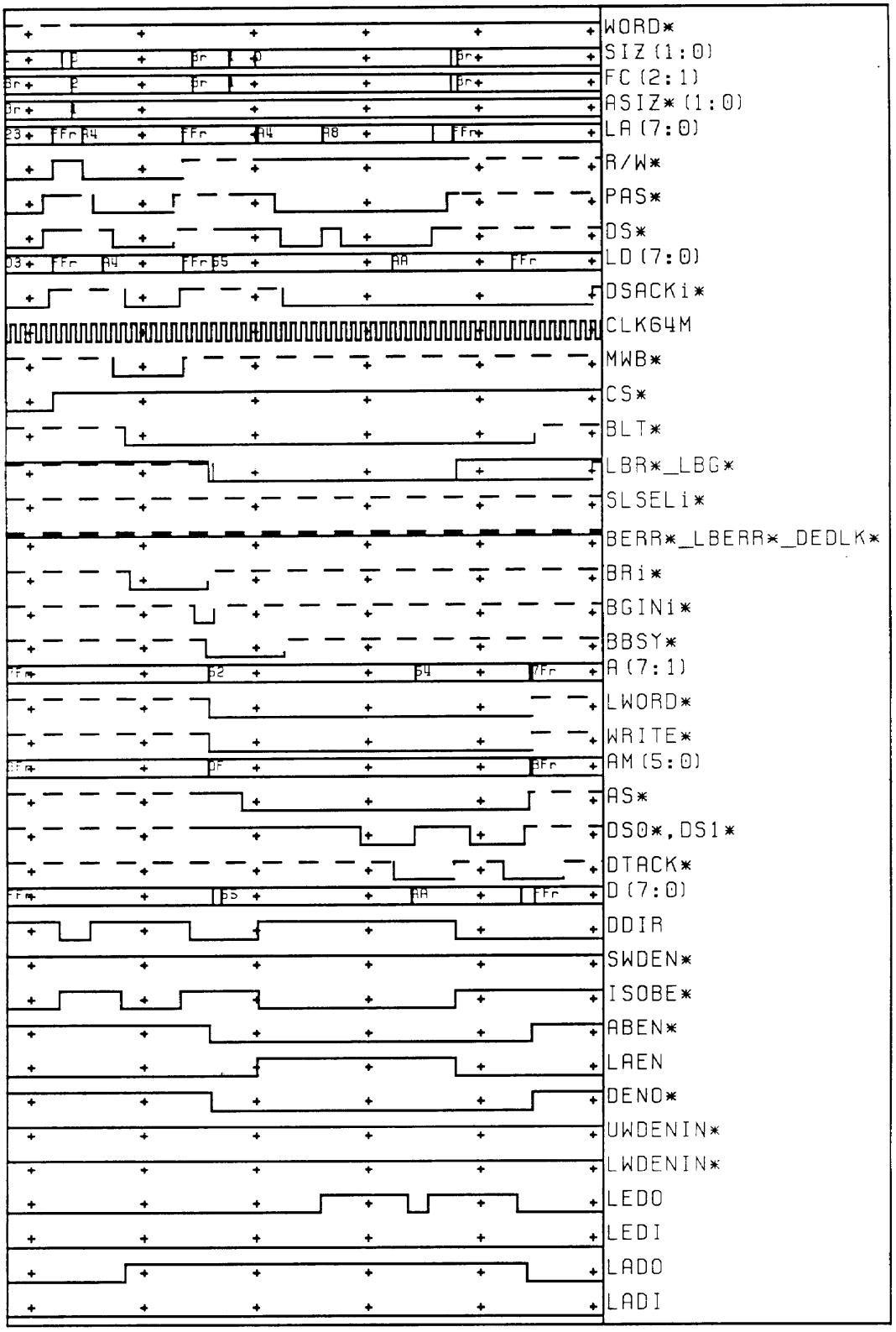

Figure 1-77. Block Transfer: VME Write: Burst of 2

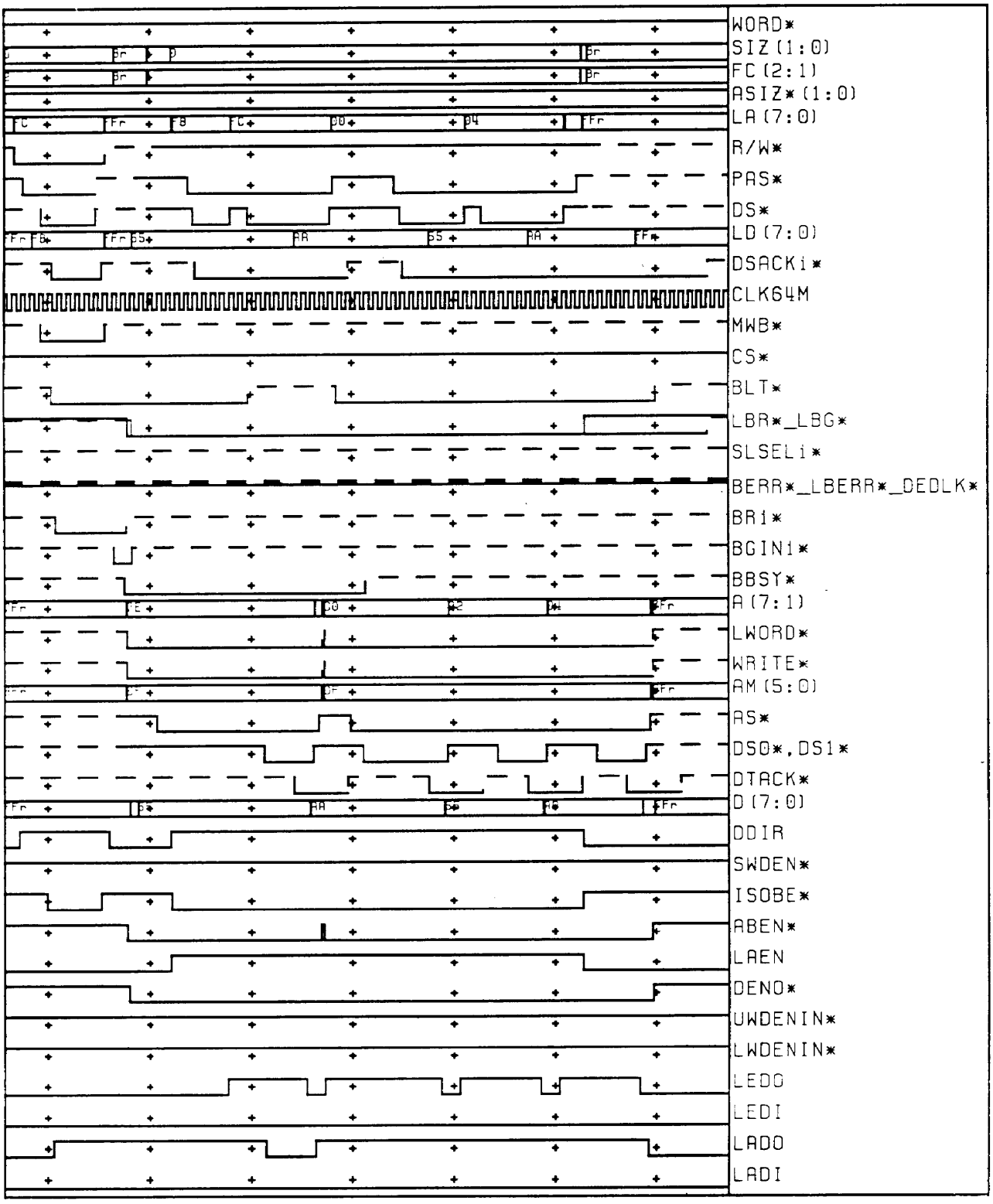

Figure 1-78. VME Boundary Crossing and Local Boundary Crossing

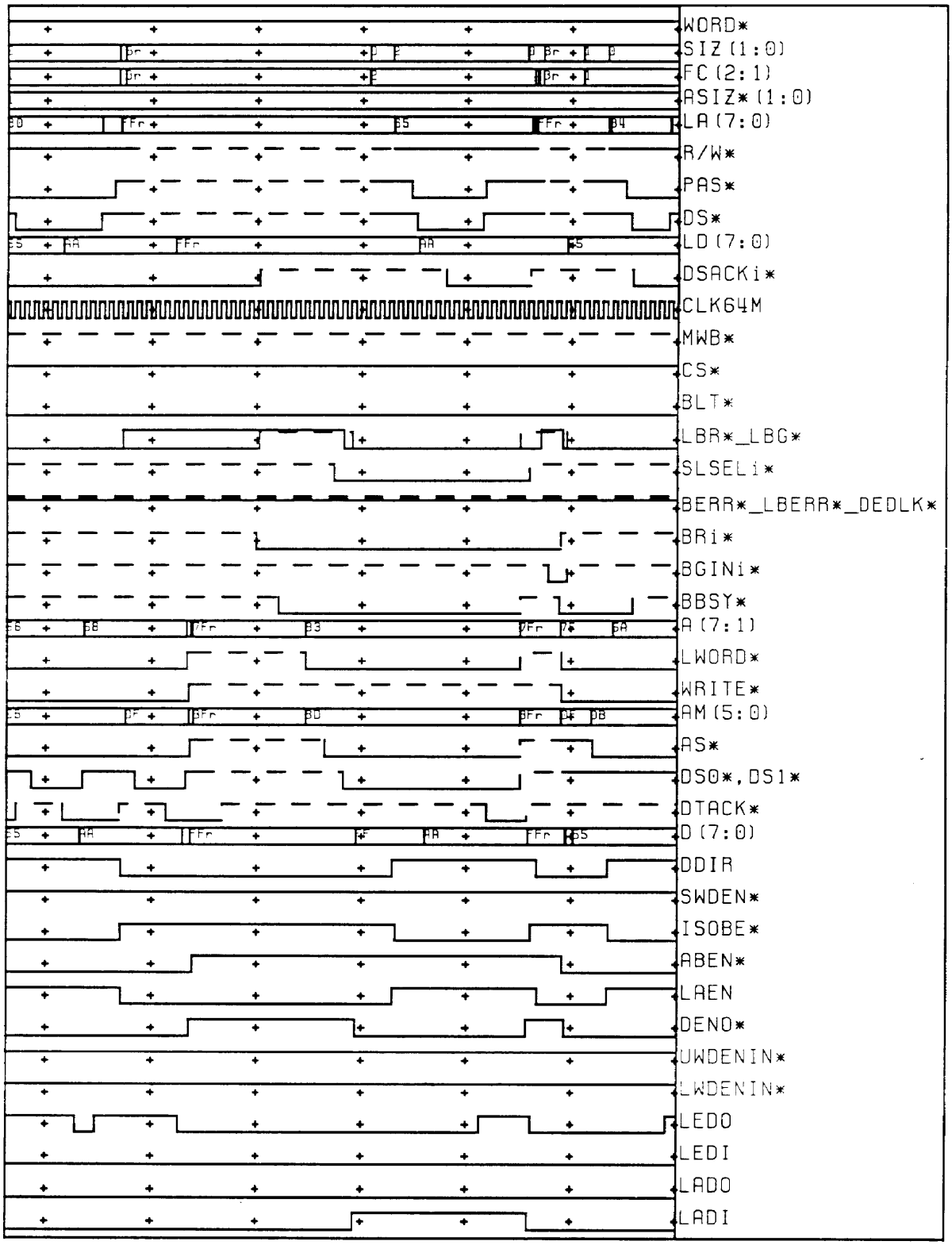

Figure 1-79. Slave Cycle During Interleave Period

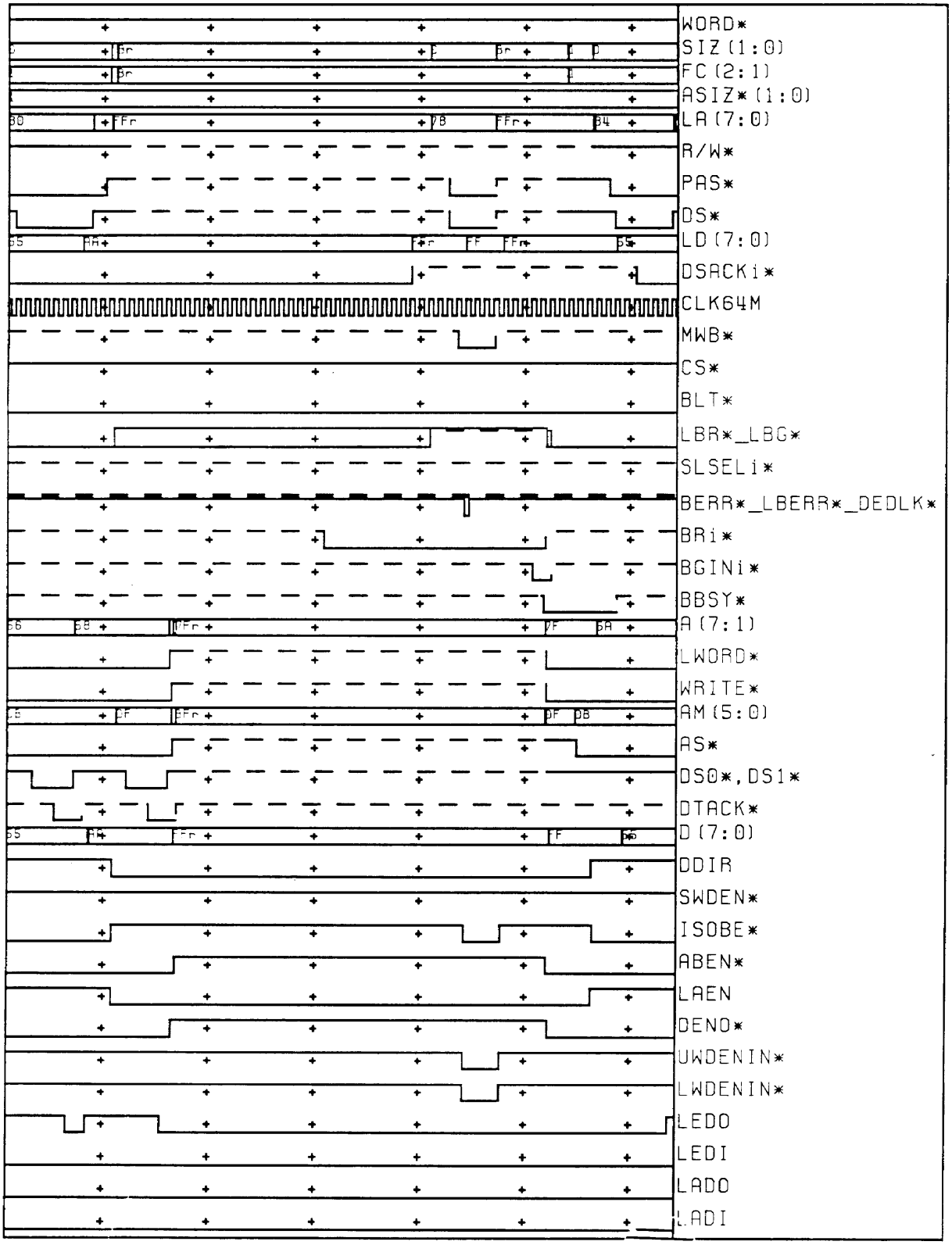

Figure 1-80. Master Cycle Deadlocked During Interleave

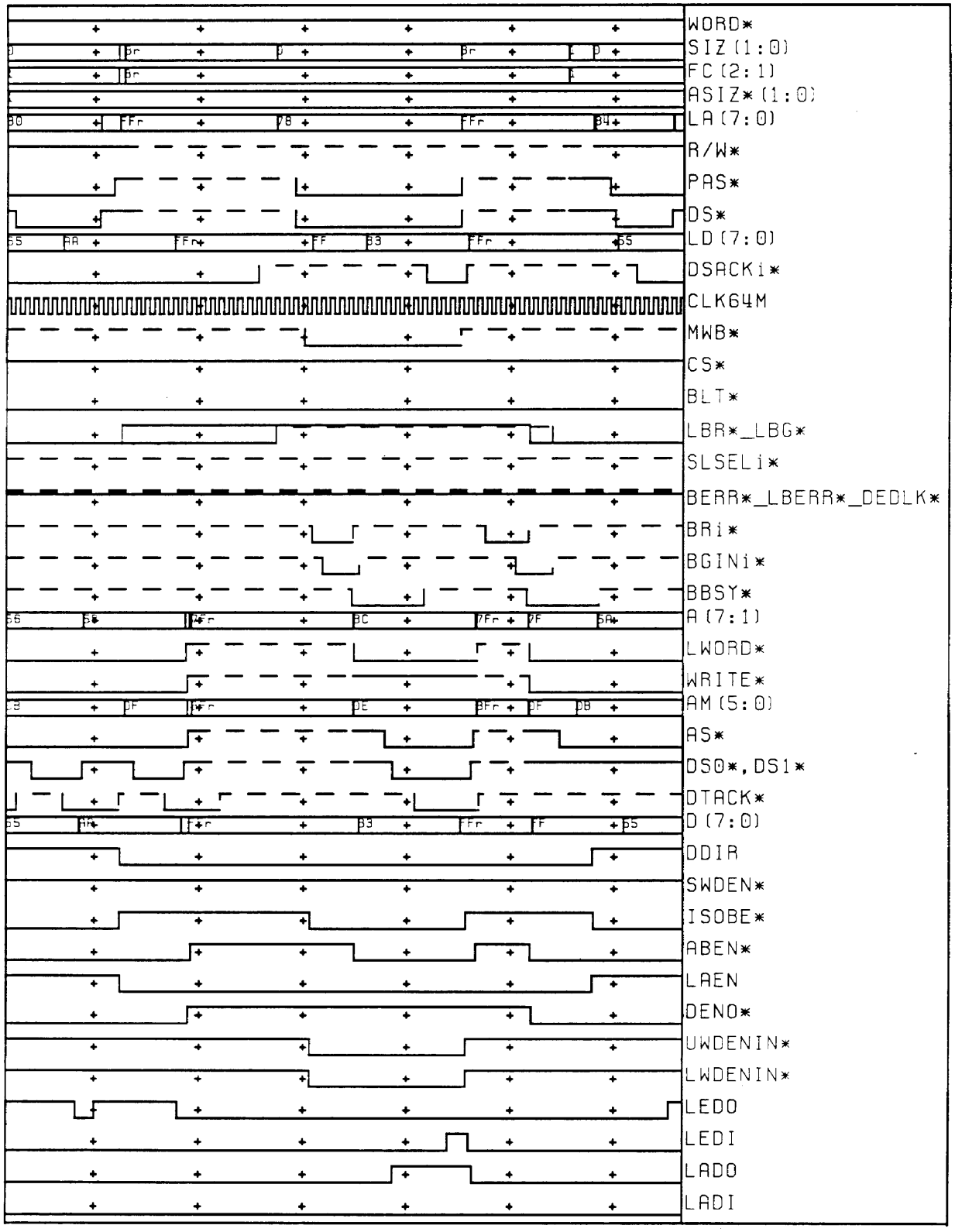

Figure 1-81. Master Cycle During Interleave with Dual-Path Option