1.12

VIC068A Register Map and Descriptions

This chapter describes the VIC068A internal configuration registers. These registers enable and disable various features of the VIC068A. (Refer to the specific sections of this guide for details on specific features.)

Table 1-16 provides information on the various reset states of the VIC068A registers. The following notes should be observed regarding this table:

- An asterisk (*) indicates a bit that is not affected by the particular reset.
- An “X” indicates a bit that is affected by that state of a particular VIC068A pin.
- ICR5 is the VIC068A-version register. Its contents will vary depending on the revision of the device being used.

Unless otherwise specified, the reset status is given in this chapter by the values located in the parentheses by each bit field. The (X/X/X) format indicates the Global/Internal/System reset state of each bit or bit field.

For compatibility with the VIC64, it is recommended that all reserved register bits be written with a 0.

Table 1-16. VIC068A Register Values After Reset Operations

Address (hex)	Name	Description	Global Reset	Internal Reset	System Reset
03	VIICR	VMEbus Interrupter Interrupt Control Register	11111000	11111***	11111***
07–1F	CICR1–7	VMEbus Interrupt Control Registers 1–7	11111000	11111***	11111***
23	DMASR	DMA Status Register	11111000	11111***	11111***
27–3F	LICR1–7	Local Interrupt Control Registers 1–7	1000X000	1***X***	1***X***
43	ICGSICR	ICGS Interrupt Control Register	11111000	11111***	11111***
47	ICMSICR	ICMS Interrupt Control Register	11111000	11111***	11111***
4B	EGICR	Error Group Interrupt Control Register	1111X000	1111X***	1111X***
4F	ICGSVBR	ICGS Vector Base Register	000011XX	000011XX	000011XX
53	ICMSVBR	ICMS Vector Base Register	000011XX	000011XX	000011XX
57	LIVBR	Local Interrupt Vector Base Register	00001XXX	00001XXX	00001XXX
5B	EGIVBR	Error Group Interrupt Vector Base Register	00001XXX	00001XXX	00001XXX
5F	ICSR	Interprocessor Communications Switch Register	00000000	****0000	00000000
63–73	ICR0-4	Interprocessor Communications Registers 0–4	00000000	00000000	00000000
77	ICR5	Interprocessor Communications Register 5	Version	Version	Version
7B	ICR6	Interprocessor Communications Register 6	X11111XX	X1111111	X1111110
7F	ICR7	Interprocessor Communications Register 7	00X00000	*0XX****	00X00000

Table 1-16. VIC068A Register Values After Reset Operations (continued)

Address (hex)	Name	Description	Global Reset	Internal Reset	System Reset
83	VIRSR	VMEbus Interrupt Request Status Register	00000000	*******0	00000000
87–9F	VIVBR1–7	VMEbus Interrupt Vector Base Registers 1–7	00001111	********	00001111
A3	TTR	Transfer Timeout Register	01101000	01101000	01101000
A7	LBTR	Local Bus Timing Register	00000000	********	********
AB	BTDR	Block Transfer Definition Register	11110000	11110000	11110000
AF	ICR	Interface Configuration Register	0000000X	0000000X	0000000X
B3	ARCR	Arbiter/Requester Configuration Register	01100000	011*0000	011*0000
B7	AMSR	Address Modifier Source Register	00000000	00000000	00000000
BB	BESR	Bus Error Status Register	X0000000	X0000000	X0000000
BF	DMASR	DMA Status Register	00000000	00000000	00000000
C3	SS0CR0	Slave Select 0 Control Register 0	00000000	00******	00******
C7	SS0CR1	Slave Select 0 Control Register 1	00000000	********	********
CB	SS1CR0	Slave Select 1 Control Register 0	00000000	00******	00******
CF	SS1CR1	Slave Select 1 Control Register 1	00000000	********	********
D3	RCR	Release Control Register	00000000	00000000	00000000
D7	BTCR	Block Transfer Control Register	00000000	00000000	00000000
DB	BTLR1	Block Transfer Length Register 1	00000000	00000000	00000000
DF	BTLR0	Block Transfer Length Register 0	00000000	00000000	00000000
E3	SRR	System Reset Register	11111111	11111111	11111111
EB-FF		Reserved Locations	11111111	11111111	11111111

VMEbus Interrupter Interrupt Control Register

Name: VIICR

Address: $03

Description: Provides enabling and IPL level encoding for the local interrupt issued when a VMEbus interrupt is acknowledged.

Bits 2–0: (0/*/*) IPL value. Value is inverted and driven onto the IPL lines when an interrupt is acknowledged

Bits 6–3: (1/1/1) Undefined/Reserved. Bits will read as 1s.

Bit 7: (1/1/1) VMEbus interrupt mask. When clear, the VIC068A signals a local interrupt at the acknowledgment of a previously issued VMEbus interrupt. When set, the VIC068A will not issue a local interrupt.

VMEbus Interrupt Control Registers 1–7

Name:	VICR1–7
Addresses: For interrupt:	$07, $0B, $0F, $13, $17, $1B, $1F 1 2 3 4 5 6 7
Description:	Provides enabling of the VIC068A as VMEbus interrupt handler for any or all of the VMEbus interrupts. Seven registers exist to provide unique masking and IPL values for the seven VMEbus interrupts.
Bits 2–0: (0/*/*)	IPL value. Value is inverted and driven onto the IPL signals when a VMEbus interrupt is acknowledged.
Bits 6–3: (1/1/1)	Undefined/Reserved. Bits will read as 1s.
Bit 7: (1/1/1)	VMEbus interrupt mask. When clear, the VIC068A acts as a VMEbus interrupt handler by signaling a local interrupt at the specified IPL level. When set, the VIC068A does not handle the VMEbus interrupt and no local interrupt is issued.

DMA Status Interrupt Control Register

Name:	DMASICR
Address:	$23
Description:	Provides enabling and IPL-level encoding for the DMA-complete interrupt issued by the VIC068A when any VIC068A local DMA operation completes (successfully or unsuccessfully).
Bits 2–0: (0/*/*)	IPL value. Value is inverted and driven onto the IPL lines when interrupt is acknowledged.
Bits 6–3: (1/1/1)	Undefined/Reserved. Bits will read as 1s.
Bit 7: (1/1/1)	DMA status interrupt mask. When clear, the VIC068A signals a local interrupt at the completion of any VIC068A local DMA operation. When set, the VIC068A will not issue a local interrupt.

Local Interrupt Control Registers 1–7

Name:	LICR1–7
Address: For LIRQ:	$27, $2B, $2F, $33, $37, $3B, $3F 1 2 3 4 5 6 7
Description:	Provides enabling, IPL level, and control of local interrupts 1–7 (LIRQ1–7*).
Bits 2–0: (0/*/*)	IPL value. Value is inverted and driven onto the IPL lines when a local interrupt is presented on the LIRQ1–7* signals and bit 7 of this register is clear (enabled).
Bit 3: (X/X/X)	LIRQ1–7* voltage state. A cleared bit indicates the LIRQ1–7* signal is asserted at the VIC068A.

Local Interrupt Control Registers 1–7 (continued)

Bit 4: (0/*/*)	Autovector enable. When set, the VIC068A will supply the interrupt status/ID vector for the local interrupt acknowledge cycle. When cleared, the VIC068A will assert the LIACK0* signal to indicate an 68K “autovector” condition or that the interrupting source should provide the Status/ID vector to the processor.
Bit 5: (0/*/*)	Edge/level enable. When cleared, the VIC068A responds to the LIRQ1-7* as a level-sensitive interrupt. When set, the VIC068A responds to LIRQ1–7* as an edge-sensitive interrupt.
Bit 6: (0/*/*)	Polarity set. When set, the VIC068A responds to interrupts as active High if bit 5 is clear (level sensitive) or on a rising edge if bit 5 is set (edge sensitive). When clear, the VIC068A responds to interrupts as active Low if bit 5 is clear (level sensitive) or on a falling edge if bit 5 is set (edge sensitive).
Bit 7: (1/1/1)	Local interrupt mask. When clear, the VIC068A is enabled to handle the corresponding local interrupt asserted on the LIRQ1–7* signals.

ICGS Interrupt Control Register

Name:	ICGSICR
Address:	$43
Description:	Provides enabling and IPL encoding for the four global switch interrupts.
Bits 2–0: (0/*/*)	IPL Value. Value is inverted and driven onto the IPL signals when a global switch is acknowledged.
Bit 3: (1/1/1)	Undefined/Reserved. Bit will read as a 1.
Bit 4: (1/1/1)	ICGS0 mask. When clear, the VIC068A will issue and handle a local interrupt when global switch 0 is set.
Bit 5: (1/1/1)	ICGS1 mask. When clear, the VIC068A will issue and handle a local interrupt when global switch 1 is set.
Bit 6: (1/1/1)	ICGS2 mask. When clear, the VIC068A will issue and handle a local interrupt when global switch 2 is set.
Bit 7: (1/1/1)	ICGS3 mask. When clear, the VIC068A will issue and handle a local interrupt when global switch 3 is set.

ICMS Interrupt Control Register

Name:	ICMSICR
Address:	$47
Description:	Provides enabling and IPL encoding for the four module switch interrupts.

ICMS Interrupt Control Register (continued)

Bits 2–0: (0/*/*)	IPL Value. Value is inverted and driven onto the IPL signals when a module switch is acknowledged.
Bit 3: (1/1/1)	Undefined/Reserved. Bit will read as a 1.
Bit 4: (1/1/1)	ICMS0 mask. When clear, the VIC068A will issue and handle a local interrupt when module switch 0 is set.
Bit 5: (1/1/1)	ICMS1 mask. When clear, the VIC068A will issue and handle a local interrupt when module switch 1 is set.
Bit 6: (1/1/1)	ICMS2 mask. When clear, the VIC068A will issue and handle a local interrupt when module switch 2 is set.
Bit 7: (1/1/1)	ICMS3 mask. When clear, the VIC068A will issue and handle a local interrupt when module switch 3 is set.

Error-Group Interrupt Control Register

Name:	EGICR
Address:	$4B
Description:	Provides enabling and IPL encoding for the error group interrupts.
Bits 2–0: (0/*/*)	IPL Value. Value is inverted and driven onto the IPL signals when an error group interrupt is acknowledged.
Bit 3: (X/X/X)	SYSFAIL* asserted. This bit is set whenever SYSFAIL* is detected asserted.
Bit 4: (1/1/1)	SYSFAIL* interrupt mask. When clear, the VIC068A generates a local interrupt when SYSFAIL* is asserted.
Bit 5: (1/1/1)	Arbitration timeout interrupt mask. When clear, the VIC068A generates a local interrupt when an arbitration timeout has occurred.
Bit 6: (1/1/1)	Write post fail interrupt mask. When clear, the VIC068A generates a local interrupt when a write post operation has failed due to a bus error. For master write posts, an assertion of BERR* will trigger an interrupt. For slave write posts, an assertion of LBERR* will trigger an interrupt.
Bit 7: (1/1/1)	AC Fail interrupt mask. When clear, the VIC068A generates a local interrupt when ACFAIL* is detected as asserted.

ICGS Interrupt Vector Base Register

Name:	ICGSIVBR
Address:	$4F
Description:	Provides the status/ID vector for the global switch interrupts. This register must be written after any VIC068A reset to enable identification encoding for bits 1-0.
Bits 1–0: (X/X/X)	Global switch number (read-only). This value indicates which global switch is pending during a global switch interrupt acknowledge cycle. These bits are used with bits 7–2 to provide a unique status/ID vector for each global switch. The numeric value of this field indicates the switch number. These bits are valid only during the interrupt acknowledge cycle.
Bits 7–2:	Status/ID. These bits are user-definable and are used with bits 1–0 to provide a unique global switch interrupt status/ID vector.

ICMS Interrupt Vector Base Register

Name:	ICMSIVBR
Address:	$53
Description:	Provides the status/ID vector for the module switch interrupts. This register must be written after any VIC068A reset to enable identification encoding for bits 1-0. This register is reset to $F0 during any VIC068A reset.
Bits 1–0: (X/X/X)	Module switch number (read-only). This value indicates which module switch is pending during a module switch interrupt acknowledge cycle. These bits are used with bits 7–2 to provide a unique status/ID vector for each module switch. The numeric value of this field indicates the switch number. These bits are valid only during the interrupt acknowledge cycle.
Bits 7–2:	Status/ID. These bits are user-definable and are used with bits 1–0 to provide a unique module switch interrupt status/ID vector.

Local Interrupt Vector Base Register

Name:	LIVBR
Address:	$57
Description:	Provides the status/ID vector for the local interrupts. This register must be written after any VIC068A reset to enable identification encoding for bits 2–0. This register is reset to $F0 during any VIC068A reset.

Local Interrupt Vector Base Register (continued)

Bits 2–0: (X/X/X) Local Interrupt number (read-only). This value indicates which local interrupt is pending during a local interrupt acknowledge cycle. These bits are used with bits 7–3 to provide a unique status/ID vector for each local interrupt. The numeric value of this field indicates the local interrupt number. These bits are valid only during the interrupt acknowledge cycle.

Bits 7–3: Status/ID. These bits are user-definable and are used with bits 1–0 to provide a unique local interrupt status/ID vector.

Error Group Interrupt Vector Base Register

Name: EGIVBR

Address: $5B

Description: Provides the status/ID vector for the error group interrupts. This register must be written after any VIC068A reset to enable identification encoding for bits 2–0. This register is reset to $F0 during any VIC068A reset.

Bits 2–0: (X/X/X) Error/Status Group Interrupt number (read-only). This value indicates which group interrupt is pending during the interrupt acknowledge cycle. These bits are used with bits 7–3 to provide a unique status/ID vector for each error group interrupt. These bits are valid only during the interrupt acknowledge cycle.

Bits 2–0	*Error/Status Interrupt*
0 0 0	ACFAIL* asserted
0 0 1	Write post failed
0 1 0	Arbitration timeout
0 1 1	SYSFAIL* asserted
1 0 0	VMEbus Interrupter interrupt acknowledge
1 0 1	DMA complete

Bits 7–3: Status/ID. These bits are user-definable and are used with bits 1-0 to provide a unique interrupt status/ID vector.

Interprocessor Communications Switch Register

Name: ICFSR

Address: $5F

Description: Provides setting, clearing, and monitoring of the interprocessor switch interrupts via the local bus. If the switch interrupts are enabled, setting these bits (more precisely, a clear-to-set transition) causes a local interrupt to occur in the same way as if the switch was set over the VMEbus.

Bits 3–0: (0/0/0) Module switches. Bits 0, 1, 2, and 3 correspond to ICMSs 0, 1, 2, and 3 respectively.

Bits 7–4: (0/*/0) Global switches. Bits 4, 5, 6, and 7 correspond to ICGSs 0, 1, 2, and 3 respectively.

Interprocessor Communication Registers 0–4

Name:	ICR0–4
Addresses: For registers:	$63, $67, $6B, $6F, $73 0 1 2 3 4
Description:	These are general-purpose read/write registers that can be accessed from either the local bus or the VMEbus. The addresses listed above are the local addresses. See Chapter 1.8 for details on accessing these registers from the VMEbus.
Bits 7–0: (0/0/0)	Data field.

Interprocessor Communication Register 5

Name:	ICR5
Address:	$77
Description:	This register provides the VIC068A version/revision number. The first VIC068A device contains a value of $F1. Contact your local Cypress Semiconductor sales office for current VIC068A revision status. The address listed above is the local address. See Chapter 1.8 for details on accessing this register from the VMEbus.
Bits 7–0:	VIC068A version/revision (read-only).

Interprocessor Communication Register 6

Name:	ICR6
Address:	$7B
Description:	This register provides local or remote reset and HALT*. The address listed above is the local address. See Chapter 1.8 for details on accessing this register from the VMEbus.

Interprocessor Communication Register 6 (continued)

Bits 1–0: Reset/HALT* status (read-only from VMEbus). These bits provide reset/HALT* status of the VIC068A and local resources according to the following table:

Bits 1–0	Reset/HALT* Status.
0 1	HALT* has been asserted longer than 6 ms by a source other then the VIC068A. These bits may both be reset by the local CPU to indicate local resources are running and operational.
1 0	The VIC068A has performed a local reset function and the VIC068A is not the system controller. These bits may both be reset by the local CPU to indicate local resources are running and operational.
1 1	Indicates that the CPU has just been released from a system reset.
0 0	Local resources are running and operational. This pattern must be written by the local CPU after a reset condition to indicate that local resources are running and operational.

Bits 5–2: (1/1/1) Undefined/Reserved. Bits will read as 1s.

Bit 6: (1/1/1) IRESET* and HALT* status (read-only from VMEbus). This bit is set upon assertion of IRESET*, and/or HALT*. It is set whether HALT* is asserted by external sources or by the VIC068A. SYSFAIL* is asserted when this bit is set if the SYSFAIL* mask bit (ICR7, bit 7) is cleared.

Bit 7: (X/X/X) IRESET* status (read-only). On a VMEbus read, this bit indicates that the VIC068A is in a reset state. On a local bus read, this bit is set whenever ACFAIL* is asserted.

Interprocessor Communication Register 7

Name: ICR7

Address: $7F

Description: This register provides semaphores to the five general-purpose interprocessor communication registers (ICR4–0). The remaining bits indicate VMEbus master status, generate HALT* and RESET*, and mask SYSRESET*. The address listed above is the local address. See Chapter 1.8 for details on accessing this register from the VMEbus.

Bits 4–0: (0/*/0) ICR4–0 semaphores. These bits provide semaphores to the five interprocessor communication registers ICR4–0 respectively. Each bit is set when the corresponding ICR is written. These bits must be cleared by the user (i.e., they are not cleared automatically). These bits can be read or written from the local bus or the VMEbus.

Interprocessor Communication Register 7 (continued)

Bit 5: (X/X/X)	VMEbus master status (read-only). This bit is set whenever the VIC068A is the VMEbus master, and the VIC068A is asserting AS*. This bit is not set when the VIC068A is VMEbus master to an idle bus in ROR and BCAP release modes. Bit 7 of the BESR may be used to indicate that the VIC068A is VMEbus master when AS* is not asserted.
Bit 6: (0/0/0)	HALT* and RESET* control. This bit may be used to assert the HALT* and RESET* pins via software. Whenever this bit is set, the VIC068A asserts HALT* and RESET* until this bit is cleared or any reset occurs.
Bit 7: (0/*/0)	SYSFAIL* mask. When set, the VIC068A is prohibited from asserting SYSFAIL* in response to bit 6 of ICR6 being set (which, by default, is set after any reset). This bit must be written after resetting the VIC068A to deassert SYSFAIL*.

VMEbus Interrupt Request/Status Register

Name:	VIRSR
Address:	$83
Description:	This register provides status and control of the VMEbus interrupts 7–1.
Bit 0: (0/0/0)	Register enable/disable. This bit provides enabling and disabling for the remainder of this register.
Bits 7–1: (0/0/0)	VMEbus interrupt switches. Setting any of these bits asserts the VMEbus IRQi* signals corresponding to the bit positions, if bit 0 is set during the write. These bits are cleared automatically when the interrupt is serviced.

VMEbus Interrupt Vector Base Registers 1–7

Name:	VIVBR
Address: for IRQ:	$87, $8B, $8F, $93, $97, $9B, $9F 1 2 3 4 5 6 7
Description:	Provides the status/ID vector for the VMEbus interrupts.
Bits 7–0:	Status/ID Vector. These bits provide the status/ID vector for VMEbus interrupt acknowledge cycles. Address $87 corresponds to IRQ1*. These bits are set to a value of $0F for global and system resets and are unchanged by internal resets.

Transfer Timeout Register

Name:	TTR
Address:	$A3
Description:	Provides control of the local and VMEbus timeout timers.

Transfer Timeout Register (continued)

Bit 0: (0/0/0) Include VMEbus acquisition. When set, the local bus timer will include waiting for VMEbus acquisition. When clear, the local bus timer will stop and reset when the VMEbus is requested.

Bit 1: (0/0/0) Arbitration timeout. When set, the VIC068A as VMEbus arbiter has detected a VMEbus arbitration timeout. This is only used when configured as the VMEbus system controller (SCON* asserted).

Bits 4–2: Local bus timeout period. Defines the local bus timeout.

Bit 4	*Bit 3*	*Bit 2*	*Local Bus Timeout (ms)*
0	0	0	4
0	0	1	16
0	1	0	32 (default)
0	1	1	64
1	0	0	128
1	0	1	256
1	1	0	512
1	1	1	Infinite (timer disabled)

Bits 7–5: VMEbus timeout period. Defines the VMEbus timeout.

Bit 7	*Bit 6*	*Bit 5*	*VMEbus Timeout (ms)*
0	0	0	4
0	0	1	16
0	1	0	32 (default)
0	1	1	64
1	0	0	128
1	0	1	256
1	1	0	512
1	1	1	Infinite (timer disabled)

Local Bus Timing Register

Name: LBTR

Address: $A7

Description: Provides timing control for PAS* and DS* signals when the VIC068A is local bus master. In the following descriptions, *n* is the binary value specified in the bit fields, and *T* is one CLK64M clock period. Clock latency may add one additional clock period to these times.

Bits 3–0: (0/*/*) Minimum PAS* asserted time. This field specifies the *minimum* asserted time for the PAS* signal whenever the VIC068A is the local bus master. The time is specified by (n + 2)T. The actual asserted time depends on a number of factors including local and VMEbus acknowledge timing.

Local Bus Timing Register

Bit 4: (0/*/*)	Minimum DS* deasserted time. This field specifies the *minimum* deasserted time for the DS* signal whenever the VIC068A is the local bus master. A time of 1T is selected when this bit is clear; 2T is selected when this bit is set.
Bits 7–5: (0/*/*)	Minimum PAS* deasserted time. This field specifies the *minimum* deasserted time for the PAS* signal whenever the VIC068A is the local bus master. The time is specified by (n + 1)T.

Block Transfer Definition Register

Name:	BTDR
Address:	$AB
Description:	Configures master block transfers (both MOVEM and block transfers with local DMA) for boundary crossings, dual-path, and user-defined address modifiers. See Chapter 1.10 for more details on implementing these features.
Bit 0: (0/0/0)	Dual-path enable. When set, the VIC068A is enabled with the dual-path feature during master block transfers with local DMA. External logic is required when this option is enabled.
Bit 1: (0/0/0)	AMSR Enable. When set, the VIC068A will issue the AM codes based in the address modifier source register for block transfers. This bit effects the AM codes for block transfers only.
Bit 2: (0/0/0)	When this bit is set, it enables local address 256-byte boundary crossings during DMA block transfer operations. External logic is required to increment latched address lines when this option is enabled.
Bit 3: (0/0/0)	When this bit is set, it enables VMEbus address 256-byte boundary crossings during DMA block transfer operations. External logic is required to increment latched address lines when this option is enabled.
Bit 7–4: (1/1/1)	Undefined/Reserved. Bits will be read as 1s.

Interface Configuration Register

Name:	ICR
Address:	$AF
Description:	Controls various features of the VIC068A including RMCs, deadlock signaling, metastability delays, and the “turbo” feature.
Bit 0: (X/X/X)	SCON* value (read-only). Reads the value of the SCON* pin. When set, the VIC068A is not the VMEbus system controller. When clear, the VIC068A is the VMEbus system controller.

Interface Configuration Register (continued)

Bit 1: (0/0/0) Turbo enable. When set, the VIC068A accelerates VMEbus transfers by reducing selected timings by one CLK64M clock period. VMEbus protocols may be violated when the turbo mode is enabled (see section 1.11.5).

Bit 2: (0/0/0) Metastability interval. When set, the VIC068A adds one additional CLK64M clock period of metastability delay on asynchronous inputs (from 3 CLK64M periods to 4).

Bits 4, 3: (0/0/0) Deadlock signaling. These bits configure deadlock signaling. Bit 4 is used to enable the assertion of HALT* and LBERR* in addition to the DEDLK* signal in deadlock situations. If bit 4 is enabled, bit 3 may be used to prevent the assertion of HALT* for RMC deadlocks.

Bit 4	*Bit 3*	*Deadlock Signaling*
0	X	DEDLK* only (default)
1	0	HALT*, LBERR*, DEDLK*
1	1	HALT*, LBERR*, DEDLK* (HALT* is not asserted for RMC cycles)

Bit 5: (0/0/0) RMC control bit 1. When set, the VIC068A will request the VMEbus whenever the RMC* is asserted independent of the MWB* signal.

Bit 6: (0/0/0) RMC control bit 2. When set, the VMEbus AS* is stretched when RMC* is asserted for VMEbus transfers.

Bit 7: (0/0/0) RMC control bit 3. When set, the VIC068A qualifies the RMC control bits 5 and 6 with the SIZ1/0 signals. If RMC control bits 5 or 6 are set and the first cycle of the RMC transfer is of byte size, the “set” behaviors are not implemented.

Arbiter/Requester Configuration Register

Name: ARCR

Address: $B3

Description: This register provides configuration of the fairness timeout and DRAM refresh features. The VMEbus request level is also configured from this register.

Bits 3–0: (0/0/0) Fairness timer enable. The VMEbus fair requester is enabled in this bit field according to the following table:

Bits 3–0	*Timeout Period/Mode*
$0	Fairness disabled (default)
$F	Timeout disabled
All other patterns	2 μs times number

Bit 4: (0/*/*): DRAM refresh. When set, the VIC068A will perform CAS-before-RAS (DS* before PAS*) refresh functions.

Arbiter/Requester Configuration Register (continued)

Bits 6, 5: VMEbus request level. The VMEbus request level is set according to the following table:

Bit 6	*Bit 5*	*VMEbus Request Level*
0	0	BR0
0	1	BR1
1	0	BR2
1	1	BR3 (default)

Bit 7: (0/0/0) Arbitration mode. When set, the VIC068A performs priority VMEbus arbitration. When clear, the VIC068A performs round-robin arbitration. This bit is only relevant when the VIC068A is configured as the VMEbus system controller (SCON* asserted).

Address Modifier Source Register

Name: AMSR

Address: $B7

Description: This register provides the user-definable address modifiers (AM codes) that can be sourced by the VIC068A for VMEbus master cycles, or used in validating AM codes during VMEbus slave cycles.

Bits 5–0: (0/0/0) Address modifier code. The AM code that is issued during master cycles or used for qualifying slave cycles. This register is used only when enabled for user-defined AM codes. Otherwise, standard VMEbus AM codes are used.

Bit 6: (0/0/0) AM5–3 qualification. When set, the VIC068A uses bits 5–3 in qualifying for slave accesses in addition to the address space size information defined by bits 3 and 2 of the SSiCR0s. This bit is overridden if bits 3 and 2 of the SSiCR0s are both set.

Bit 7: (0/0/0) AM2–0 generation. When set, the VIC068A issues the AM2–0 codes based on the FC2/1 signals. AM5–3 will be issued from bits 5–3 of this register.

Bus Error Status Register

Name: BESR

Address: $BB

Description: This register provides BERR*/LBERR*, self-access, VMEbus mastership, and timeout status. All bits except bit 7 are flags that must be cleared manually by the local processor after being set by status conditions. If these bits are to be used for a specific operation, it is important that they be cleared prior to starting that operation.

Bit 0: (0/0/0) Local timeout during VMEbus acquisition. This bit, when set, indicates that a local bus timeout has occurred during an attempted acquisition of the VMEbus.

Bus Error Status Register (continued)

Bit 1: (0/0/0)	SLSEL1* self-access. This bit is set when the VIC068A is selected by the assertion on the SLSEL1* signal, while operating as VMEbus master.
Bit 2: (0/0/0)	SLSEL0* self-access. This bit is set when the VIC068A is selected by the assertion on the SLSEL0* signal, while operating as VMEbus master.
Bit 3: (0/0/0)	Local bus timeout. This bit, when set, indicates a local bus timeout occurred without qualification.
Bit 4: (0/0/0)	VMEbus timeout. This bit, when set, indicates the VIC068A has signaled a VMEbus timeout. This bit is relevant only if the VIC068A is system controller and the VMEbus timeout is enabled.
Bit 5: (0/0/0)	VMEbus bus error. This bit is set when a VMEbus bus error is signaled (BERR* asserted).
Bit 6: (0/0/0)	Local bus error. This bit is set when a local bus error is signaled by a source other then the VIC068A (LBERR* asserted to the VIC068A).
Bit 7: (X/X/X)	VMEbus mastership. This bit is set whenever the VIC068A is VMEbus master.

DMA Status Register

Name:	DMASR
Address:	$BF
Description:	This register provides status of a VIC068A DMA transfer. This includes the block transfer with local DMA function. Status bits are included to show various BERR* and LBERR* statuses and DMA termination statuses.
Bit 0: (0/0/0)	Block transfer in progress. This bit, when set, indicates an interleaved block transfer is in progress. Once set, this bit is cleared automatically by the VIC068A after completion of the local DMA operation, or by resetting the VIC068A.
Bit 1: (0/0/0)	LBERR* during DMA transfer. This bit, when set, indicates a LBERR* was signaled during a DMA transfer. Once set, this bit must be cleared manually by writing a 0 (zero) to this bit location, or by resetting the VIC068A.
Bit 2: (0/0/0)	BERR* during DMA transfer. This bit, when set, indicates a BERR* was signaled during a DMA transfer. Once set, this bit must be cleared manually by writing a 0 (zero) to this bit location, or by resetting the VIC068A.
Bit 3: (0/0/0)	Local bus error (read-only). This bit is set when a local bus error is signaled by a source other then the VIC068A (LBERR* asserted to the VIC068A). This bit is a read-only copy of bit 6 of the BESR.

DMA Status Register (continued)

Bit 4: (0/0/0)	VMEbus bus error. This bit is set when a VMEbus bus error is signaled (BERR* asserted). This bit is a copy of bit 5 of the BESR.
Bits 5, 6: (1/1/1)	Undefined/Reserved. These bits will be read as 1s.
Bit 7: (0/0/0)	Master write post information stored. This bit is set whenever master write post information is stored.

Slave Select 0 Control Register 0

Name: SS0CR0

Address: $C3

Description: This register provides control of the slave selection 0 facilities of the VIC068A. Enabling of the LIRQ2* timer interrupt is also configured in this register.

Bits 1–0: (0/*/*) Local transfer mode. These bits set the local transfer mode when the VIC068A is local bus master for both slave and master block transfers.

Bit 1	*Bit 0*	*Mode*
0	0	No support is given for slave block transfers on SLSEL0*. The VIC068A will BERR* any attempt to receive a VMEbus block transfer. Master block transfers with local DMA will not function in this mode.
0	1	Emulate single-cycle transfers on the local bus. In this mode, the VIC068A emulates single-cycle transfers when performing slave block transfers and master block transfers with local DMA. By emulating single-cycle transfers, the VIC068A toggles the PAS* for each cycle. DSACKi must toggle for each transfer and not be held asserted.
1	0	Accelerated transfers on the local bus. In this mode, the VIC068A asserts the PAS* signal for the entire slave block transfer and master block transfer with local DMA. The DSACKi* signals should be held asserted in this mode.
1	1	Undefined/Reserved.

Bits 3–2: (0/*/*) Address space configuration. The SLSEL0* address space is configured according to the following table:

Bit 3	*Bit 2*	*Address Space*
0	0	A32 (extended) (default)
0	1	A24 (standard)
1	0	A16 (short)
1	1	User defined, uses AMSR

Slave Select 0 Control Register 0 (continued)

Bit 4:
(0/*/*)

D32 enable. D32 slave operations are enabled for SLSEL0* when this bit is set. This bit has no effect for enabling D32 master accesses. This bit also controls byte-lane switching for D16 Block transfers. When set ISOBE* and SWDEN* alternate states thus alternating which D16 bus data is placed. When clear, only SWDEN* is asserted for D16 block transfers.

Bit 5:
(0/*/*)

Supervisory access. When set, SLSEL0* slave accesses are restricted to supervisory accesses. Other accesses are BERRed. Supervisory accesses are checked with the AM(2) signal.

Bits 7–6:
(0/0/0)

Periodic interrupt timer enable. These bits enable and determine the frequency of the periodic LIRQ2* interrupt. If the VIC068A is to handle this local interrupt, LICR2 must be enabled. The frequencies for this interrupt are given below:

Bit 7	*Bit 6*	*Timer Mode*
0	0	Timer disabled (default)
0	1	50-Hz output on LIRQ2*
1	0	1000-Hz output on LIRQ2*
1	1	100-Hz output on LIRQ2*

Slave Select 0 Control Register 1

Name: SS0CR1

Address: $C7

Description: This register provides the various access and acquisition timings for slave transfers and slave block transfers for SLSEL0* in addition to data acquisition timing for master block transfers with local DMA.

Slave Select 0 Control Register 1 (continued)

Bits 3–0: (0/*/*) Timing field 0. This bit field establishes the following data access/acquisition timings:

- single-cycle slave access timing for SLSEL0* (SAT)
- first cycle of a slave block transfer for SLSEL0* (SBAT0)
- first cycle of a master block transfer with local DMA (MBAT0)

The delays are programmed in multiples of the CLK64M clock period according to the following table

Bit 3	*Bit 2*	*Bit 1*	*Bit 0*	*CLK64M Clock Period Delay*
0	0	0	0	0
0	0	0	1	2.0
0	0	1	0	2.5
0	0	1	1	3.0
0	1	0	0	3.5
0	1	0	1	4.0
0	1	1	0	4.5
0	1	1	1	5.0
1	0	0	0	5.5
1	0	0	1	6.0
1	0	1	0	6.5
1	0	1	1	7.0
1	1	0	0	7.5
1	1	0	1	8.0
1	1	1	0	8.5
1	1	1	1	9.0

Slave Select 0 Control Register 1 (continued)

Bits 7–4: (0/*/*) Timing Field 1. This bit field establishes the following data access/ acquisition timings:

- second and subsequent cycle of a slave block transfer for SLSEL0* (SBAT1)
- second and subsequent cycle of a master block transfer with local DMA (MBAT1)

The delays are programmed in multiples of the CLK64M clock period according to the following table:

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*CLK64M Clock Period Delay*
0	0	0	0	0
0	0	0	1	2.0
0	0	1	0	2.5
0	0	1	1	3.0
0	1	0	0	3.5
0	1	0	1	4.0
0	1	1	0	4.5
0	1	1	1	5.0
1	0	0	0	5.5
1	0	0	1	6.0
1	0	1	0	6.5
1	0	1	1	7.0
1	1	0	0	7.5
1	1	0	1	8.0
1	1	1	0	8.5
1	1	1	1	9.0

Slave Select 1 Control Register 0

Name: SS1CR0

Address: $CB

Description: This register provides control of the slave selection 1 facilities of the VIC068A. Master and slave write posting is enabled in this register as well.

Slave Select 1 Control Register 0 (continued)

Bits 1–0: 0/*/*
Local Transfer Mode. These bits set the local transfer mode when the VIC068A is local bus master for both slave and master block transfers.

Bit 1	*Bit 0*	*Mode*
0	0	No support is given for slave block transfers on SLSEL1*. The VIC068A will BERR* any attempt to receive a VMEbus block transfer.
0	1	Emulate single-cycle transfers on the local bus. In this mode, the VIC068A emulates single-cycle transfers when performing slave block transfers. By emulating single-cycle transfers, the VIC068A toggles PAS* for each cycle. DSACKi* must toggle for each transfer and not be held asserted.
1	0	Accelerate transfers on the local bus. In this mode, the VIC068A asserts PAS* for the entire slave block transfer. The DSACKi* signals should be held asserted in this mode.
1	1	Undefined/Reserved.

Bits 3–2: (0/*/*)
Address Space Configuration. The SLSEL1* address space is configured according to the following table:

Bit 3	*Bit 2*	*Address Space*
0	0	A32 (extended)
0	1	A24 (standard)
1	0	A16 (short)
1	1	User defined, uses AMSR

Bit 4: (0/*/*)
D32 enable. D32 slave operations are enabled for SLSEL1* when this bit is set. This bit has no effect for enabling D32 master accesses.

Bit 5: (0/*/*)
Supervisory access. When set, SLSEL1* slave accesses are restricted to supervisory accesses. Other accesses are BERRed. Supervisory accesses are checked with the AM(2) signal.

Bit 6: (0/0/0)
Master write post enable. When set, master write posting is enabled.

Bit 7: (0/0/0)
Slave write post enable. When set, slave write posting is enabled.

Slave Select 1 Control Register 1

Name: SS1CR1

Address: $CF

Description: This register provides the various access and acquisition timings for slave transfers and slave block transfers for SLSEL1*.

Slave Select 1 Control Register 1 (continued)

Bits 3–0: (0/*/*)

Timing field 0. This bit field establishes the following data access/acquisition timings:

- single-cycle slave access timing for SLSEL1* (SAT)
- first cycle of a slave block transfer for SLSEL1* (SBAT0)

The delays are programmed in multiples of the CLK64M clock period according to the following table:

Bit 3	*Bit 2*	*Bit 1*	*Bit 0*	*CLK64M Clock Period Delay*
0	0	0	0	0
0	0	0	1	2.0
0	0	1	0	2.5
0	0	1	1	3.0
0	1	0	0	3.5
0	1	0	1	4.0
0	1	1	0	4.5
0	1	1	1	5.0
1	0	0	0	5.5
1	0	0	1	6.0
1	0	1	0	6.5
1	0	1	1	7.0
1	1	0	0	7.5
1	1	0	1	8.0
1	1	1	0	8.5
1	1	1	1	9.0

Slave Select 1 Control Register 1 (continued)

Bits 7–4: (0/*/*) Timing field 1. This bit field establishes the following data access/acquisition timing:

- second and subsequent cycle of a slave block transfer for SLSEL1* (SBAT1)

The delays are programmed in multiples of the CLK64M clock period according to the following tables:

Bit 7	*Bit 6*	*Bit 5*	*Bit 4*	*CLK64M Clock Period Delay*
0	0	0	0	0
0	0	0	1	2.0
0	0	1	0	2.5
0	0	1	1	3.0
0	1	0	0	3.5
0	1	0	1	4.0
0	1	1	0	4.5
0	1	1	1	5.0
1	0	0	0	5.5
1	0	0	1	6.0
1	0	1	0	6.5
1	0	1	1	7.0
1	1	0	0	7.5
1	1	0	1	8.0
1	1	1	0	8.5
1	1	1	1	9.0

Release Control Register

Name: RCR

Address: $D3

Description: This register configures the VMEbus release mode. The burst count for block transfers with local DMA is also configured in the RCR.

Bits 5-0: (0/0/0) Block transfer burst length. The burst length for both MOVEM block transfers and block transfers with local DMA are configured in this bit field. The value indicates the number of cycles per block transfer (not the number of bytes). A value of 0 in this bit field indicates the maximum 64 cycles per burst. All other values correspond directly to the burst count.

Bits 7,6: (0/0/0) Release mode. This bit field defines the release mode used by the VIC068A when releasing the VMEbus after the completion of a VMEbus transfer.

Bit 7	*Bit 6*	*Release Mode*
0	0	ROR—Release on Request (default)
0	1	RWD—Release When Done
1	0	ROC—Release on BCLR* assertion
1	1	BCAP—VMEbus Capture and Hold

Block Transfer Control Register

Name:	BTCR
Address:	$D7
Description:	The BTCR provides control of the VIC068A block transfers. The local interleave periods and data direction are defined in this register. The enabling bits for all of the VIC068A's block transfer modes are located here as well. These enabling bits are mutually exclusive and more than one should not be set at the same time.
Bits 3–0: (0/0/0)	Interleave period. The interleave period for block transfers is defined here. The interleave period is 250 ns times the value programmed in this bit field.
Bit 4: (0/0/0)	Data direction. This bit defines the direction of a block transfer with local DMA (MOVEM data direction determined by the R/W* signal). When set, VMEbus block reads occur. When clear, VMEbus block writes occur.
Bit 5: (0/0/0)	MOVEM enable. When set, MOVEM transfers are enabled. After this bit is set, the next VMEbus transfer is treated as the start of a VMEbus block transfer. Clearing this bit concludes a MOVEM block transfer in progress. It is important to set this bit immediately before and clear this bit immediately after the actual MOVEM transfer.
Bit 6: (0/0/0)	Block transfer with local DMA enable. When set, block transfers with local DMA are enabled. After this bit is set, the next assertion of MWB* is considered the initiation cycle of a VMEbus block transfer with local DMA. It is important to set this bit immediately before and clear this bit immediately after the actual block transfer.
Bit 7: (0/0/0)	Special purpose. For normal operation set this bit to 0.

Block Transfer Length Registers 1–0

Name:	BTLR1–0
Addresses:	$DB (BTLR1), $DF (BTLR0)
Description:	These registers configure the byte count for block transfers with local DMA. BTLR1 is considered the most significant byte and BTLR0 the least significant. Bit 0 of BTLR0 must never be set because this implies at least one 8-bit transfer is required to complete the block transfer. Only D16 and D32 block transfers are supported. If bit 0 of BTLR0 is set, the block transfer length is ignored and only one burst is performed.
Bits 7–0: (0/0/0)	Block transfer length. Defines the block transfer length in bytes. BTLR1 contains the most significant 8 bits of the length, and BTLR0 the least.

System Reset Register

Name:	SRR
Address:	$E3
Description:	The system reset register provides the means to perform a VMEbus system reset (SYSRESET* asserted). Writing a value of $F0 causes this function to occur. A system reset is also performed within the VIC068A.
Bits 7–0: (1/1/1)	System reset field. Writing this bit field with a value of $F0 causes SYSRESET* to be asserted for a minimum of 200 ms and a system reset to be performed within the VIC068A.