1.11

Miscellaneous Features

This chapter describes additional miscellaneous features of the VIC068A.

1.11.1 Resetting the VIC068A

The VIC068A is reset by any of three distinct reset conditions. These reset conditions are initiated by asserting various inputs or, in the case of a system reset, writing a VIC068A register. Since it is possible for more than one reset condition to be present simultaneously, the resets have the following priority:

1. global reset

2. internal reset

3. system reset

Upon completion of a VIC068A reset, ICR6[6] is set, thus causing SYSFAIL* to be asserted. To remove the SYSFAIL* set ICR7[7], which is cleared by a global or power-up reset.

IMPORTANT

It is vital to the proper operation of the VIC068A that a global reset be performed at power-up. It is not necessary to wait for a system reset (caused by an assertion of SYSRESET* on the VMEbus) to complete before asserting a global reset. See section 1.11.1.2.

1.11.1.1 Internal Reset

The internal reset is the most common and easiest to implement of the VIC068A resets. This resets all the VIC068A internal circuitry and selected register bit fields. This reset is typically used as a push-button reset after power-up.

The internal reset is initiated by asserting the IRESET* signal for a minimum of 20 ns. Immediately after the assertion of IRESET*, the VIC068A asserts the LBR* signal. The VIC068A then waits 1 ms for the assertion of LBG*. If LBG* is asserted within the 1-μs timeout, the VIC068A asserts HALT* and RESET* immediately. If LBG* is not asserted within this timeout period, the VIC068A asserts HALT* and RESET* as if LBG* had been received. The VIC068A attempts this reset handshaking sequence to provide an orderly reset of local resources.

After the VIC068A asserts HALT* and RESET*, the VIC068A deasserts LBR*, places all three-state outputs to a high-Z state, and begins a 200-ms timeout period. If IRESET* is

still asserted after this timeout expires, the VIC068A begins an additional 200-ms timeout. The reset does not complete until the 200-ms timeout expires after IRESET* is deasserted.

If the VIC068A is the VMEbus system controller, the VIC068A also asserts SYSRESET* with the RESET* and HALT* signals.

After the conclusion of an internal reset, the HALT* and RESET* signals (and SYSRESET* if VMEbus is system controller) are deasserted and all outputs are brought to their quiescent states.

1.11.1.2 Global Reset

The global reset provides the most complete reset to the VIC068A. This resets all VIC068A internal circuitry and all register bit fields to predefined states. A global reset must be issued at power-up to insure proper operation of the VIC068A.

The global reset is initiated by asserting the IPL0 signal after the IRESET* signal is asserted. It is important that IPL0 be asserted 16 ns (commercial) or 20 ns (industrial/ military) after the IRESET* signal. This allows IRESET* to reverse the direction of the IPL0 line to an input. For a reliable global reset, the IPL0 signal should be asserted for a minimum of 50 ns.

Two notes should be observed when using global resets:

- SYSCLK is not driven while IPL0 is being asserted.
- The BGiOUT* daisy-chain is disconnected during the global reset.

The characteristics of the global reset are present only while IPL0 is asserted. This implies that the aforementioned behaviors are present only during the time IPL0 is asserted. Before the IPL0 signal is asserted, the VIC068A is in an internal reset state. After IPL0 is asserted, the VIC068A is in an internal reset state except that the registers have already had their bit fields set to their default global reset state.

If a global reset is needed when the VIC068A is configured as VMEbus system controller, assert IPL0 for a minimum time. This causes SYSCLK to be disabled only for the minimum time IPL0 is asserted. The same is true for the BGiOUT* daisy-chain behavior.

The global reset mechanism is identical to the internal reset (LBG* and HALT* or RESET* timeouts, etc.) with the following two exceptions:

- All register bit fields are set to their default states.
- If the IPL0 signal is deasserted first (i.e., before IRESET*), the reset continues until a 200-ms timeout expires.
- If the IRESET* signal is deasserted first (i.e., before IPL0), the reset concludes immediately instead of waiting for the 200-ms timeout to expire.

SYSRESET* is asserted during a global reset when configured as VMEbus system controller, as it is during an internal reset.

1.11.1.3 System Reset

The system reset is a VMEbus-defined reset that is signaled by the assertion of the VMEbus signal SYSRESET*. The system reset is typically issued from another module to reset an entire VMEbus system. The system reset resets all the VIC068A internal circuitry and selected register bit fields. The VIC068A may both issue and receive a system reset. If the VIC068A issues a system reset, it also resets itself.

There are two ways to issue a system reset:

- Write the SRCR with the value of $F0.
- Implement an internal or global reset while configured as a VMEbus system controller.

The VIC068A receives a system reset by having its SYSRESET* signal asserted. When this occurs, the VIC068A begins the same procedures as if an internal reset had been performed.

The system reset is identical in function to the internal reset with the following exceptions:

- The effect on certain VIC068A register bit fields are different.
- If SYSRESET* is asserted beyond the 200-ms timeout described by the internal reset, the reset completes immediately after SYSRESET* is deasserted.

If an internal or global reset is performed on a system controller VIC068A while SYSRE-SET* is being asserted by another board, the VIC068A will not assert SYSRESET*. This implies that any SYSRESET* asserted to a system controller VIC068A should be asserted for the 200 ms required by the VMEbus specification.

1.11.1.4 Power-On Reset

To reliably reset the VIC068A at power-on, a global reset must be performed. In addition, the VIC068A must be in a "stable" operating environment at the initiation of the reset. A stable operating environment is defined by the following conditions:

- V_{CC} has reached 5V dc.
- The CLK64M signal is within the specified operating range (see Chapter 1.16).
- All inputs are in a negated state (excluding address/data buses).

If the VIC068A is not in a stable environment when IRESET* is asserted, the VIC068A may not reset reliably. If the power-on reset is performed when the environment is not stable, re-issue the global reset when the environment is stable.

Because a global reset causes certain VMEbus system controller operations to be suspended (see section 1.11.1.2), the power-on reset circuitry must be designed to assert the IPL0 signal for a "minimum" time while the VIC068A is the VMEbus system controller. Minimum is defined to be greater than the required 50 ns but less than the time the disabled features are required to be enabled for a particular application.

1.11.2 The Local Bus Timeout Timer

The VIC068A contains a local bus timeout timer that may be used to time certain local timeout conditions for the local bus. The timer begins on the assertion of DS*. If the timer period expires without an assertion of either the DSACKi* or LBERR* signals, the VIC068A asserts LBERR* and sets BESR[3].

The local timeout timer may be configured to include or not include time waiting for VMEbus acquisition. If enabled to include VMEbus acquisition time, BESR[0] is set when a timeout occurs. Once VMEbus mastership is obtained, the local timeout timer is reset and does not expire. At this point a VMEbus timeout timer (if one exists for the particular VMEbus system) is used to indicate timeout conditions. If the VIC068A is used as the system controller, this VMEbus timeout timer is located internal to the VIC068A.

If the local timeout timer is configured not to include VMEbus acquisition time, the timer resets at the assertion of BRi* and does not expire.

The local bus timeout periods are configurable for 4, 16, 32, 64, 128, 256, and 512 ms.

1.11.3 The DRAM Refresh Controller

The VIC068A contains a DRAM refresh controller. When enabled in the ARCR, the VIC068A increments a DRAM refresh counter every 15 μs. When the count of this counter reaches 4, the VIC068A requests the local bus by asserting LBR*. After the local bus is granted, the VIC068A performs a CAS-before-RAS refresh (that is, DS*-before-PAS*). The VIC068A increments the refresh counter until the local bus is granted so the actual number of cycles that are performed would equal the number in the refresh counter when the local bus is granted to the VIC068A. If a VMEbus slave request is pending, the VIC068A gives priority to the slave transfer and the DRAM refresh is performed after the slave transfer is complete, but within the same assertion of LBR*.

When the VIC068A receives the local bus, the VIC068A drives the FC2/1 signals with the DRAM refresh function codes. It then asserts PAS* and DS* according to the timing configured in the LBTR. Insure that the minimum High time specified for PAS* is greater then the minimum precharge time for the particular DRAMs being used. The VIC068A drives the LA[7:0] signals High and asserts LAEN when performing DRAM refresh. The SIZ1/0 signals are driven with a 32-bit code.

The refresh counter is a modulo-64 counter. If it reaches 64 without having the VIC068A obtain the local bus, DRAM refresh cycles may be lost. The VIC068A local bus timer may be used to insure that DRAM refresh cycles are not lost due to excessive local bus latency.

1.11.4 Rescinding Outputs

The VIC068A contains selected output signals that utilize a rescinding feature. A rescinding output is a three-state output driver that first drives the output High before three-stating. This is necessary for proper functionality of high-speed buses. The VIC068A rescinding outputs are as follows:

VMEbus	Local bus
DTACK*	PAS*
AS*	DS*
LWORD*	LBERR*
WRITE*	R/W*
BERR*	SIZ1/0*
IACK*	FC2/1*
DS1/0*	
BBSY*	

1.11.5 Turbo Mode

By setting ICR[1], it is possible to reduce certain delays within the VIC068A. When set, the VIC068A reduces the following by 1 CLK64M period:

- VMEbus address set-up time
- VMEbus data set-up time
- DTACK* asserted time for slave block transfers

Because VMEbus times may be violated with this mode enabled, this mode should be used with caution.

1.11.6 Metastability Delays

Because the VMEbus is an asynchronous bus (the local bus may also be), the VIC068A must insure that its synchronous logic is protected from possible metastable conditions. The VIC068A accomplishes this using a traditional double-sampling latch. The VIC068A samples an input, then a specified settling time later samples it again. This allows for any metastability that may have occurred to settle to a stable value. This settling time is programmable to 3T or 4T in the ICR.