



Table of Contents

[Introduction](#)

[How to Use This Book](#)

Section 1. The VICO068A VMEbus Interface Controller

[Chapter 1.1](#) Introduction to the VIC068A

1.1.1 Description

1.1.2 Features Summary

[Chapter 1.2](#) VIC068A Signal Descriptions

1.2.1 VMEbus Signals

1.2.2 Local Signals

1.2.3 Buffer Control Signals

[Chapter 1.3](#) Overview of the VIC068A

1.3.1 Resetting the VIC068A

1.3.2 The VIC068A VMEbus System Controller

1.3.3 VIC068A VMEbus Master Cycles

1.3.3.1 Master Write-Posting

1.3.3.2 Indivisible Cycles

1.3.3.3 Deadlock

1.3.3.4 Self-Access

1.3.4 VIC068A VMEbus Slave Cycles

1.3.4.1 Slave Write-Posting

1.3.5 Address Modifier (AM) Codes

1.3.6 VIC068A VMEbus Block Transfers

1.3.6.1 MOVEM Master Block Transfers

1.3.6.2 Master Block Transfers with Local DMA

1.3.6.3 Slave Block Transfers

1.3.7 VIC068A Interrupt Generation and Handling Facilities

1.3.8 Interprocessor Communication Facilities

[Chapter 1.4](#) System Controller Operations

1.4.1 VMEbus Arbitration

1.4.2 The VMEbus Arbitration Timeout Timer

1.4.3 The VMEbus Transfer Timeout Timer

1.4.4 The BGi Daisy-Chain Driver

1.4.5 The IACK* Daisy-Chain Driver

Chapter 1.5	VIC068A VMEbus Master Operations
	1.5.1 VMEbus Requests
	1.5.2 Release Modes
	1.5.2.1 Release On Request (ROR)
	1.5.2.2 Release When Done (RWD)
	1.5.2.3 Release On Clear (ROC)
	1.5.2.4 VMEbus Capture and Hold (BCAP)
	1.5.2.5 Release Under RMC* Control
	1.5.3 VIC068A VMEbus Master Write Cycle
	1.5.4 VIC068A VMEbus Master Read Cycle
	1.5.5 Master Write Posting
	1.5.6 Indivisible Cycles
	1.5.6.1 Indivisible Single-Address Cycles (ISACs)
	1.5.6.2 Indivisible Multiple-Address Cycles (IMACs)
	1.5.7 Deadlock
	1.5.7.1 Undetectable Deadlocks
	1.5.8 Self-Access
	1.5.9 VMEbus/Local Bus Data and Port Size
	1.5.10 Fair Request Timeout
	1.5.11 Address-Only Cycles
	1.5.12 The Address Modifiers for Master Cycles
Chapter 1.6	VIC068A VMEbus Slave Operations
	1.6.1 The Valid Slave Select
	1.6.2 The Local Bus Request
	1.6.3 The Local Bus Grant
	1.6.4 Local Bus Timing
	1.6.5 VMEbus/Local Bus Data and Port Size
	1.6.6 The Latched Bus Interface
	1.6.7 Slave Write Posting
	1.6.8 Slave Acknowledge Timing (SAT)
Chapter 1.7	VIC068A Control Register Access
	1.7.1 Control Registers
	1.7.2 Control Register Access
Chapter 1.8	Interprocessor Communication Facilities
	1.8.1 Valid ICF Selection
	1.8.2 Interprocessor Communication Registers
	1.8.3 Interprocessor Communication Global Switches
	1.8.4 Interprocessor Communication Module Switches
Chapter 1.9	Interrupts
	1.9.1 VMEbus Interrupter
	1.9.2 The VIC068A VMEbus Interrupt Handler
	1.9.3 Local Interrupt Handler
	1.9.4 The FCIACK Cycle
	1.9.5 The Error/Status Interrupts
	1.9.6 Interrupt Priority Order

1.9.7 Clock-Tick Interrupt Generator

1.9.8 Interrupt Control Registers

[Chapter 1.10](#) VIC068A Block Transfer Functions

1.10.1 VIC068A Master Block Transfer

1.10.1.1 Block Transfers with Local DMA

1.10.1.2 MOVEM Block Transfers

1.10.1.3 Buffer Control Signals During Master Block Transfers

1.10.1.4 Performing Block Transfers to VMEbus Slaves Not Supporting Block Transfers

1.10.2 VIC068A Slave Block Transfers

1.10.3 Buffer Control Signals During Slave Block Transfers

1.10.4 Using the CY7C964 for Additional Block Transfer Support

[Chapter 1.11](#) Miscellaneous Features

1.11.1 Resetting the VIC068A

1.11.1.1 Internal Reset

1.11.1.2 Global Reset

1.11.1.3 System Reset

1.11.1.4 Power-On Reset

1.11.2 The Local Bus Timeout Timer

1.11.3 The DRAM Refresh Controller

1.11.4 Rescinding Outputs

1.11.5 Turbo Mode

1.11.6 Metastability Delays

[Chapter 1.12](#) VIC068A Register Map and Descriptions

[Chapter 1.13](#) VIC068A AC Performance Specifications

[Chapter 1.14](#) VIC068A Signal List and Pinouts

[Chapter 1.15](#) VIC068A Simulation Waveforms

[Chapter 1.16](#) DC Performance Specifications

[Chapter 1.17](#) Package Diagrams

Section 2. The VIC64 VMEbus Interface Controller

[Chapter 2.1](#) Introduction

[Chapter 2.2](#) Compatibility

[Chapter 2.3](#) 64-Bit Operations

2.3.1 VMEbus Specification

2.3.2 Address Modifier Codes

2.3.3 Boundary Crossing

2.3.4 External Circuit Complexity

[Chapter 2.4](#) VIC64: Additional Information

2.4.1 VIC64 Signal Description (Chapter 1.2)

2.4.2 System Controller Operations (Chapter 1.4)

2.4.3 VMEbus Master Operations (Chapter 1.5)

2.4.3.1 D64 Master Write Cycles

- 2.4.3.2 D64 Master Read Cycles
- 2.4.4 VMEbus Slave Operations (Chapter 1.6)
 - 2.4.4.1 D64 Slave Read Cycles
 - 2.4.4.2 D64 Slave Write Cycles
- 2.4.5 Interrupts (Chapter 1.9)
- 2.4.6 VIC64 Block Transfer Functions (Chapter 1.10)
 - 2.4.6.1 D64 Transfers, VMEbus Boundary Crossing
- 2.4.7 Miscellaneous Features (Chapter 1.11)
 - 2.4.7.1 Selection of System Controller Functionality
 - 2.4.7.2 Enhanced Turbo Mode
- 2.4.8 Register Map and Descriptions (Chapter 1.12)
 - 2.4.8.1 Interprocessor Communications Register 5
 - 2.4.8.2 Block Transfer Definition Register
 - 2.4.8.3 Release Control Register
 - 2.4.8.4 Block Transfer Length Register 2
- 2.4.9 AC Performance Specifications (Chapter 1.13)

[Chapter 2.5](#) DC Performance Specifications

[Chapter 2.6](#) Pin Configurations

[Chapter 2.7](#) Package Diagrams

Section 3. The CY7C960/961 Slave VMEbus Interface Controllers

[Chapter 3.1](#) Introduction

- 3.1.1 Feature List
- 3.1.2 Family Overview
- 3.1.3 CY7C960 Architectural Overview
- 3.1.4 Key Concepts
 - 3.1.4.1 Local Bus Concepts
 - 3.1.4.2 VMEbus Concepts
- 3.1.5 Address Mapping

[Chapter 3.2](#) System Block Diagrams

[Chapter 3.3](#) Pin Description

- 3.3.1 VMEbus Signals
- 3.3.2 Local Signals
- 3.3.3 Local Buffer Control Signals

[Chapter 3.4](#) Programming the CY7C960

- 3.4.1 Configuration Bit Stream
- 3.4.2 Operation at Power-On or Reset
- 3.4.3 VMEbus Method
- 3.4.4 Serial PROM Method
- 3.4.5 Combination Method
- 3.4.6 Configuration Software
- 3.4.7 Programmable Features

Chapter 3.5	VMEbus Interface Description
	3.5.1 Definition of Terms
	3.5.2 Overview
	3.5.3 Region Mapping
	3.5.3.1 AM/LA Multiplexing
	3.5.4 Bus Holdoff
	3.5.4.1 Transaction Type Detection
	3.5.5 Decode Delay Timing
	3.5.6 Slave Addressing Before Initialization
	3.5.7 Address and Data Strobe Event Processing
	3.5.8 Slave Data Transfer Acknowledgment
	3.5.9 Slave Write Posting
	3.5.10 Slave Read-Ahead Cycles
	3.5.11 Interrupt Cycle Support
	3.5.12 Interrupt Handshake Support
Chapter 3.6	CY7C964 Interface
	3.6.1 CY7C964 Overview
	3.6.2 CY7C964 Connections
	3.6.3 Swap Buffer Control
Chapter 3.7	Interfacing without CY7C964
	3.7.1 Reduced Cost, Fewer Features
Chapter 3.8	DRAM Control Description
	3.8.1 Overview
	3.8.2 Types of DRAM
	3.8.3 VMEbus Implications
	3.8.4 Refresh Cycles
	3.8.5 Refresh Timing
	3.8.6 DBE Refresh Enable Feature
	3.8.7 Refresh and Reset
	3.8.8 Local Acknowledge Behavior
	3.8.9 DBE Signal Behavior
	3.8.10 Formal Signal Description
	3.8.10.1 RAS*, CAS*, ROW, COL
	3.8.11 Programmable Features
	3.8.11.1 Refresh Enable
	3.8.11.2 Cycle Timing
	3.8.11.3 Refresh Period
	3.8.11.4 DBE Refresh
	3.8.11.5 DBE Polarity
	3.8.11.6 ROW, COL Polarity
Chapter 3.9	I/O Control Description
	3.9.1 Region Mapping
	3.9.2 Chip Select Output Control
	3.9.3 Chip Select Output Timing
	3.9.3.1 Overview

- 3.9.3.2 Read-Aheads
- 3.9.3.3 Local Acknowledge Timing
- 3.9.4 Data Byte Enable Usage
- 3.9.5 Using I/O In DRAM Mode

Chapter 3.10 Design Considerations

- 3.10.1 Design Philosophy
- 3.10.2 CY7C964 Interface
- 3.10.3 Local Bus Philosophy
- 3.10.4 Read-Ahead Cycles
- 3.10.5 Write Posting
- 3.10.6 VMEbus Error Considerations

Chapter 3.11 CY7C961 Description

- 3.11.1 Introduction
- 3.11.2 CY7C961 Lock Cycle Support
 - 3.11.2.1 Overview
 - 3.11.2.2 Description
- 3.11.3 CY7C961 Master Block Facility
 - 3.11.3.1 Overview
 - 3.11.3.2 Master Block Transfer Control from VMEbus
 - 3.11.3.3 Master Block Transfer Control from Local Side of Interface
 - 3.11.3.4 Programming the Master Block Facility
 - 3.11.3.5 Register Definitions
- 3.11.4 Pin Description Addendum
 - 3.11.4.1 VMEbus Signals
 - 3.11.4.2 Local Buffer Control Signals
 - 3.11.4.3 Local Signals
 - 3.11.4.4 Master Block Transfer Performance
- 3.11.5 Examples of Block Transfers

Chapter 3.12 AC Parameters

Chapter 3.13 DC Performance Specifications

Chapter 3.14 Package Diagrams

Section 4. The CY7C964 Bus Interface Logic Circuit

Chapter 4.1 Introduction

Chapter 4.2 Features

Chapter 4.3 Interfacing to Cypress VMEbus Interface Controllers

- 4.3.1 VMEbus Signal Group
- 4.3.2 Buffer Control Signal Group
- 4.3.3 CY7C964 Local Signal Group
- 4.3.4 CY7C964 Address Comparison and Local Signal Group
- 4.3.5 Local Data Swap Buffer Logic

Chapter 4.4 Signal Descriptions

- 4.4.1 VMEbus Signals
- 4.4.2 Local Signals

Chapter 4.5	CY7C964 Operation
	4.5.1 Overview
	4.5.2 Master Block Transfer Local Address Counter (C1)
	4.5.3 Local Address Multiplexer (S5)
	4.5.4 Slave Block Transfer Local Address Counter/Latch (C2)
	4.5.5 Master Block Transfer VMEbus Address Counter (C3)
	4.5.6 VMEbus Address Latch (L8) and Multiplexer (S3)
	4.5.7 VMEbus Address Comparator
	4.5.8 VMEbus D64 Block Transfer Data Pipeline and Multiplexer
	4.5.9 VMEbus D64 Block Transfer Data Demultiplexer
Chapter 4.6	CY7C964 Alternate BLT Initiation Operation for VIC068A and VIC64
Chapter 4.7	DC Performance Specifications
Chapter 4.8	AC Performance Specifications
Chapter 4.9	Pin Description
	4.9.1 Pin Definitions
	4.9.2 Pin Configurations
Chapter 4.10	Package Diagrams

Section 5. The VAC068A VMEbus Address Controller

Chapter 5.1	Introduction to the VAC068A
	5.1.1 Features Summary
	5.1.2 General Description
Chapter 5.2	VAC068A Signal Descriptions
	5.2.1 VMEbus Signals
	5.2.2 CPU/Local Interface Signals
	5.2.3 Parallel I/O-Shared Function Signals
	5.2.4 Data Flow Control Signals
Chapter 5.3	VAC068A Overview
	5.3.1 Applications
	5.3.2 VMEbus Address Decoding
	5.3.2.1 Master Access
	5.3.2.2 Programmable VMEbus Space
	5.3.2.3 A24 VMEbus Space
	5.3.2.4 A16 VMEbus Space
	5.3.3 VMEbus Slave Access
	5.3.4 Local Memory Map Decoding
	5.3.4.1 DRAM Decode
	5.3.4.2 Programmable Decode
	5.3.4.3 EPROM Decode
	5.3.4.4 Local I/O Select Decode
	5.3.5 Local Decode Control/Status
	5.3.5.1 Function Code Decode
	5.3.6 Programmable Input/Output
	5.3.6.1 Serial I/O

- 5.3.6.2 I/O Select
- 5.3.7 Interrupt Support
 - 5.3.7.1 Interrupt Status Register
 - 5.3.7.2 PIO Interrupt
- 5.3.8 Miscellaneous Features
 - 5.3.8.1 PIO9 Debounce
 - 5.3.8.2 Isolated Data Bus
 - 5.3.8.3 Programmable DSACKi* Timing
 - 5.3.8.4 VIC068A/VAC068A DMA Support
 - 5.3.8.5 IORD* and IOWR*
 - 5.3.8.6 I/O Recovery Timer
 - 5.3.8.7 IACK Cycle Emulation for Non-680X0 Processors
 - 5.3.8.8 Cache Inhibit Output

Chapter 5.4

VAC068A Operation

- 5.4.1 Resetting the VAC068A
 - 5.4.1.1 Global Reset
 - 5.4.1.2 Soft Reset
 - 5.4.1.3 RESET* Termination
- 5.4.2 System Initialization
- 5.4.3 Configuring the Local Memory Map
 - 5.4.3.1 DRAM Size
 - 5.4.3.2 VSB Space
 - 5.4.3.3 VMEbus A32, D32 Access
 - 5.4.3.4 Shared Resource Area
 - 5.4.3.5 EPROM Space
- 5.4.4 Configuring the VMEbus Address Map
 - 5.4.4.1 SLSEL0* Access
 - 5.4.4.2 SLSEL1* Access
 - 5.4.4.3 ICFSEL* Access
 - 5.4.4.4 VME A24 Master Cycle
 - 5.4.4.5 VME A16 Master Cycle
 - 5.4.4.6 Decode Control Register
- 5.4.5 VME Master Access
- 5.4.6 VME Slave Operation
 - 5.4.6.1 Slave Transfer Sequence
- 5.4.7 VME Master Block Transfer
- 5.4.8 VIC068A/VAC068A Interconnect Diagram

Chapter 5.5

VAC068A Register Map and Descriptions

Chapter 5.6

VAC068A AC Performance Specifications

Chapter 5.7

VAC068A Signal List and Pinout

Chapter 5.8

DC Performance Specifications

Chapter 5.9

Package Diagrams

Glossary