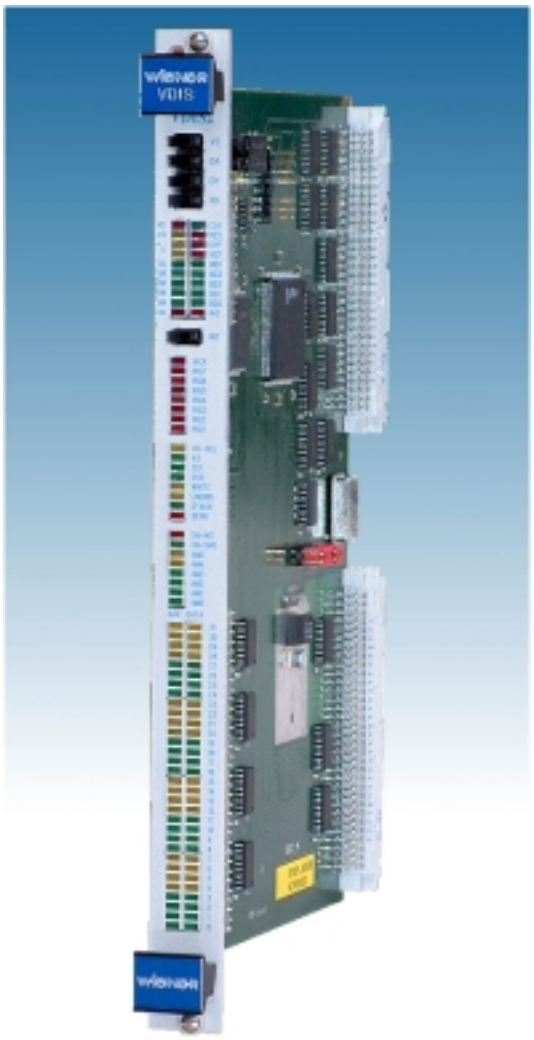

VDIS-2

VME test and diagnostic module

User manual

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1 GENERAL INFORMATION

The new VDIS-2 is a new generation of the VDIS VME bus display and diagnostic module, which has been successfully used in VME applications in industry and research for the past 12 years. VDIS-2 is a helpful tool for configuration, set-up and test of VME systems and software debugging as well as for maintenance and service of VME hardware.

New features:

- VDIS-2 is equipped with a 256 Byte VME-SHORT address area for extended test functions fully programmable via VME
- Enlarged LED panel for better display

New VME-SHORT-area functions:

- Software control for all front panel switches
- Interrupt Logic for test purposes
- All addresses, data and VME-control lines are stored for each VME-cycle in a register for read-back
- 32-bit data register for read and write tests
- 32-bit test counter

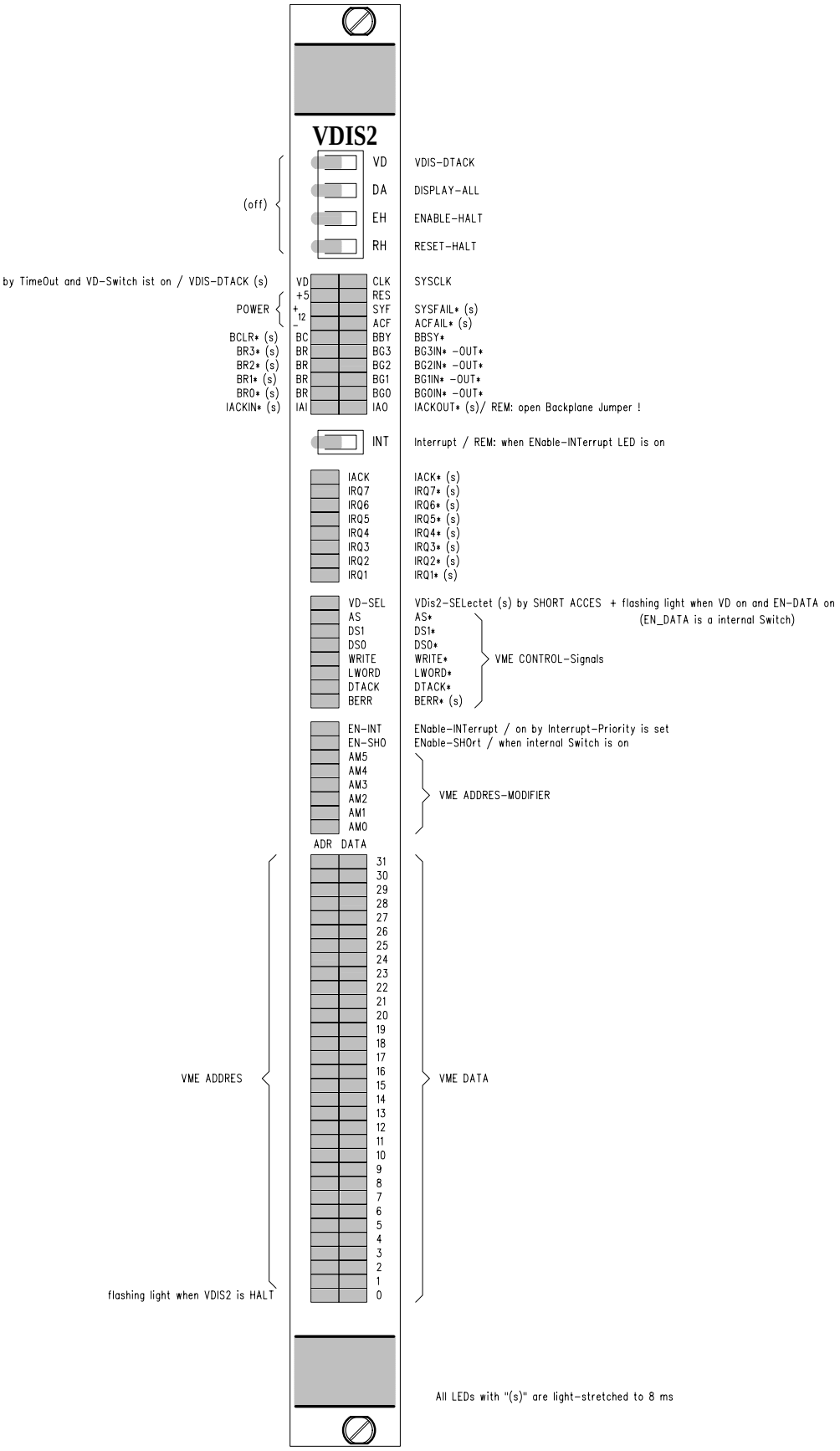
VDIS2 standard features:

- LED display for all relevant VME-bus lines:

Data Transfer Bus:	**D00..D31, A00..A31, AM0..AM5, LWORD*, WRITE* AS*, DS0*, DS1 *, DTACK*, BERR*.**
Interrupt Bus:	**IRQx*, IACK*, IACKIN*,IACKOUT***
Arbitration Bus:	**BRx*, BGxIN* - BGxOUT*, BBSY*,BCLR***
Utility Bus:	**SYSRESET*, SYSFAIL*, ACFAIL*, SYSCLK*.**
Other:	**+5Volt, +12Volt, -12Volt, VDIS-DTACK*,**
	EN-SHORT, VDis2-SELECT, EN-INTERRUPT, HALT

- Can hold and keep visible signal groups with corresponding qualifier in certain conditions (BERR, BBSY, DTACK, …)
- Uses signal stretcher to increase visibility of signal groups and corresponding qualifier for better display (IRQ, …)
- **VD** (VDIS DTACK) diagnostic mode, VDIS-2 generates in case of a missing DTACK from other VME units the DTACK at the end of a programmable „time-out“ time , in this mode the data of the previous cycle are available for read-back (VME READ only)
- **EH** (ENABLE HALT) diagnostic mode, records the status of all VME bus signals in case of a bus error and holds it until a manual reset occurs
- VDIS-2 is simple to use and transparent for any software.
- VDIS is a standard 6U VME slave module
- All main operating elements are accessible on the front panel. The display elements are color coded and functionally grouped.

2 FRONT PANEL VIEW



3 FUNCTIONAL DESCRIPTION

3.1 Introduction

VDIS displays most of the VMEbus signals with colored LEDs on the front panel. For easy recognizing all address and data signals are arranged in four groups with different colors allowing a fast transcription of bit patterns into hexadecimal digits.

A shining LED shows an active signal. For instance, the LED “D0” (Data 0) lights, if the signal on this VME-bus line has a level higher than the TTL active threshold. Otherwise the LED „AS*“ lights, if the signal on this VME-bus line has a level which is lower than the TTL switching threshold.

As described in detail on the following pages, some of the signals will be “captured” by the VDIS-2 logic or will be elongated via “Stretcher” (signal elongation settings) to a visible duration. Some signals are displayed staticly.

3.2 VME-bus Signal Processing and Display

The following signals are captured by a DTACK* or BERR* :

Data:	D00..D31
Addresses:	A01..A31
Address modifier:	AM0..AM5
Control signals:	AS*, DS0*, DS1 *, WRITE*, LWORD*
Interrupt-Bus:	IACK*, IACKIN*, IACKOUT*

In case of missing DTACK* or BERR*, the above listed bus signals are stored at the end of DS0* / DS1*. This may cause a discrepancy between the stored data signals and the status of the VME cycle if the address, data and AM hold times of the VME master are too short.
In these cases, all control signals are displayed correctly because of storing the signals in start registers. The DTACK* und BERR* signals are “on activity” stored and displayed.

The following signals are captured with BBSY*:

Arbitration-Bus:	BG0IN*, BG0OUT*, BG1IN*, BG1OUT* BG2IN*, BG2OUT*, BG3IN*, BG3OUT*

The following signals are stretched to be visible:

Interrupt-Bus:	IRQ1*..IRQ7 , IACK*, IACKIN*, IACKOUT*
Arbitration-Bus:	BGx*, BRx*, BCLR*, BBSY*
Utility-Bus:	SYSRESET*, SYSFAIL*, ACFAIL* ,BERR*

SYSCLK* signal:
VDIS-2 detects the SYSCLK signal by using a differential logic circuit. In a VME crate with multiple master modules only one should be configured as system-controller. In case of several system controllers on one bus the SYSCLK signal is fed multiple times to the bus. This can be indicated by flashing CLK-LEDs. One of the VDIS-2 status bits further contains the information about the presence of the SYSCLK signal.

3.3 Other LEDs

Power LEDs:
The power LEDs are indicating the presence of the correct voltages on the VME bus power lines +5Volt, +l2Volt und -l2Volt. All voltages are monitored with a integrated circuit MAX 8215 with the following thresholds:

- +5Volt-LED lights if U_{+5V} > +4,6Volt.
- +l2Volt-LED lights if U_{+12V} > +10,6 Volt.
- -l2Volt-LED lights if U_{-12V} < -10,6 Volt.

It is assumed that the +5V line used by the VDIS-2 is properly working. If this is not the case, it may cause wrong logic or display operations.

LED „VD“ (VDIS-DTACK):
VD indicates that VDIS-2 is working in a mode to generate DTACK* after the time-out period if no other VME module generates this signal. The display is stretched to approximately 8 ms.
In case of an active HALT this LED lights permanently.

LED „INT“:
INT corresponds to an activated interrupt priority in the interrupt register. By pressing the switch „INT“ an IRQx will be generated on the VME-bus.

LED „EN-SHORT“:
Displays that the VDIS-2 short address mode is switched on. The „EN-SHORT“ switch is located on the PCB behind the front panel. In this mode SHORT calls are possible to program or to read-out VDIS-2.
In a special mode this LED further indicates available data after the time-out in case of missing DTACK (switches VD and EN-DATA = ON). This is shown by flashing (inverting) of the EN-SHORT LED.

LED „HALT“:
The A00 address line does not exist on the VME-bus. Because of manufacturing reasons this LED is equipped on the display and used to indicate a „HALT“ status by a short flashing of this LED (for details see chapter 3.4).
Please note that the A00 LED is not labeled on the front panel.

The following bus lines are not displayed:
+5VSTBY, SERCLK, SERDAT* und RESERVED

3.4 VDIS-2 Switches and Jumpers

For an easy operation the common used switches are located on the VDIS-2 front panel, i.e. there are three switches (**VD**, **DA**, **EH**) as well as 2 push-buttons (**RH**, **INT**) which are described in

detail as follows. Further there are two internal switches located on the PCB behind the front panel (**SHORT / ENABLE DATA modes**). These switches have to be configured before inserting VDIS-2 into the VME crate. The jumper array JA8 to JA15 defines the SHORT base address.
All other jumpers on the PCB are for future extensions and presently not used.

3.5 Front panel switches

„VD“ switch (VDIS-DTACK)
activates the “DTACK by VDIS-2” mode in which VDIS-2 generates the DTACK signal on the VME-bus after a predefined time-out period. The length of the time-out period is fix 4µs (if „EN-SHORT“ off). This time can be programmed to be either 3µs, 2µs or 1µs, if the VDIS-2 is used in the „EN-SHORT“ mode.
In mode „VDIS-DTACK = ON“ VDIS-2 responds to all bus transfers which are not terminated by a time-out. This covers not only regular data transfers, but also „interrupt-acknowledge-cycles“. The „EN-DATA“ function can only be used in active „VD“ mode.

„DA“ switch (DISPLAY ALL)
enables the non-interpretive display-only mode. In case of „DA=OFF“ the signals of all bus transfers are interpreted by the VDIS-2 logic for correct display. Thus a “Byte-Transfer” does only overwrite the corresponding byte of the display or in case of a 16-bit short address cycle only the A01 - A15 and D00 - D15 bytes are displayed.
In “DA=ON“ VDIS-2 will display all registered address, data and address modifier lines.

„EH“ switch (ENABLE HALT)
activates the “hold on error” mode. In case of a bus error all data, address and control signals will be stored and displayed. The status of the “VD” will cause various actions in this mode:

1. “VD=ON”: in case of missing DTACK* from other VME units VDIS-2 generates the DTACK* indicated by the shining red LED “VD“ and switches into HALT mode shown by a flashing **“HALT“ LED.**

2. “VD=OFF”: any bus error generated on the VME-bus will result in switching VDIS-2 into HALT mode which will be indicated by a flashing **“HALT“ LED.**

The hold state (HALT) can only be released by pushing the “RH“ button. This enables VDIS-2 to detect the next occuring bus error.

„RH“ button (RESET HALT)
releases VDIS-2 from the hold state (HALT) to an active ENABLE HALT mode.

„INT“ button (INTERRUPT)
sets the interrupt flip flop. The interrupt is only requested if an allowed interrupt-priority value (1 to 7) is defined at the interrupt-register. In this case, the LED „EN-INT“ will lighten.
The interrupt flip flop can only be reset by software (SHORT MODE).

3.6 Internal Switches

“EN-SHORT“ switch (ENABLE SHORT)
enables or disables the SHORT area of VDIS-2. In this mode several VDIS-2 functions as well as the front panel switch configuration can be programmed. All addresses and functions are described in detail in the following chapters.

“EN-DATA“ switch (ENABLE DATA)
If both „VD“ and „EN-DATA“ are switched on, VDIS-2 transfers the content of the data register onto the VME-bus in case of a read-cycle and after the time-out. Following a DTACK* will be generated with a delay of about 30ns. In case of “EN-DATA=OFF” no data can be retrieved from VDIS-2 except for the SHORT READ for VDIS-parameters / features.

4 REMARKS

4.1 General Comments

The VDIS-2 display does not disturb or affect the VME-bus or the functionality of any VME-bus module, only if it is used in one of the special diagnostic modes for troubleshooting.

VDIS-2 adds a TTL-LS-load to all VME-bus lines. The signals DTACK* and IRQx* have an additional load of one 74LS641-1.

VDIS-2 bridges the “Daisy-Chain” lines BGxIN* to BGxOUT*. Similar bridges on the VME backplane do not affect the VDIS-2 function.

ATTENTION !!! The signals IACKIN* and IACKOUT* have to be generated and to be controlled by the VDIS2-interrupt-logic circuit. The corresponding bridge on the VME backplane has to be open!!!

VDIS-2 can be used in a crate with an only 3U high J1 (P1) backplane, too. In this case all signals of the not present P2 (J2) bus Dl6..D31 and A24..A31 are in a non-defined state. Usually open lines will be displayed as active ones.

Some older VME backplanes do not have automatic daisy chain detection. In this case there may be slots with not connected daisy chain lines. Using VDIS-2 in such a slot causes a non-defined state for these signals which will be shown as non-active. However random distortions may occur

SYSRESET clears all displayed VME-bus data however SYSRESET*, SYSFAIL*, ACFAIL* and SYSCLK will be displayed.

4.2 VDIS-2 Timing

All addresses, data, address modifiers, IACK*, IACKOUT*, LWORD*, WRITE*, AS*, DS0* and DS1 are stored in normal operation at DTACK* or BERR* negation phase.

All signals are transferred with an almost similar delay time into the LATTICE-FPGA. For normal operation a general set-up and hold time of at least 15ns is expected for all signals.

All VDIS-2 timing parameters are as specified within the „VME-bus Specification , ANSI/IEEE-STD 1014-1987, IEC 821 and 297“ for VME-bus Slaves.

The VDIS-2 signal-stretcher can capture signals with a width of minimum length of 10ns or longer and display these signals for a visible extended time.

4.3 Power Consumption

Voltage Line	Maximum Current	Power
+5V	1.1A to maximum 1.4 A	max. 7 W

5 RECOMMENDATIONS FOR VDIS-2 USE

5.1 Monitoring

For permanent monitoring of VME-bus activities VDIS-2 can be added to any VME system. In this case "VD" should be switched off. Depending on the required tasks "EH" may be active. Please note that some VME operating systems check the available address space during initialization until the first bus error occurs. Furthermore there are VME block modes (CBLT according to VME-P) which are terminated by a time-out. In these cases a bus error can be detected legally.
Depending on the position of VDIS-2 inside a VME crate, different types of tests are possible. These tests are described in more details in the following chapters.

5.2 Address Data -Tests

It is possible to test the VME-bus data and address lines for disconnections or shortages by cycles with alternating write / read operations to different addresses in "VD" mode.
Example:

i write: all even address and data bits are 1 (other 0)
i+1 write: all odd address and data bits are 1 (other 0)
In a continuous cycle a homogeneously changing pattern has to be displayed. Furthermore it is possible to read back addresses, data, address modifiers and control signals for comparison with the software HALT function.

ATTENTION! Please make sure that no other slave module in the VME system is accessed in such a test by selecting a suitable address modifier.

5.3 Detection of random bus errors

Operating VDIS-2 in the "EH" mode allows to detect random bus errors even without using a software debugger. These errors are usually caused by defective hardware or by incorrect software code as "not initialized " or "disappearing" pointer. Even "spurious interrupts" can be detected.

Some VME masters generate only local bus errors. In these circumstances VDIS-2 cannot detect a VME-bus problem. If using VDIS-2 in the "VD" and "EH" mode however errors can be detected . The time-out of the VME master has to be longer (> 5µs) than the VDIS-2 setting to allow to display the access address in case of a time-out error.

5.4 Bus allocation test

For this purpose VDIS-2 has to be plugged into the slot right before (to the left of) the VME master. In this case the LED's indicate how often the bus is allocated by the particular master or other ones of the same priority level. This test cannot be done for the VME-bus master with system controller function which is located in slot "0" of the VME crate.

5.5 Interrupt-Daisy-Chain Check

Similar to the bus allocation test, it is possible to get an indication about not responded or randomly generated interrupts by selecting the right slot number for VDIS-2 and enabled “EH“ mode.

Attention: The interrupt daisy-chain jumper has to be open!

5.6 Utility Bus Check

Failures are visible by looking at the relevant LEDs. Shortly occurring interferences on the ACFAIL* line become visible due to the VDIS-2 signal stretching function.
In case of multi-master systems it is possible to detect a multiple inducted system clock (SYSCLK). This will be indicated by a flashing CLK-LED (changing its lightening intensity) due to overlaying interference effects which may occur in such cases.

6 SHORT MODE OPERATION

In addition to the front panel switches VDIS-2 has two internal switches for the EN-SHORT and EN-DATA function (see chapter 5.2).
To enable the SHORT-mode the EN-SHORT switch has to be in ON position and the jumper array JA08 – JA15 has to be configured for the correct short base address.

PLEASE NOTE: The „EN-DATA“ switch / function is independent from the SHORT mode and does not correspond to the SHORT data read.

6.1 SHORT mode configuration

VDIS-2 can be accessed in the SHORT address mode (AM = $29 or $2D) if “EN-SHORT=ON“.
The jumper array JA8 to JA15 defines the SHORT base address as following.

JA15	JA14	JA13	JA12	JA11	JA10	JA9	JA08	Function
A15	A14	A13	A12	A11	A10	A9	A8	VME-Short-address
:	I	I	I	:	I	I	I	Factory setting (0x8800)

: = Jumper open = logic 1
I = Jumper inserted = logic 0

The factory default VDIS-2 SHORT base address is $8800 (0x8800)

Important Notice: Please make sure that this address space is not used otherwise.

6.2 Access times

Write to VDIS-2: duration from AS* to DTACK* approx. 120ns.
Read from VDIS-2: duration from AS* to DTACK* approx. 120ns.

All data are available on the VME bus 60ns before DTACK*.

7 SHORT MODE ADDRESS MAP

Short-Addres + Offset	Access Type	WR-Function /DATA	RD-Function /DATA
+ $80..FC	WORD LWORD	**Reset COUNTER** **Reset COUNTER**	**COUNTER Cnt15..Cnt00** **COUNTER Cnt31..Cnt00**
+ $40..7F + $40..7E + $40..7C	BYTE WORD LWORD	**DATA-Reg D07..D00/D15..D08** **DATA-Reg D15..D00** **DATA-Reg D31..D00**	**DATA-Reg D07..D00/D15..D08** **DATA-Reg D15..D00** **DATA-REG D31..D00**
+ $32..	WORD	-	**AddrReg A23..A16** **CLK- u. Power-Status**
+ $30..3C	WORD LWORD	**-** **-**	**AddrReg A15..A1** **AddrReg A31..A1**
+ $20..2C	Word	**Software-Interrupt Control**	**VME-Control-Signal Reg.**
+ $10..1C	Word	**Interrupt Control Reg.** **Timeout Reg.**	**Interrupt Control Reg.** **u. Timeout Reg.**
+ $00..0C	Word	**Control Function**	**STATUS Register**

The VDIS-2 SHORT mode covers a 256 byte address space. The base address has to be defined by jumpers JA8 to JA15. Accessing this address area is only possible if "EN-SHORT=ON".
LWORD calls to word addresses (A2 = 0) are possible, however, the data bits D31 – D16 are not relevant in this case.

7.1 Control and status register (0x00)

Short-Addr.+$00	WR-Control-Register	RD-STATUS-Register
WORD	D15 - D14 - D13 - D12 - D11 - D10 - D09 – D08 - D07 = SO-HALT D06 - D05 - D04 = SO-ENDATA D03 = SO-RH puls D02 = SO-EH on D01 = SO-DA on D00 = SO-VD on	D15 = 1 > CLPW OK / 0 = Error D14 = Jumper J2 (for future function) D13 = Jumper J1 (for future function D12 = SW-ENDATA /Switch-ENDATA D11 = SW-RH /Switch-RH D10 = SW-EH /Switch-EH D09 = SW-DA /Switch-DA D08 = SW-VD /Switch-VD D07 = SO-HALT D06 = X D05 = X D04 = SO-ENDATA /Software-ENDATA D03 = SO-RH /Software-RW D02 = SO-EH /Software-EH D01 = SO-DA /Software-DA D00 = SO-VD /Software-VD

Data bit = 0 means **off**
Data bit = 1 means **on / active**

Due to the control register, VDIS-2 can be completely controlled via software, i.e. it is possible to define the VDIS-2 switch settings and operating modes by setting the corresponding bits D00 to D04 in the control register. Please note that the final function / mode is a logic **OR** of the front panel switch state and the control register setting!
VDIS-2 has an additional software HALT function "SO-HALT" (bit D07) which allows to hold the content of the data-, address- and VME control registers unchanged. This allows to read back the values from the previous VME cycle from these registers.

The VDIS-2 status register displays the condition of all switches as well as the software register.

The CLPW (CLOCK and POWER) bit indicates a correct VME environment and is determined in the following way (**AND** , **AND NOT** are logic operators):

CLPW = (SCLKOK) **AND** (+5VOK) **AND** (+12VOK) **AND** (-12VOK) **AND NOT** (+5VOV)

SCLKOK = SYSCLK is active on VME backplane
+5VOK = +5 Volt supply > +4,6Volt
+12VOK = +12 Volt supply > + 10,6 Volt
-12VOK = -12 Volt supply < – 10,6Volt
+5VOV = +5 Volt supply > + 5,5 Volt (OVERVOLTAGE !)

The status of SCLKOK and the individual power line conditions are stored additionally in the VME address register (offset 0x32, see paragraph 7.4).

7.2 Interrupt and Timeout Register (0x10)

Short-Adr.+$10	WR I.T. Register	RD I.T. Register
WORD	D15 = x D14 = x D13 = Timout (bit 1) D12 = Timout (bit 0) D10 = Interrupt-Mode 0=RORA/1=ROAC D11 = Interrupt-Priority (bit 2) D10 = Interrupt-Priority (bit 1) D08 = Interrupt-Priority (bit 0) D07 = Interrupt-Vector (bit 7) D06 = Interrupt-Vector (bit 6) D05 = Interrupt-Vector (bit 5) D04 = Interrupt-Vector (bit 4) D03 = Interrupt-Vector (bit 3) D02 = Interrupt-Vector (bit 2) D01 = Interrupt-Vector (bit 1) D00 = Interrupt-Vector (bit 0)	D15 = 0 D14 = 0 D13 = Timout (bit 1) D12 = Timout (bit 0) D10 = Interrupt-Mode 0=RORA/1=ROAC D11 = Interrupt-Priority (bit 2) D10 = Interrupt-Priority (bit 1) D08 = Interrupt-Priority (bit 0) D07 = Interrupt-Vector (bit 7) D06 = Interrupt-Vector (bit 6) D05 = Interrupt-Vector (bit 5) D04 = Interrupt-Vector (bit 4) D03 = Interrupt-Vector (bit 3) D02 = Interrupt-Vector (bit 2) D01 = Interrupt-Vector (bit 1) D00 = Interrupt-Vector (bit 0)

VDIS-2 has interrupt capability. A valid interrupt priority (value 1 to 7) has to be defined within bits D08 – D11 in order to generate a VME-bus interrupt. This is indicated by a shining “INT“ LED. In this case the interrupt flip flop becomes active by pressing the “INT“ button on the front panel or by requesting an interrupt via software (please see paragraph 7.3 VME Control and Software Interrupt Control Register). IRQx becomes active according to the defined interrupt priority.
Please note, that in case of a VME master activated interrupt the corresponding interrupt vector has to be loaded first. For a description of the interrupt mode (RORA/ROAC) please consult the VME bus manual / specification.

In the VDIS-DTACK mode (“VD“ =ON) the VME bus display VDIS-2 generates the DTACK* signal after the time-out. The length of the time-out period is adjustable when working in SHORT mode.

TO bit 1	TO bit 0	Time to DTACK*
0	0	4µs
0	1	3µs
1	0	2µs
1	1	1µs

In case of de-activated SHORT mode (“SHORT”=OFF) the time-out length is fixed to 4µs.

7.3 VME Control Register + SOIC (0x20)

Short-Adr.+$20	WR Softw. Interrupt Control (soic)	RD VME-Contol-Register (creg)
WORD	D15..D02 = x D01 = 1 = Software Interrupt D00 = 1 = Reset Interrupt-FF	D15 = IACK* D14 = IACKIN* D13 = IACKOUT* D12 = DTACK* D10 = BERR* D11 = AS* D10 = DS0* D08 = DS1* D07 = WRITE* D06 = LWORD* D05 = AM5 D04 = AM4 D03 = AM3 D02 = AM2 D01 = AM1 D00 = AM0

AM0..IACK* will be stored in every VME cycle except HALT or SO-HALT

7.4 VME Adress Register (0x30)

Short-Adr.+$30	WR VME-ADR-Register	RD VME-ADR-Register (areg)
WORD LWORD --- WORD (+$32)		D15..D00 = areg15..01,0 D31..D00 = areg31..01,0 --- D15 = SCLKOK (1 = SYSCLK aktiv) D14 = +5V OK (1 = U > +4,6 V) D13 = +12V-OK (1 = U > +10,6V) D12 = -12V-OK (1 = U > -10,6V) D11 = +5V-OverVoltage (0 = U < +5,5 V) D10..D08 = 0 D07..D00 = areg23..areg16

A31..A01 will be stored in **areg** in every VME cycle except HALT or SO-HALT

7.5 VME Data Register (0x40)

Short-Adr.+$40	WR VME-DATA-Register	RD VME-DATA-Register (dreg)
BYTE WORD LWORD		D15..D00 = dreg15..00 / LB or HB D15..D00 = dreg15..00 D31..D00 = dreg31..00

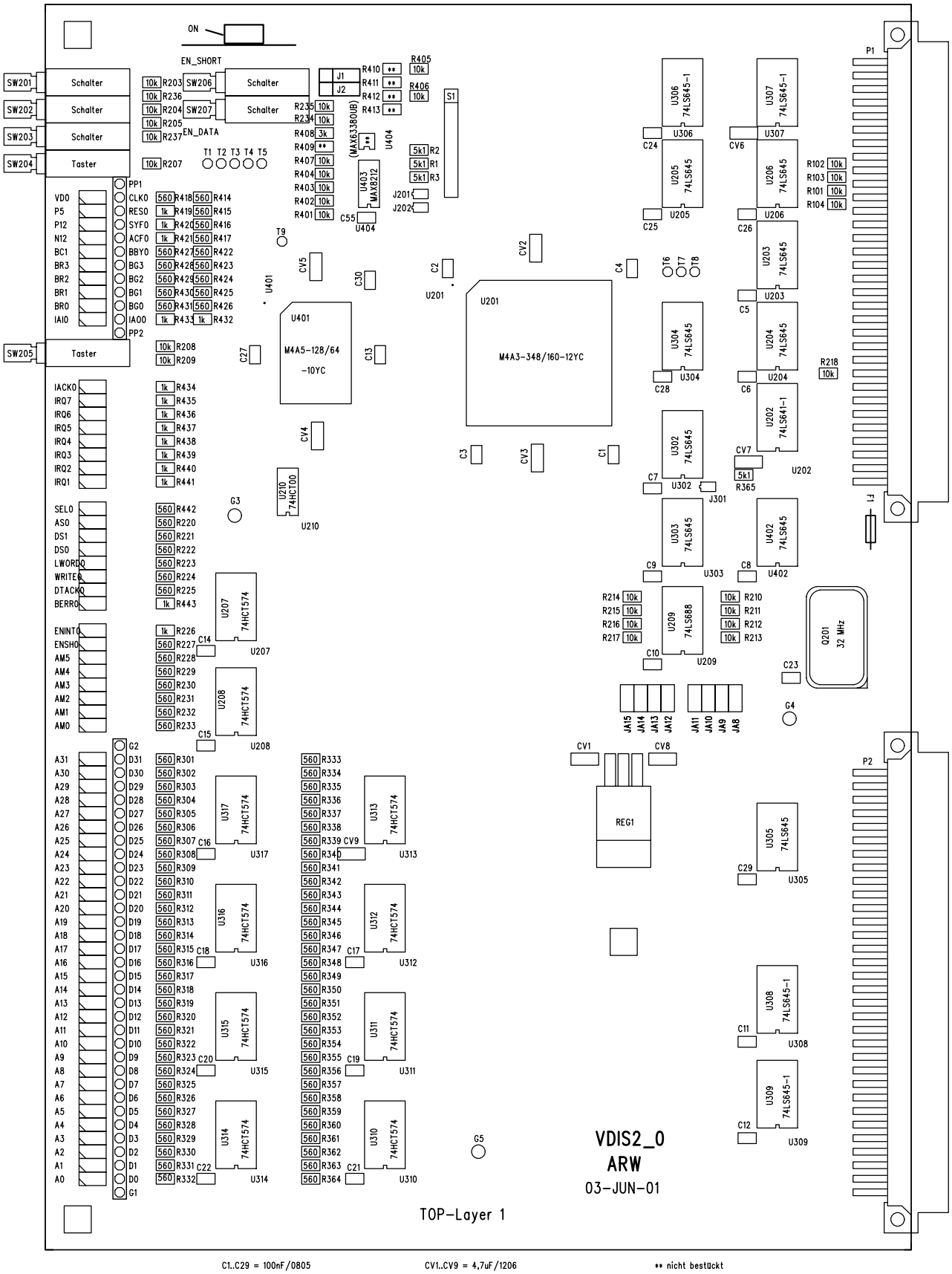
D31..D01 will be stored in **dreg** in every VME cycle except HALT or SO-HALT

7.6 Test Counter (0x80)

Short-Adr.+$80	WR Counter	RD Counter (cnt)
WORD LWORD	Clear Counter (data not used) Clear Counter (data not used)	D15..D00 = cnt15..00 D31..D00 = cnt31..00

The content of cnt will be increased by 1 with each cnt read .

8 VDIS-2 PCB LAYOUT



9 VME-BUS REFERENCE

9.1 VME-bus J1 connector

P1 on the VME module is a male 96-pin DIN 41612 connector (style C) with 3 rows a, b and c:

PIN #	Row A Signal Name	Row B Signal Name	Row C Signal Name
1	D 00	BBSY*	D 08
2	D 0l	BCLR*	D 09
3	D 02	ACFAIL*	D 10
4	D 03	BGOIN*	D 11
5	D 04	BG0OUT*	D 12
6	D 05	BG1IN*	D 13
7	D 06	BG1OUT*	D 14
8	D 07	BG2IN*	D 15
9	GND	BG2OUT*	GND
10	SYSCLK	BG3IN*	SYSFAIL*
11	GND	BG3OUT+	BERR*
12	DS1*	BR0*	SYSRESET*
13	DS0*	BRl *	LWORD*
14	WRITE*	BR2*	AM 5
15	GND	BR3 *	A 23
16	DTACK*	AM 0	A 22
17	GND	AM 1	A 21
18	AS*	AM 2	A 20
19	GND	AM 3	A 19
20	IACK*	GND	A 18
21	IACKIN*	SERCLK	A 17
22	IACKOUT*	SERDAT*	A 16
23	AM 4	GND	A 15
24	A 07	IRQ7*	A14
25	A 06	IRQ6*	A 13
26	A 05	IRQS*	A 12
27	A 04	IRQ4*	A 11
28	A 03	IRQ3 *	A 10
29	A 02	IRQ2*	A 09
30	A 01	IRQ1*	A 08
31	-12V	+5V STBY	+12V
32	+5V	+5V	+5V

9.2 VME-bus J2 Connector

P2 on the VME module is a male 96-pin DIN 41612 connector (style C) with 3 rows a, b and c.

PIN #	Row A Signal Name	Row B Signal Name	Row C Signal Name
1	N.C.	+5V	N.C.
2	N.C.	GND	N.C.
3	N.C..	RESERVED	N.C.
4	N.C.	A 24	N.C.
5	N.C.	A 25	N.C.
6	N.C.	A 26	N.C.
7	N.C.	A 27	N.C.
8	N.C.	A 28	N.C.
9	N.C.	A 29	N.C.
10	N.C.	A 30	N.C.
11	N.C.	A 31	N.C.
12	N.C.	GND	N.C.
13	N.C.	+5V	N.C.
14	N.C.	D 16	N.C.
15	N.C.	D 17	N.C.
16	N.C.	D 18	N.C.
17	N.C.	D 19	N.C.
18	N.C.	D 20	N.C.
19	N.C.	D 21	N.C.
20	N.C.	D 22	N.C.
21	N.C.	D 23	N.C.
22	N.C.	GND	N.C.
23	N.C.	D 24	N.C.
24	N.C.	D 25	N.C.
25	N.C.	D 26	N.C.
26	N.C.	D 27	N.C.
27	N.C.	D 28	N.C.
28	N.C.	D 29	N.C.
29	N.C.	D 30	N.C.
30	N.C.	D 31	N.C.
31	N.C.	GND	N.C.
32	N.C.	+5V	N.C.

N.C. = not connected on VDIS-2
All signals with ' * ' are active in case of a level below the TTL threshold.

9.3 VME-bus address modifiers

Adress Modifier (hex)	Function
3F	Standard Supervisory Block Transfer
3E	Standard Supervisory Programm Access
3D	Standard Supervisory Data Access
3C	Reserved
3B	Standard Nonprivileged Block Transfer
3A	Standard Nonprivileged Programm Access
39	Standard Nonprivileged Data Access
38 .. 2E	Reserved
2D	Short Supervisory Access
2C .. 2A	Reserved
29	Short Nonprivileged Access
28 .. 20	Reserved
1 F .. 10	User-defined
0F	Extended Supervisory Block Transfer
0E	Extended Supervisory Programm Access
0D	Extended Supervisory Data Access
0C	Reserved
0B	Extended Nonprivileged Block Transfer
0A	Extended Nonprivileged Programm Access
09	Extended Nonprivileged Data Access
08 .. 00	Reserved

10 NOTES