1.7 VIC068A Control Register Access

1.7.1 Control Registers

The VIC068A contains 58 8-bit internal registers addressable from the local bus. These registers provide complete control and monitoring of the VIC068A.

1.7.2 Control Register Access

Access to internal registers of the VIC068A is accomplished through the assertion of CS*, PAS* and DS*. It is the value of R/W* that determines if the access is a read or a write.

When CS*, PAS* and DS* are all driven Low (in any order) to the VIC068A, access to an internal register is initiated (i.e., REGISTER_ACCESS* = 0 when (CS*[0] and PAS*[0] and DS*[0]). Register access completes when either CS*, PAS*, or DS* deassert (i.e., REGISTER_ACCESS* = 1 when (CS*[1] or PAS*[1] or DS*[1]). *Figure 1-8* shows a timing diagram of the VIC068A internal register accesses. The timing values are explained in *Table 1-12.*

Table 1-12. Register Access Timing Values

Operation		Commercial		Industrial		Military	
		Min.	Max.	Min.	Max.	Min.	Max.
REGISTER ACCESS							
M1	PAS*[0] & DS*[0] & CS*[0] to DSACKi*[L]	4T+5	5T+34	4T+5	5T+35	4T+4	5T+38
M2	PAS*[0] & DS*[0] & CS*[0] to LD[7:0] Valid	3T+5	4T+28	3T+5	4T+29	3T+4	4T+37
M3	AS*[0] & ICFSEL*[0] to DTACK*[L]	4T+6	4T+30	4T+5	4T+31	4T+5	4T+34
M4	PAS*[0] & DS*[0] & CS*[0] to LD[7:0], LA[7:0] Valid	2T+6	3T+30	2T+5	3T+31	2T+5	3T+34

Although the registers are 8 bits wide, the VIC068A always acknowledges a register access with both DSACK*s. This is because the VIC068A registers are addressed on longword boundaries and occupy 32 bits of address space.

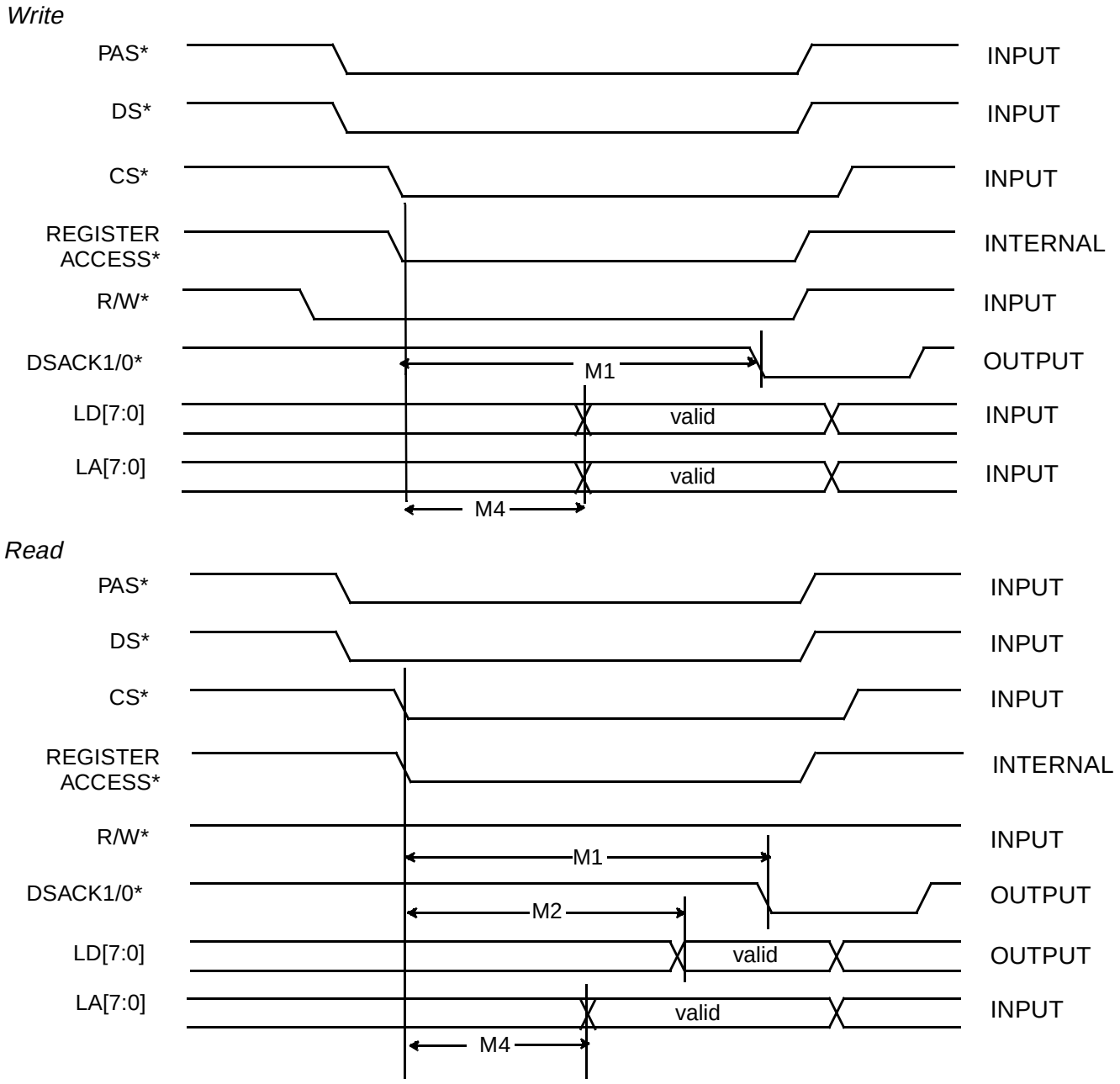

Figure 1-8. VIC068A Internal Register Access Timing

When reading a register, the VIC068A delivers data on LD[7:0]. When writing data, the VIC068A must see data on LD[7:0]. Because of this, the VIC068A only acknowledges a register access that is addressed “correctly” according to the following table:

SIZ1, SIZ0	*VIC068A acknowledges if LA[1:0] is:*
0 0	0 0
0 1	1 1
1 0	1 0
1 1	1 1

This insures that data will be available to/from LD[7:0] according to 68K protocol.

The VIC068A addresses given in this user's guide are byte addresses located at the LA[1:0] = 1 1 position. This implies that if the registers are to be addressed through a longword access, LA[1:0] must be 0 0. If accessed though a word access, LA[1:0] must be 1 0.

For example, if the variable *vic* contains the VIC068A register base address for a particular application, the following Motorola instructions would identically move the DMASR data (address = $BF) to the Motorola D0 register:

```
move.b  (vic,$bf), d0

move.w  (vic,$be), d0

move.l  (vic,$bc), d0
```