PCI 9050
Design Notes Rev. 1.1
January 1999

A. Product Status

Product	Revision	Description	Samples	Production
PCI 9050	PCI 9050-1	Released Silicon	August 1996	October 1996

B. Documentation Status

Document	Revision	Description	Date
Data sheet	Version 1.01	PCI 9050-1 Data Sheet	August 1996

The scope of this document encompasses the PCI 9050 PCI Bus Target Interface Device

1. RD# Signal (Read Strobe), CS[3:0]# (Chip Select)

Design Issue: The PCI 9050 drives all local output signals when it owns the local bus. After it asserts LHOLDA to grant the local to another master, PCI 9050 floats all local output signals. However, PCI 9050 drives the RD# and CS[3:0]# signals at all time. This results in a bus contention when the RD# and CS[3:0]# signals are shared by multiple masters.

Recommendation:

1. Tri-state RD# and CS[3:0]# from the PCI 9050 through an external 74LS125 (LHOLDA is used as a gate signal).

2. Add an external multiplexer to RD# and CS[3:0]# signals and use LHOLDA as the select signal.

Note: Items 1 & 2 both require local output signals to be pulled up or pulled down to an inactive state.

2. Blank Serial EEPROM and Default Value for PCI Target Retry Delayed Clock

Design Issue: The PCI Target Retry Delayed Clock determines the number of PCI clocks (multiplied by 8) after the beginning of a direct slave cycle until a retry is issued. The default value for PCI Target Retry Delayed Clock is 0 and 64K of memory for the Expansion ROM Space. If a blank serial EEPROM is used, the PCI bus will get continuous retry when the PCI 9050 tries to look for the Expansion ROM on the local bus.

Recommendation:

1. The PCI 9050 application must be accompanied by a pre-programmed serial EEPROM and the PCI Target Retry Delayed Clock value equals or greater than 3 (multiplied by 8).

2. The PCI 9050 application must be accompanied by a pre-programmed serial EEPROM with the PCI Read mode (Delayed Read) bit set.

3. Floating Local Signals

Design Issue: PCI 9050 floats all local output and input/output signal when it does not drive the local bus.

Recommendation:

To prevent this, keep these signals in an in-active mode, external pull-up on control signals such as, LA[27:0], LAD[31:0], ADS#, LW/R#, CS[3:0]#, RD#, and WR# and external pull-down on ALE are recommended.

4. Delayed Read Retry/Disconnect

Design Issue: During Delayed Direct Slave Reads, if the delayed read mode bit, CNTRL[24] is set, the PCI 9050 will treat all PCI Delayed Read as Retries, which may allow for a second chance for the initial Master to complete the requested Read cycle. Any subsequent Direct Slave cycles to a different address other then from the address when the disconnect occurred will be retried until PCI address matches or a 32K clock timeout occurs.

Recommendations:

1. Software should recover from disconnect by retrying the initially requested Read cycle.
2. Software should wait for 32K clock timeout to occur before posting any other Reads to the PCI 9050.