1.1 Introduction to the VIC068A

1.1.1 Description

The Cypress Semiconductor VMEbus Interface Controller, VIC068A, is a single, integrated circuit designed to minimize the cost and board-area requirements of VMEbus boards, while at the same time maximizing their performance. The VIC068A was designed using Cypress's high-performance standard cells on a CMOS process. The VIC068A provides all VMEbus system controller functions plus many other features that simplify the development of VMEbus-based modules. The VIC068A utilizes Cypress's patented and military-approved high-drive CMOS drivers. These CMOS drivers connect directly to the VMEbus signal pins.

The VIC068A was developed through the joint efforts of Cypress Semiconductor and the VMEbus Technology Consortium under the auspices of the VMEbus International Trade Association (VITA). Because of this cooperation, the VIC068A offers an implementation that provides the broadest feature set and multi-vendor compatibility available on the market.

A block diagram of the VIC068A is shown in *Figure 1-1*. A typical 68030 application is shown in *Figure 1-2.*

1.1.2 Features Summary

The complete VMEbus Interface Controller and Arbiter includes

- PRI, SGL, and RRS arbitration
- the capability to drive arbitration signals directly
- arbitration timeout timer
- VMEbus timeout timer
- the capability to drive BGOUT*, IACK* daisy-chain

The complete VMEbus Master Interface includes

- five release modes
- write posting
- indivisible cycle support
- deadlock detection
- fair requesting

- user-defined AM code generation

The complete VMEbus Slave Interface includes

- write posting
- configurable local access timing
- slave block transfer support

Interleaved Block Transfer support includes

- block transfers with local DMA
- programmable transfer length, burst length, interleave period, and access timing
- “dual-path” option

The compete VMEbus, Local Interrupt Handler/Generator includes

- seven local interrupt signals
- seven VMEbus interrupt signals
- seven-level local encoding
- error/status interrupts
- periodic “heartbeat” interrupt

Interprocessor Communication Support includes

- four global mailbox interrupts
- four module mailbox interrupts
- five mailbox registers

Other features include

- local DRAM refresh control
- local timeout timer
- “turbo” mode
- programmable metastability delay

The VIC068A meets the IEEE VMEbus Specification 1014 Rev C.1.

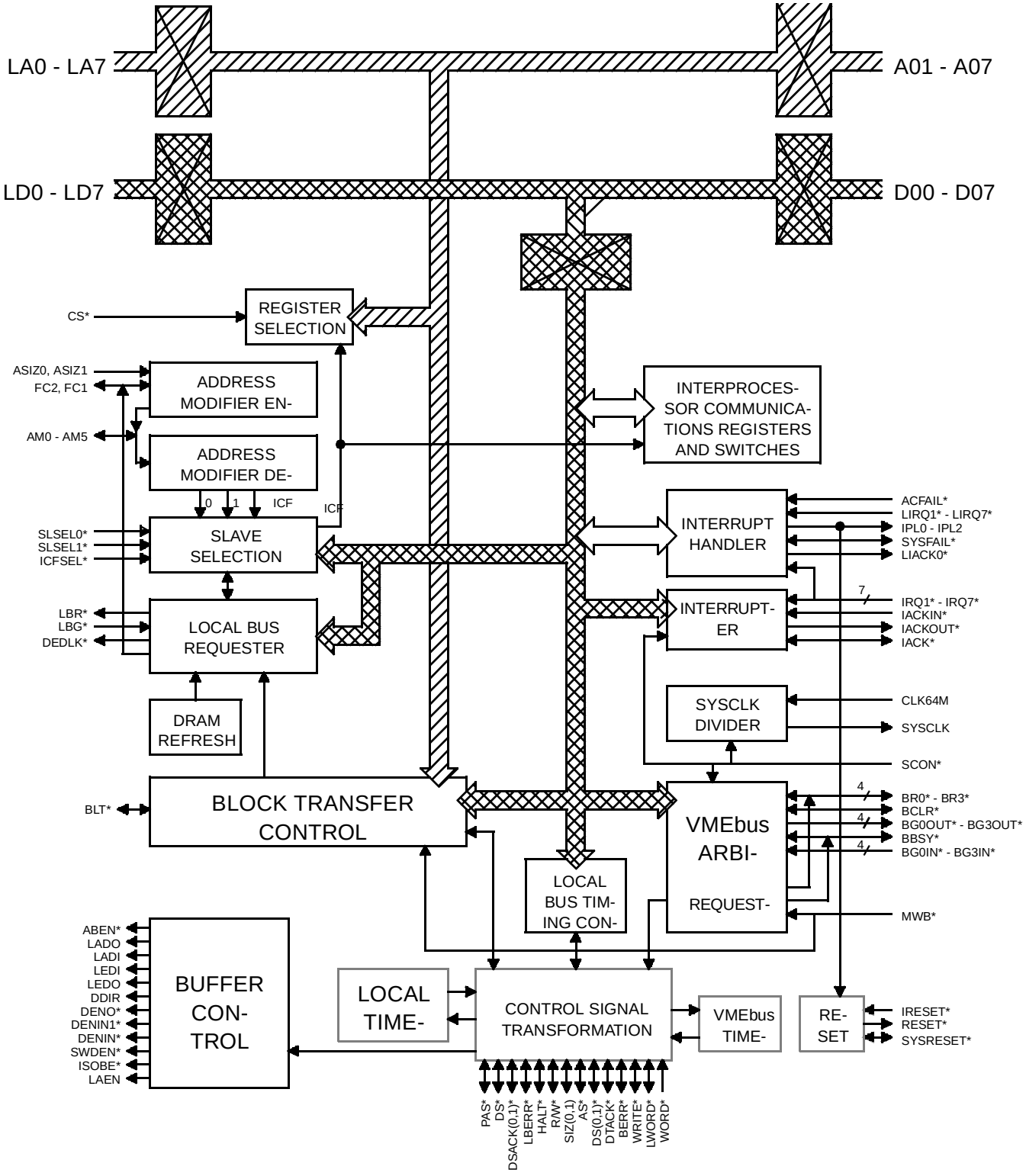

Figure 1-1. VIC068A Block Diagram

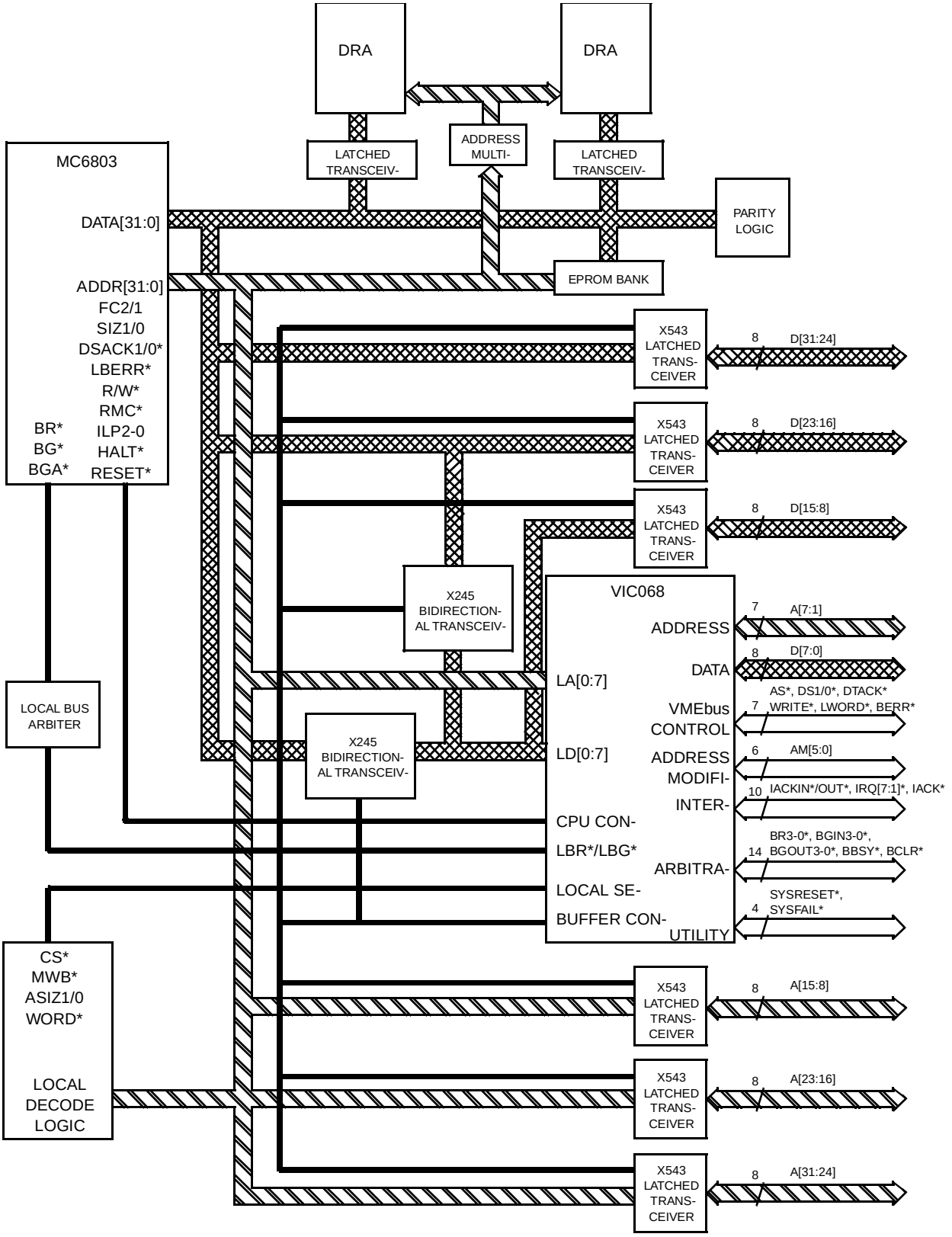

Figure 1-2. VIC068A on 68030 Board