1.8 Interprocessor Communication Facilities

The VIC068A contains three categories of interprocessor communication facilities (ICFs):

- Interprocessor Communication Registers (ICRs)
- Interprocessor Communication Global Switches (ICGSs)
- Interprocessor Communication Module Switches (ICMSs)

The ICRs are 8-bit registers that may be accessed from either the local bus or the VMEbus.

The ICGSs and the ICMSs are switches that may be set to interrupt the local processor.

These facilities are located in seven registers that are visible from both the local bus and the VMEbus. When accessed via the local bus, the registers are read/written by normal VIC068A register access methods. When accessed via the VMEbus, the ICFSEL* signal is used as a register select signal. The register addresses, when accessed from the local bus are not the same as when accessed from the VMEbus. The VIC068A contains an internal arbiter to arbitrate between local and VMEbus accesses to these facilities.

Additional registers used for the ICFs are as follows:

- ICGS Interrupt Control Register (ICGSICR)
- ICMS Interrupt Control Register (ICMSICR)
- ICGS Interrupt Vector Base Register (ICGSIVBR)
- ICMS Interrupt Vector Base Register (ICMSIVBR)
- Interprocessor Communication Switch Register (ICSR)

1.8.1 Valid ICF Selection

The ICFSEL* signal is used to signal that the VMEbus master desires access to the VIC068A interprocessor communication facilities. This signal is usually driven from VMEbus address decoders. When ICFSEL* is asserted, the VIC068A checks A[5:1] to determine what ICF is desired. Self-access to the ICF facilities is not detected by the VIC068A. The VIC068A then verifies the AM codes against the following table:

ICF	*AM code(s)*
ICR	$29, $2D (A16, user or supervisory data)
ICGS	$2D (A16, supervisory data)
ICMS	$29, $2D (A16, user or supervisory data)

Once a valid ICF select has occurred, the VIC068A then processes the request. The ICF VMEbus address is shown in *Table 1-13*.

Table 1-13. ICF VMEbus Address Map

A7	A6	A5	A4	A3	A2	A1	LWORD	Function
X	X	0	0	0	0	0	1	ICR0 Access
X	X	0	0	0	0	1	1	ICR1 Access
X	X	0	0	0	1	0	1	ICR2 Access
X	X	0	0	0	1	1	1	ICR3 Access
X	X	0	0	1	0	0	1	ICR4 Access
X	X	0	0	1	0	1	1	ICR5 Access
X	X	0	0	1	1	0	1	ICR6 Access
X	X	0	0	1	1	1	1	ICR7 Access
X	X	0	1	0	0	0	0	Clear ICGS0
X	X	0	1	0	0	0	1	Set ICGS0
X	X	0	1	0	0	1	0	Clear ICGS1
X	X	0	1	0	0	1	1	Set ICGS1
X	X	0	1	0	1	0	0	Clear ICGS2
X	X	0	1	0	1	0	1	Set ICGS2
X	X	0	1	0	1	1	0	Clear ICGS3
X	X	0	1	0	1	1	1	Set ICGS3
X	X	1	0	0	0	0	0	Clear ICMS0
X	X	1	0	0	0	0	1	Set ICMS0
X	X	1	0	0	0	1	0	Clear ICMS1
X	X	1	0	0	0	1	1	Set ICMS1
X	X	1	0	0	1	0	0	Clear ICMS2
X	X	1	0	0	1	0	1	Set ICMS2
X	X	1	0	0	1	1	0	Clear ICMS3
X	X	1	0	0	1	1	1	Set ICMS3
X	X	1	1	X	X	X	X	Undefined/Reserved

1.8.2 Interprocessor Communication Registers

The VIC068A contains seven interprocessor communication registers (ICRs). These registers are accessible from both the local bus and the VMEbus. ICRs 4–0 are considered general-purpose read/write registers. ICR5 is the VIC068A version/revision register. The value of this register indicates the mask revision of the device. ICR6 contains HALT* and RESET* status of the VIC068A. ICR7 provides semaphores for ICRs 5–0. These sema-

phores are set whenever ICRs 5–0 are written. In addition, ICR7 also indicates VMEbus mastership and a mask for SYSFAIL*. Refer to Chapter 1.12 for detailed register descriptions.

1.8.3 Interprocessor Communication Global Switches

The ICGSs are software switches that may be set over the VMEbus to interrupt a group of VMEbus modules.

When the VIC068A issues the global switches, it is performing a VMEbus byte-wide write to the pre-defined global switch address.

If the global switch interrupts are enabled in the ICGSICR of the VIC068A slave, a local interrupt is generated on a clear-to-set transition of the selected switch. When acknowledged (FCIACK* asserted), the slave VIC068A handles the interrupt by returning the status/ID value from the ICGSVBR. See Chapter 1.9 for details on VIC068A interrupt generation and handling. Once a switch is set, it must be cleared before it can be re-set.

Because the global switches are meant to be issued to several modules, the VIC068A as VMEbus master must assert DTACK* to complete the VMEbus cycle. The VIC068A issues DTACK* if the ICFSEL* signal is asserted while performing the VMEbus master cycle.

Notice that if a valid ICF select has occurred, A[2:1] selects the ICGS switch and A0 (i.e., DS1* and DS0*) indicates whether the switch is to be set or cleared. That is, a byte-wide write to an even address clears the selected switch and a byte-wide write to an odd address sets the selected switch.

The ICSR may be used to provide monitoring of the global switches.

1.8.4 Interprocessor Communication Module Switches

Like the ICGSs, the ICMSs are software switches that may be set over the VMEbus to interrupt the local processor. The module switches, however, are meant to be issued to a specific module.

As in the global switches, the VIC068A issuing the module switches performs a VMEbus byte-wide write to the pre-defined switch address.

Because the module switches are meant for a specific module, the VIC068A as VMEbus slave (the module whose switch was just set) must assert the DTACK*. The VIC068A issuing the ICMS need not have its ICFSEL* signal asserted.

The interrupt and addressing mechanisms are the same for ICMSs as they were for ICGSs.

The ICSR may be used to provide monitoring of the module switches. Unlike the global switches, this register may be written by local resources to interrupt the CPU.