PCI 9050

Errata Rev. 1.1
January 1999

A. Product Status

Product	Revision	Description	Samples	Production
PCI 9050	PCI 9050-1	Released Silicon	August 1996	October 1996

B. Documentation Status

Document	Revision	Description	Date
Data sheet	Version 1.01	PCI 9050-1 Data Sheet	August 1996

The scope of this document encompasses the PCI 9050 PCI Bus Target Interface Device.

1. Reads from Local Configuration Registers

Problem: If bit 7 of the base address for the I/O or Memory mapped Configuration Registers (PCI configuration register offset 14h or 10h) is set to 1, the local configuration registers can not be read. Under this condition, they will all return zeroes when the PCI master (typically the host) attempts to read them. They can be written to from both the PCI master and the EEPROM. In other words, the information is correctly written into the local configuration registers, but it can not be read the PCI Master. If bit 7 is set to 0, the local configuration registers can be read correctly. In a PCI system, the BIOS determines the base address (i.e. sets the value of bit 7) during the initial configuration cycle.

Solution/workaround:

1. During adapter hardware and driver development, it may be desirable to read the configuration registers to confirm that the local configuration registers were programmed properly. If the BIOS have bit 7 set to 0, a PCI master can read these registers. If the BIOS has set bit 7 to 1, change the base address of the memory or I/O mapped local configuration registers so that bit 7 is de-asserted. This value can be easily changed by writing to offsets 10h and 14h, which hold the base address. For example, say the host assign a value of 0000FC81h to I/O mapped local configuration register (PCR 14h). Use PLXMON (9050RDK) or your own driver to change this base address to 0000FC01h (type PCR 14 0000FC01 at the PLXMON command prompt).

2. Assign 256 bytes of I/O spaces to one of the un-used Local Spaces in the Serial EEPROM. Swap the PCI Base for the un-used Local Address Spaces to PCI Base Address 1 for I/O Mapped Configuration Registers after the system booted.

Impact:

In the production phase, for some types of adapters it is never necessary to read the local configuration registers. In these cases, this errata has no impact. However, in some situations, it is desirable to read the local configuration registers. Situations, which are impacted, are;

1. Interrupt Status. If there is only one local interrupt source, the errata has no impact. However, if there are two local interrupt sources, the PCI master can not read the local configuration registers to determine where the interrupt come from. In this case, the interrupt status should be stored in local memory or an on-board register. The PCI master should read the status from the local memory or register.
2. User Inputs (1,2,3, and 4), used for transferring bit or status data from the local side. If messages need to be passed to the host, a section of local memory can be defined and a direct slave read access could be made to retrieve the data.
3. Serial EEPRM read and valid bits, for host initiated read from an external serial EEPROM. This mode is generally used only in development.

2. Expansion ROM Space Enable

Problem: If the PCI BIOS does not set the Expansion ROM Space enable bit in the PCI 9050 during initialization, the PCI 9050 will return all 0's for the range, indicating that there is no Expansion ROM. This problem applies only to boards that need to use Expansion ROM Space.

Solution/workaround:

Most standard PCI BIOS do not set the enable bit during initialization. Therefore, to use an Expansion ROM, in most cases requires modification to the BIOS.

3. Delayed read during 32K PCI clocks timeout

Problem: As per PCI spec, when a master performs a delayed read, it must complete that delayed read. When a delayed read is not completed within 32K PCI clocks, the target with the pending delayed read should discard it. (protect against violations or PCI 2.0 devices). There is a one-clock window (last clock of 32K timeout) in which the PCI 9050 is discarding the delayed read. During this 1clock window, new PCI cycles are not monitored. If a new

PCI cycle is begun during that 1 clock window, the PCI 9050 ignores the PCI cycle. Therefore, a master abort will occur on the PCI bus.

Solution/Workaround:

This is an extremely rare occurrence. If you encounter it, software should recover both the timeout and master abort with a retry.

4. LOCK# de-assertion during an idle phase

Problem: If a locked operation is done to the PCI 9050 and the LOCK# signal is de-asserted during an idle phase, the PCI 9050 has a one clock window in which it is loading LOCK# de-assertion condition into its FIFO. If a new PCI access (FRAME_ asserted) to the PCI 9050 occurs 1 clock after the LOCK# signal is de-asserted, the PCI 9050 will ignore it (master abort). This will occur because the PCI 9050 has not acknowledged the LOCK# de-assertion condition.

Solution/Workaround:

This is an extremely rare occurrence. If you encounter it, software should recover the master abort with a retry.