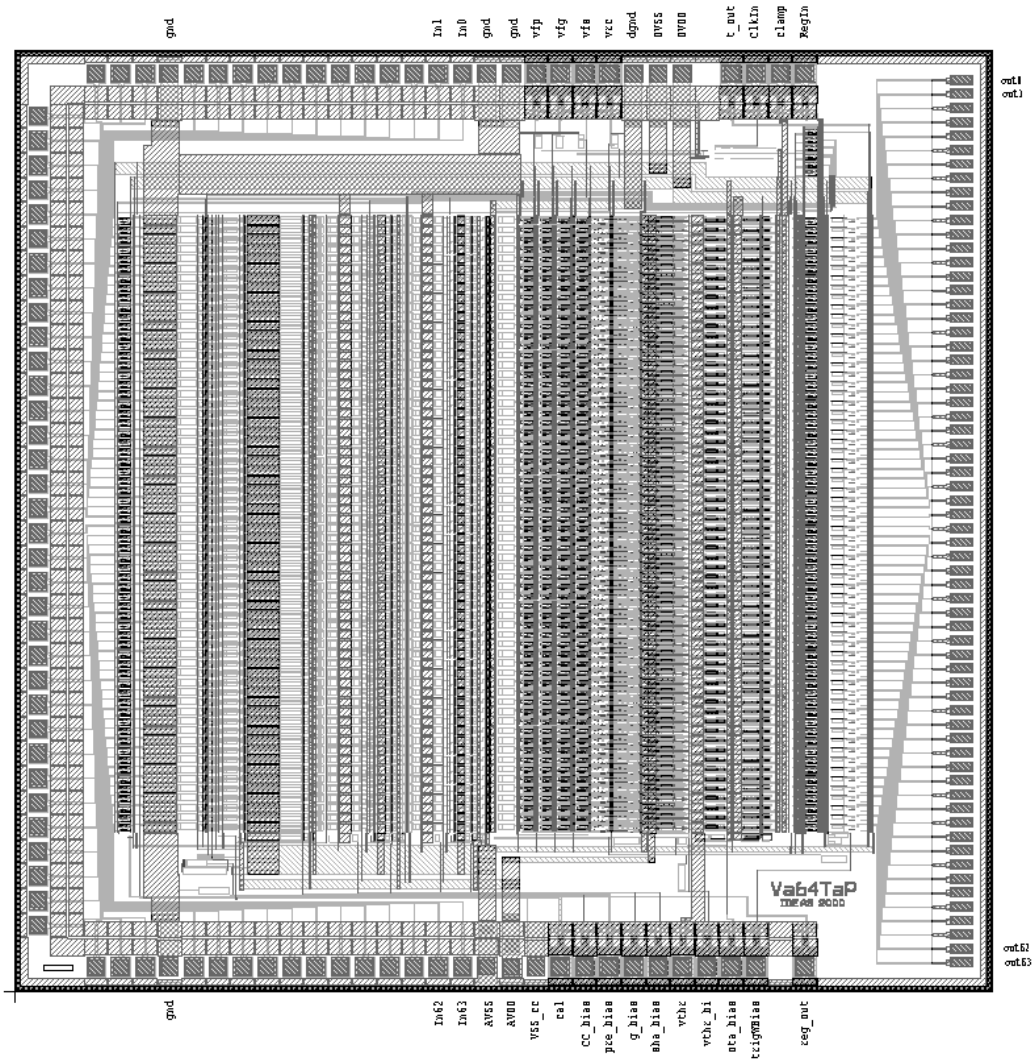
VA64TAP

Documentation v0.94



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General

The Va64Tap is a low-power, low noise ASIC optimised for moderate detector capacitances (~10pF). The preamplifier has high gain. There is a gain-stage after the preamplifier, which is possible to disable with a bit in the control register. The output of the gain stage/preamplifier is filtered by a CR-RC fast shaper with a peaking time of 75ns. Each channel has a discriminator, with a 4-bit trim-DAC to reduce threshold spread. The ASIC has 64 parallel trigger outputs, one for each channel. The trigger is encoded as a current, and should be terminated with low impedance.

Physical

- Process: 0.8 µm N-well CMOS, double-poly, double metal.
- Die size: 5605 µm x 5380 µm
  Thickness: ~ 600 µm
- Input bonding pads: Single row on three sides.
  Pad size: 90 µm x 90 µm
  Pad pitch: 140µm (see. fig. 2)
- Output pads: Single row on one side.
  Pad size: 50 µm x 120 µm
  Pad pitch: 80 µm (see fig. 2)
- Control and power pads: Single row on upper and lower side.
  Pad size: 90 µm x 90 µm
  Pad pitch: 140 µm (see fig. 2)

Highlights of specs

- ENC: 500e- @ 10pF and 75ns Tp
- Threshold uniformity: ±200e-
- Threshold nominal value: 3000e-
- Fall time shaper: <10% @200ns

Pad Description

The output, control and power pads are listed clockwise from the upper left. Positive current direction into the chip. All voltages assumes an ASIC powered with VDD and VSS as described in the table.

Pad name	Type	Description	Nominal value	Nominal voltage (for cur. biases)
Gnd (3)	p	Signal ground	0 V	
vfp	ai	Control voltage to feedback resistance in pre-amplifier. Internally generated.	-123mV	
vfg	ai	Control voltage to feedback resistance in gain stage. Internally generated.	-90mV	
vfs	ai	Control voltage to feedback resistance in shaper-amplifier. Internally generated.	750mV	
Vrc	ai	Control voltage for High-pass filter resistor (NMOS) in front of Discrim. Internally generated.	1.4V	
Dgnd	p	Ground	0 V	
dvss	p	Digital Vss	-2 V	
dvdd	p	Digital Vdd	+2 V	
T_out	do	Common trigger output for all channels. Open drain current into the chip. Switchable with control bit.	Logical, current	
Clkin	di	Clock Input for register	Logical	
clamp	p	Reference for the voltage swing reduction of the discriminator outputs.	0 V	
Reg_in	Di	Input to the register	Logical	
Reg_out	D0	Output of register	Logical	
Twbi	Ai	Bias adjust for trigger width. Internally generated.	-4 µA	760mV
Obi	Ai	Bias current to Discriminator. Internally generated.	+120 µA	-895mV
Ref_bi	Ai	Bias for trim-DACs. Internally generated.	+10µA	-880mV
Vthr	Ai	Discriminator threshold	± 50mV (e.g)	
sha_bias	ai	Bias current for shaper-amplifiers. Internally generated.	+120 µA	-440mV
g_bias	ai	Bias current for shaper-amplifiers. Internally generated.	+120 µA	-440mV
pre_bias	ai	Bias current for pre-amplifiers. Internally generated.	+500 µA	-445mV
CC_bias	ai	Bias Leak-current compensation. Internally generated.	+2µA	880mV
cal	ai	Test input signal	1 MIP	
VSS_CC	p	=AVSS filtered (~ no current)	-2V	
avdd	p	Analogue Vdd	+2 V	
avss	p	Analogue Vss (+ chip backplane)	-2 V	

p = power, di = digital in, do = digital out, ai = analogue in, ao = analogue out

Functional description

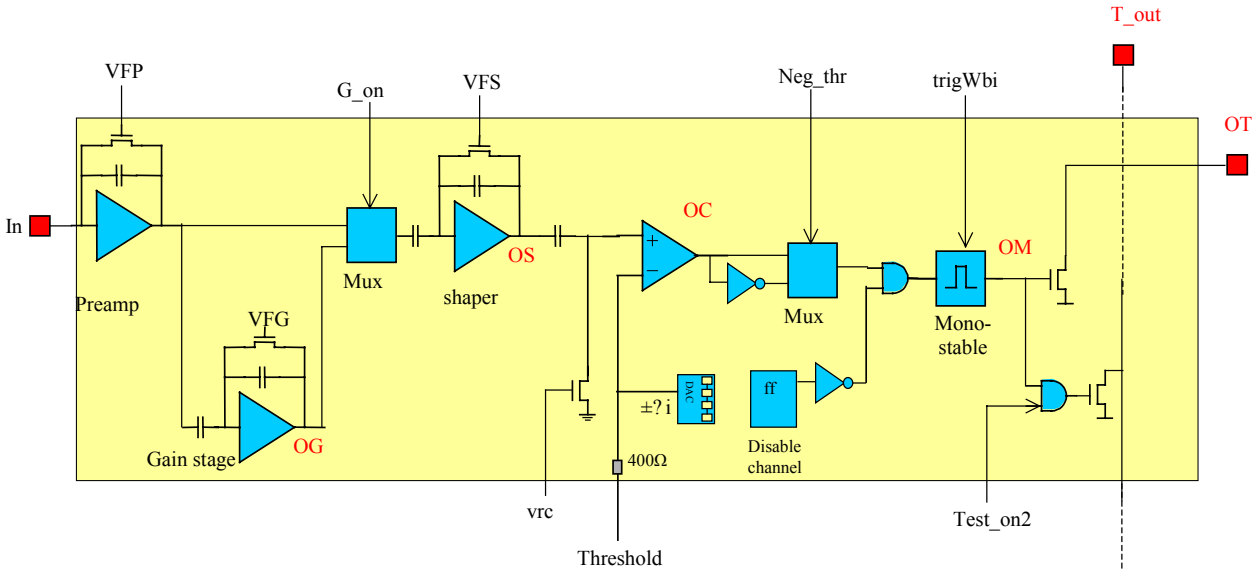


Fig 5. VA64Tap Channel Architecture

The Va64Tap channel is shown in the figure above. After the preamplifier, the signal path is split in two. Depending on the setting of the global control bit "*g_on*", the input of the shaper is connected to either the preamp or the gain stage. The gain stage has inverting gain, meaning that the polarity of the threshold and the value of the control bit "*neg_thr*" need to be changed. The noise filtering shaper has a peaking time of ~70ns. A high pass filter is situated after the shaper to remove offsets on the input signal to the discriminator. The Discriminator offset is also reduced by a 4 bit trim-DAC. The trim-DAC adds or subtracts current through a resistor placed in series with the global on-chip threshold line. The DAC has 1 mV steps with nominal biases. When tuning the DACs, optimal performance is obtained if the current from the trim-DACs in the various channels zeros out, meaning no net current is flowing out of the chip.

The discriminator output *OC* should be inverted by selecting the inverted output if the discriminator threshold is negative. This is done by setting the control bit "neg_thr".

Setting the according channel bit in the disable register can disable any channel. If the channel is not disabled, a signal that triggers the discriminator will be formed into a pulse with a duration controlled by the "*trigWbias*". The parallel trigger output *OT* is an open-drain current that should be terminated with a low impedance in order to avoid pick-up in other channels. It can be connected directly to the input of the LS64 ASIC.

An additional feature is implemented in the channel to facilitate testing. If the global control register bit *test_on2* is set, an additional trigger output *t_out* is enabled. The t_out is available

through an external pad. This node is connected to all channels in parallel, meaning that a trigger on any channel will be possible to monitor on this line.

Adjusting the return to baseline

The most important parameters for adjusting the return to baseline for the system, is the peaking time, the high pass filter before the discriminator and the pulse width of the trigger.

Adjusting the peaking time

The shaping time can be adjusted externally by the two bias-pads *Vfs* and *sha_bias*. Adjusting one will influence the effect of the other.

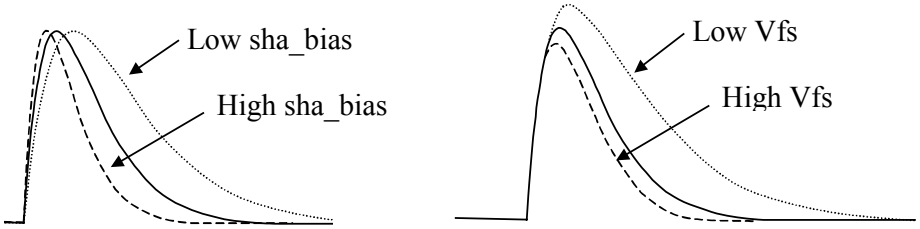
Changing the sha_bias will change the dc-level of the input (since the Vgs of the input PMOS transistor has to increase/decrease as response to the change in current). This dc-level represents the source-voltage of the feedback NMOS transistor, and with an unchanged *Vfs*, the Vgs of this transistor will consequently change. Therefore, to maintain the same resistance value, *Vfs* must change in correspondance to the change in the input dc-level caused by a change in *sha_bias*.

This will consequently affect the shaper output signal in two ways:

1. The change in feedback resistance will cause a change in the time-constant of discharding the feedback capacitor meaning that the differentiation time, or fall-time, will change. Reduced resistance (increase of *sha_bias*) will cause a shorter fall-time and vice versa.
2. Changing sha_bias will also affect the rise-time of the shape because the transconductance of the input transistor will change. Increase of *sha_bias* will cause faster rise-time and vice versa. Consequently, combining this with the previous point, an increase of *sha_bias* will increase the rise-time and decrease the fall-time which will reduce the peaking-time.

Only changing the *Vfs* (keeping *sha_bias* constant) will affect only the fall-time but the effect will be stronger.

A good shape depends on the requirements. Nominally, the shape should be an ideal semigaussian CR-RC shape, but it is not necessarily so. Generally, it is advantageous to minimize the “tail” of the signal (fall-time) since this part conserves the DC component of the signal and hence a long tail will make the amplifier more sensitive to the parallel noise (detector leakage-current noise and biasing-resistor noise).



Only adjusting sha_bias Only adjusting Vfs

Clearly, the desired shape will most often be found by adjusting both parameters.

Adjusting the peaking time

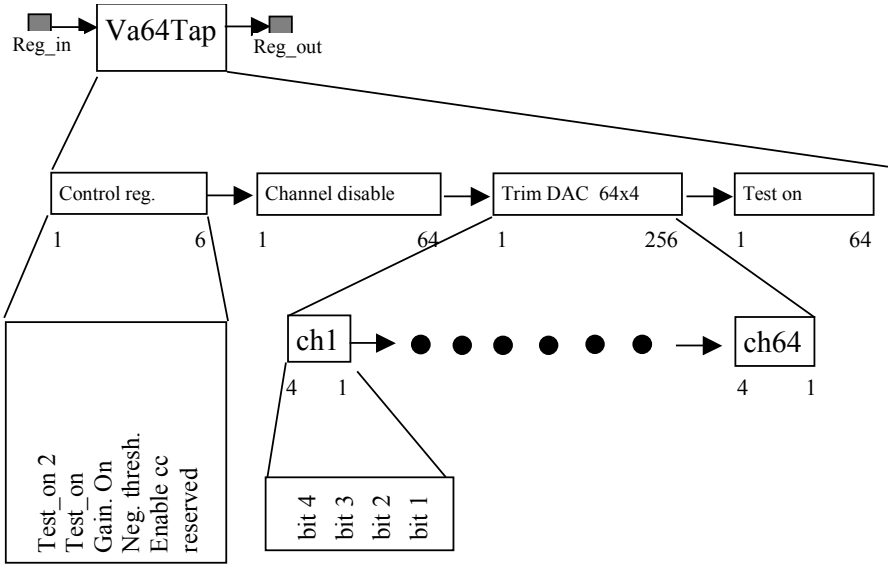
The high-pass filter in front of the discriminator should be optimised in order to make sure that it does not affect the return to base line. The time constant of the filter should be as low as possible without intorducing damping of the signal. The resistance of the filter is implemented with a NMOS connected to DGND. The resistance can be tuned through the *Vrc* bias pad. To reduce the resistance, increase the voltage.

Adjusting the trigger pulse width

The pulse width of the ASIC output signal should be made short enough to not introduce any ambiguity to which cycle it belongs. The default pulse width is 50nS. The pulse width is inversed proportional with the *trigWbi* bias. Thus, increasing the bias will give a shorter duration of the output pulse.

Control register

Clocking in a serial bit pattern sets the ASIC registers.



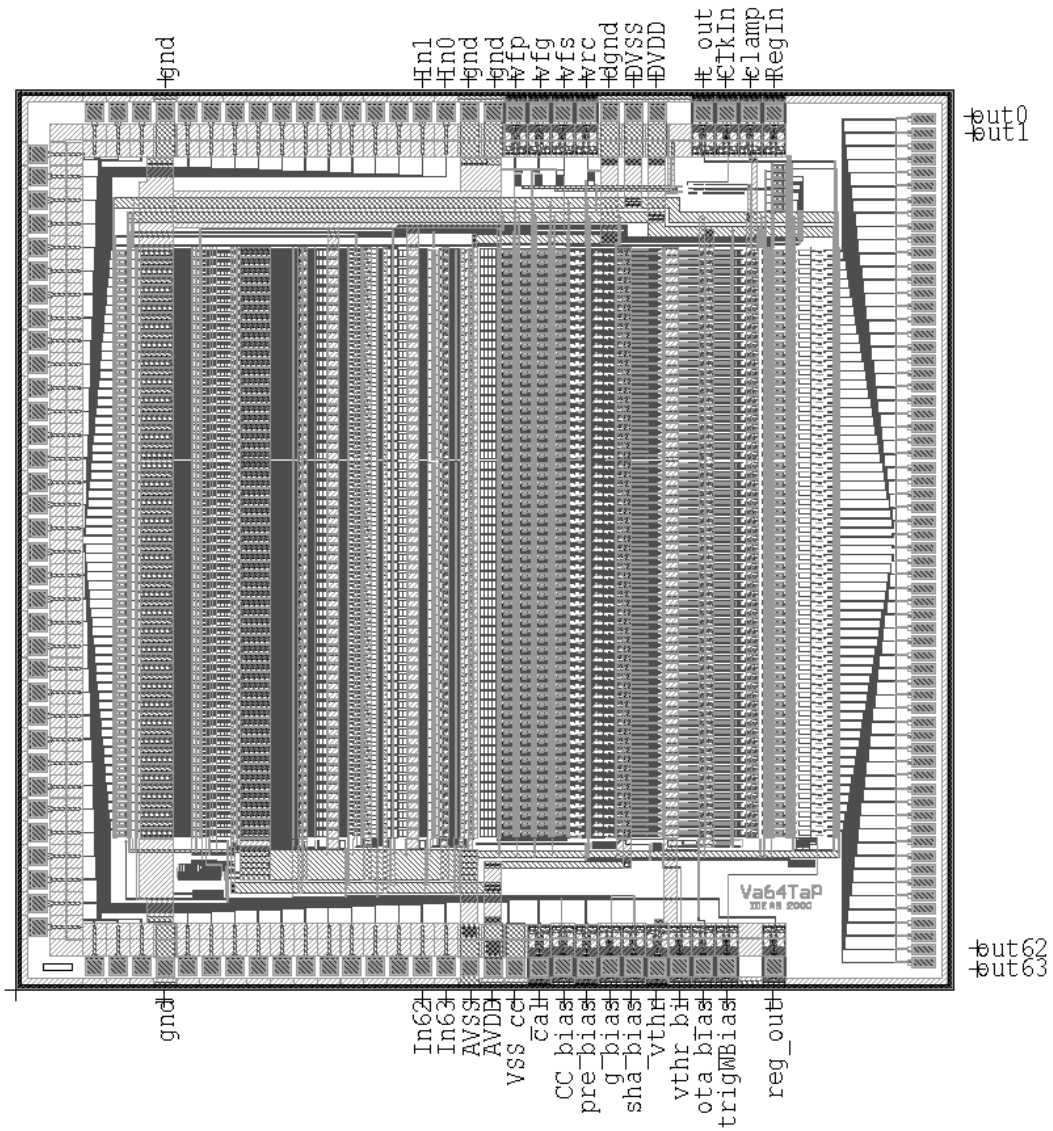
Thus the first bit clocked in on reg_in is Test_on ch 64 on ASIC 3, then subsequent bits comes in accordance with the figure above.

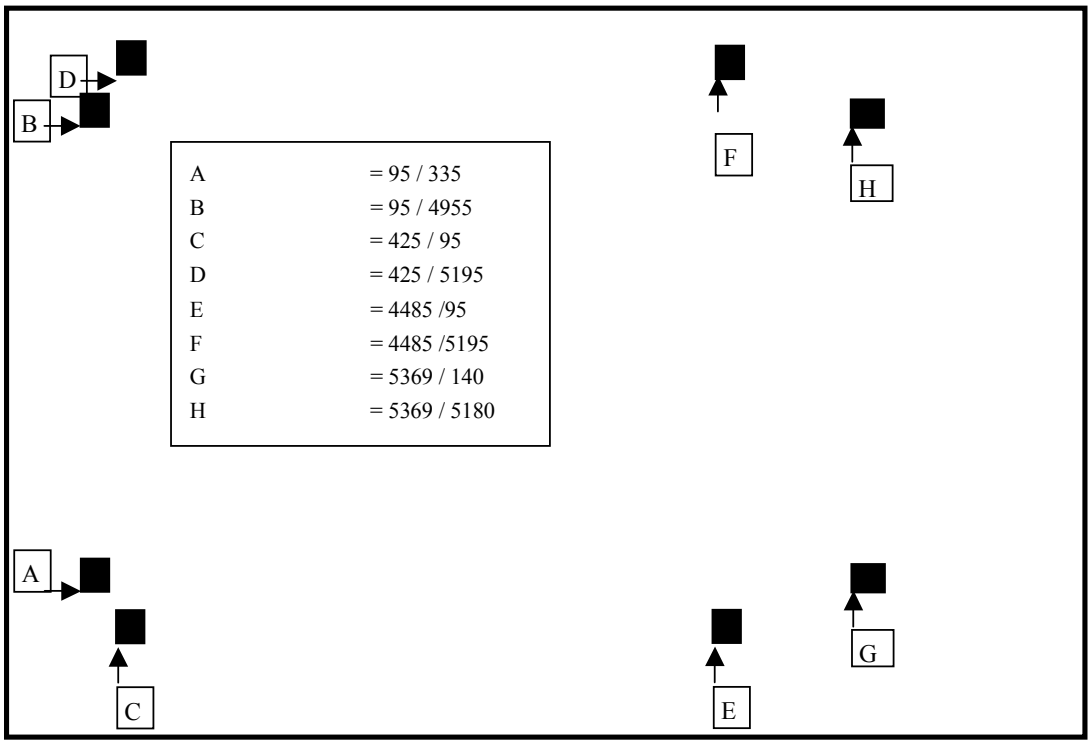
Control register

Test on 2 is used for parallel testing and Test on is for single channel testing. Gain on and negative threshold relate the threshold voltage polarity.

Input signal	Positive	Positive	Negative	Negative
Gain_on	0	1	0	1
Neg_thr	0	1	1	0
Threshold polarity	Positive	Negative	Negative	Positive

Enable cc Enables current compensation. Reserved is always set to ‘0’.


gnd
Hn1
Hn0
gnd
gnd
Vfp
Vfg
Vfs
Vrrc
dgnd
DVSS
DVDD
t_out
CtrlIn
clamp
RegIn
out0
out1
out62
out63
gnd
In62
In63
AVSS
AVDD
Vss_cc
cal
CC_bias
pre_bias
g_bias
sha_bias
_vthr
vthr_bi
ota_bias
trigWBias
reg_out
Va64TaP



Chip geometry & pad placement (Not to scale - all dimensions in µm.
Please note that the referred co-ordinates are layout co-ordinates.
Add 50-100 µm on each side for scribe/cutting tolerances).

Trim DAC bits

Bit1	Bit2	Bit3	Bit4	Offset change (mV)
0	0	0	0	None
0	0	0	1	- 1
0	0	1	0	- 2
0	0	1	1	- 3
0	1	0	0	-4
0	1	0	1	-5
0	1	1	0	-6
0	1	1	1	-7
1	0	0	0	None
1	0	0	1	+ 1
1	0	1	0	+ 2
1	0	1	1	+ 3
1	1	0	0	+4
1	1	0	1	+5
1	1	1	0	+6
1	1	1	1	+7