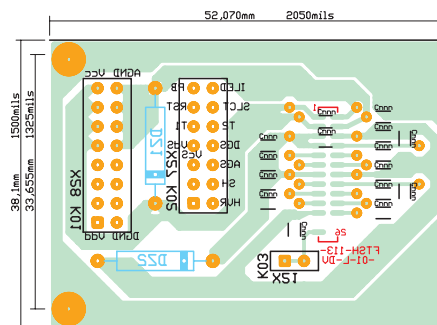


TPPF1-D PCB, ver.1

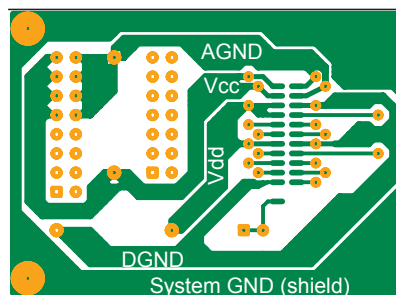
(1 cell, actual config. 3x3)

2003.11.10.

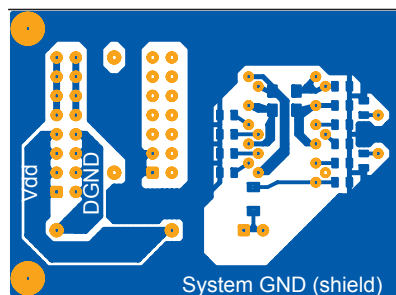


Top Layer (2)

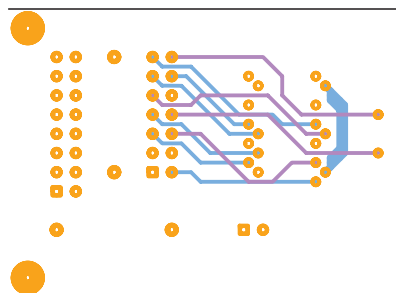
Component layout :
red - top layer, black - bottom layer
(zeners optional)



Top Layer (2)



Bottom Layer (1)



Layer 4