TPPF1-C PCB Test Methods, Specifications And Limits

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1) Test of the isolation between any two lines

The test sequentially activates each line to 5 V via a 220 kΩ resistor and checks all other lines for possible error (> 300 mV). The test is sensitive enough to detect and discriminate :

a) a short or R up to 2 MΩ between any two lines or ground

b) voltage limiter sense resistors presence between Vcc-Agnd and Vdd-Dgnd

2) High-voltage test

a) sustained 500 V dc test for 10 s on the HV-Bias line (risetime 0.5 s)

b) leakage current from HV-Bias to HV-return (0 V reference) at 500 V dc, range $I_{\mathrm{lkmax}} = 10\ \mu$A, resolution 0.3 nA, error threshold 25 nA (equivalent to 20 GΩ)

c) leakage current from HV-Bias to system ground (Shield) at 500 V dc, range $I_{\mathrm{lkmax}} = 10\ \mu$A, resolution 0.3 nA, error threshold 25 nA (equivalent to 20 GΩ)

All other lines are shorted to ground, so a leakage to any other line shows up as increased ground leakage current (although, by PCB design, all other lines are shielded by either HV-return or ground).

3) Trace resistance test

4-point Kelvin resistance measurement between the input and output connectors ; each line is sequentially activated by 100 mA and the voltage drop is measured by a 2 V range, 100 μV resolution ADC, resulting in a 20 Ω range and 1 mΩ resolution, with absolute error < 0.5 %.

4) Voltage limiter threshold test (TPPF1-C pcbs)

Each voltage limiter is activated for 300ms by a 300mA current and the maximum overshoot at the start and a 50ms average final level are recorded. Error tolerance is -100mV / +25mV about the nominal 5.4V and 5.8V levels for Vcc and Vdd respectively, with a test resolution of 1mV.