

PP1 PCB Test Methods, Specifications And Limits

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1) Connectivity and Capacitance Test

- a) connection from the connector to the capacitance (no resistance measured)
- b) short or R up to $2\text{ M}\Omega$ between any two lines or ground
- c) capacitance value test, from 10 pF to approx. $20\text{ }\mu\text{F}$, resolution 10 pF , absolute accuracy $< 1\%$.

The test sequentially activates each line and checks all other lines for possible error. For details, see the block circuit diagram in Fig.1.

2) High-Voltage Test

- a) sustained 500 Vdc test for $\sim 30\text{ s}$ on the HV-Bias line (risetime 0.5 s)
- b) leakage current from HV-Bias to HV-return at 500 V , $Z_{\text{in}} = 1\text{ M}\Omega$, $V_{\text{in max}} = 10\text{ V}$, $I_{\text{lk max}} = 10\text{ }\mu\text{A}$, resolution 30 pA .
- c) leakage current from HV-Bias to Ground at 500 V , $I_{\text{lk max}} = 10\text{ }\mu\text{A}$, resolution 30 pA (Z_{in} is virtual ground, amplifier input offset voltage $< 100\text{ }\mu\text{V}$, amplifier input current $< 25\text{ pA}$).

Other lines are protected by design layout of the PCB and are not tested. For details, see the block circuit diagram in Fig.2.

3) Trace Resistance Test

- a) 4-point Kelvin resistance measurement from the connector to the LM-Tape solder pads ; each line is sequentially activated by 100 mA and the voltage drop is measured by a 2 V range, $100\text{ }\mu\text{V}$ resolution ADC, resulting in a $20\text{ }\Omega$ range and $1\text{ m}\Omega$ resolution, with absolute accuracy $< 0.5\%$.

For details, see the block circuit diagram in Fig.3.

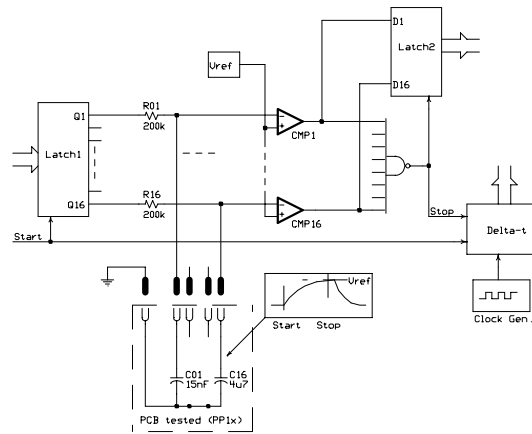


Fig.1 : Capacitance test

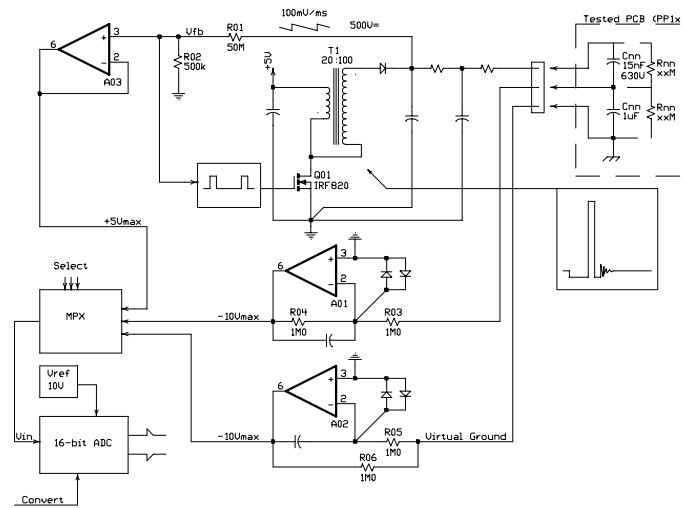


Fig.2 : High-Voltage test

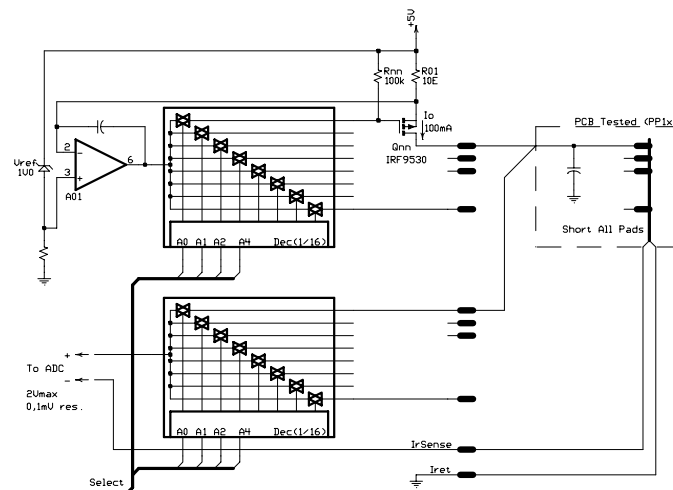


Fig.3 : Line Resistance test