Front-end read-out of the Alice TOF

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- Alice TOF: required resolution < 100 ps
- How does it look like
- Is it interesting for TOP?

TOF detector

- multigap resistive plate chambers (MRPC)
- front end electronics provides a timing signal and a time-over-threshold signal (for time vs amplitude correction)
- custom-made multihit TDC system, 25 ps resolution

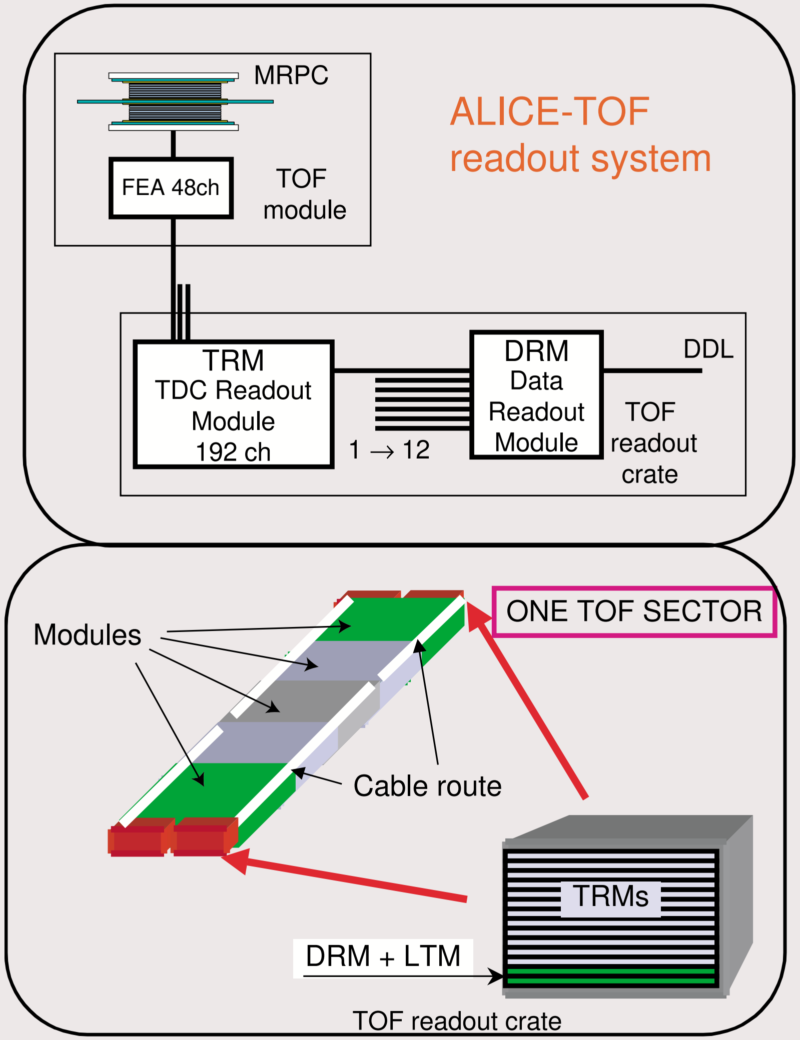

Figure 4.1: ALICE TOF readout general scheme.

Front end circuit

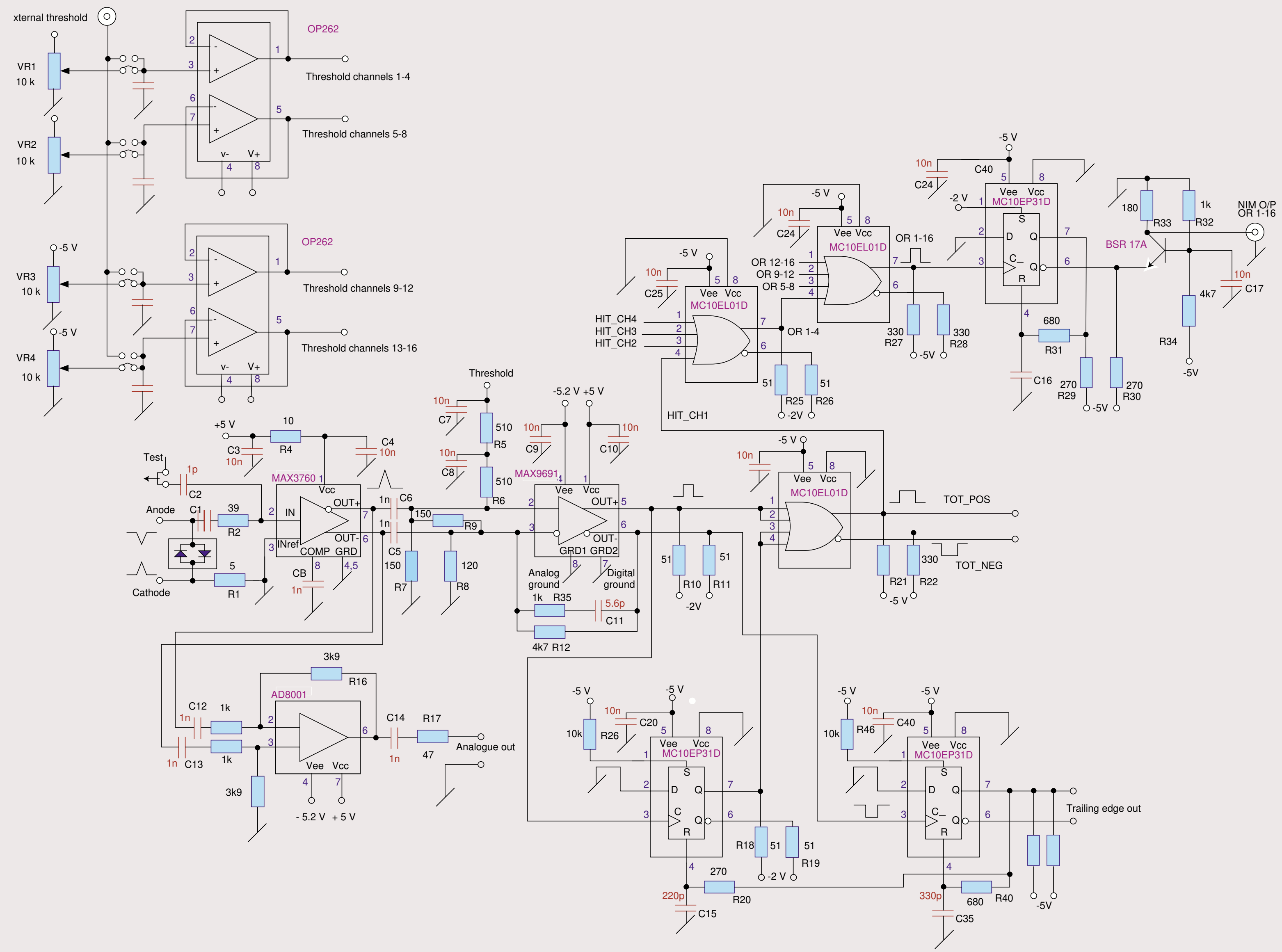

Figure 4.2: Circuit diagram of 16-channel Front-End Analogue card used for the tests.

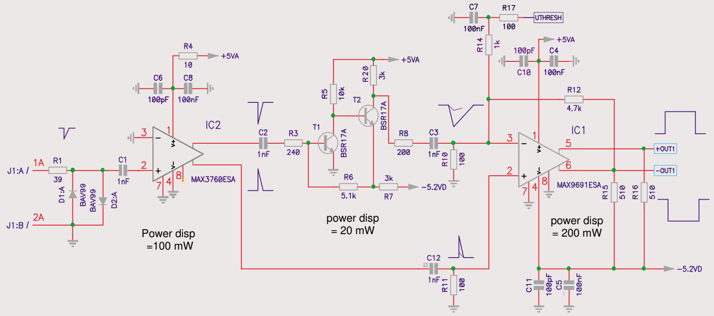

Figure 4.3: Front-end analogue card circuit diagram (one channel).

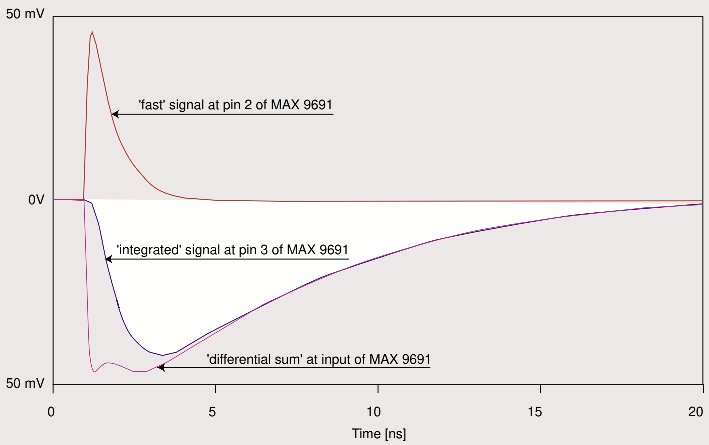

Figure 4.4: Simulated performance of integration circuit.

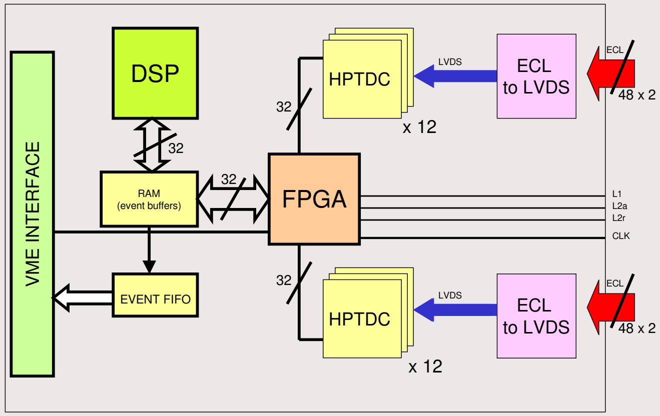

Figure 4.6: Block diagram of one TRM module with 192 channels.

group of two channels has a 256 words deep buffer attached to it. A trigger matching is then performed between a trigger time tag and the time measurements themselves at a given offset, within a user programmable time window. Hits matching a trigger are passed to a common readout FIFO (again 256 words deep) shared by each four-channel group.

4.3.2 The TRM

A block diagram of the TRM is shown in Fig. 4.6. This module receives 192 ECL shaped signals from the FEAs: these signals internally converted to LVDS standard, are sent to the 24 HPTDCs. An FPGA will then perform the readout of the HPTDCs. To ensure high bandwidth the FPGA will act as an external readout controller of two separate chains consisting of 12 HPTDC slaves (in token-base parallel-readout configuration). The use of an Altera APEX family FPGA is foreseen. A Digital Signal Processor (DSP) will control various setup operations (including R-C delay chain calibration) and data packaging. The use of a Analog Devices Shark family DSP is foreseen. Memory (RAM and SRAM) is provided for event buffering and program hosting.

Program loading and general control of the TRM will be managed through a VME interface. Initialisation and setup of the HPTDC chips will be normally performed through the DSP.

At reception of a L1 signal from the ALICE Central Trigger Processor (CTP) the HPTDCs will look for hits with a time offset of $\approx 6.2\,\mu$s (the exact value will be determined by the L1 decision time, still to be specified [3]) and a programmable time window (of the order of 100 ns), moving them to the internal readout FIFO. This operation does not cause dead time to the acquisition of data by the HPTDC.

Immediately after the L1 signal, the FPGA looks at the HPTDC readout FIFO and performs the readout of one event (the HPTDC provides event separation between hits with event header and trailer for each received trigger). The FPGA will then send the data to the DSP for further processing (data

Status

- Contact with the responsible group members established
- If interested, we could get gerber files of the front-end circuit