CDC status

NANAE TANIGUCHI (KEK)

7TH B2GM
NOVEMBER 19, 2010

CDC session

7th B2GM, November 17, 2010

16:45->*18:45* 05 CDC (Rm 425)

16:45	Test chamber for 3D trigger (15') (Slides)	JaeBak Kim
17:00	3D trigger (15') (Slides)	Eunil Won
17:15	TRG in CDC (15') (Slides)	Yoshihito Iwasaki
17:30	Status and scedule of electronics (15') (Slides)	Tomohisa Uchida
17:45	Charge division and test of 48ch board (30') (Slides	Nanae Taniguchi
18:15	Structure and schedule (15') (Slides)	Shoji Uno

members of NPC II group joined

CDC session

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Program (CDC session)

1st B2GM, December 11, 2008

Link to Indico agenda

Time	Title	Speaker	Slides
Thursday 11 December 2008			
16:00	R&D for CDC upgrade	N. Taniguchi	[pdf]

Activity of CDC group (including software and 3D trigger group) is increasing

Fabrication of the CDC test chamber

- From July. 9 to August. 24

7th B2GM

Korea Univ.

Presented by Jaebak Kim

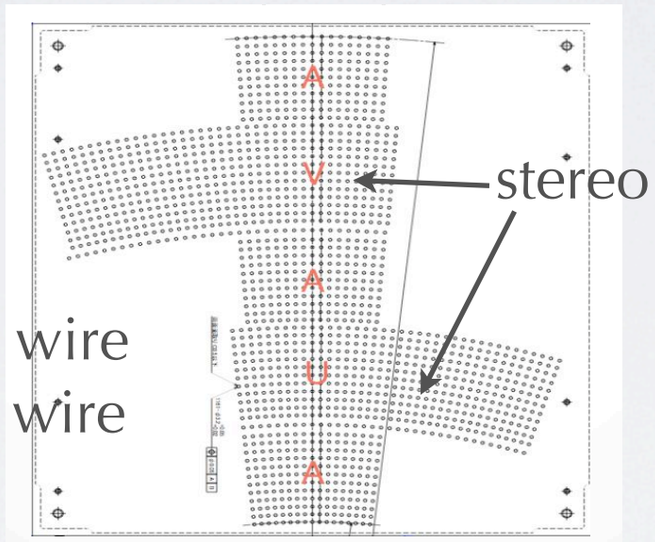
Jaebak Kim (Korea Univ.)

TEST CHAMBER FABRICATION

- For 3D trigger (L1 TRG) study, configuration is same as Belle II CDC, corresponding to outer 5 super-layers
- Jaebak Kim, Kyuntae Kim, Hyunki Moon, Chulwon Lee, Eunil Won (Korea Univ.), Min-Zu wang, and Juo Yu Fan (NTU)

In this summer

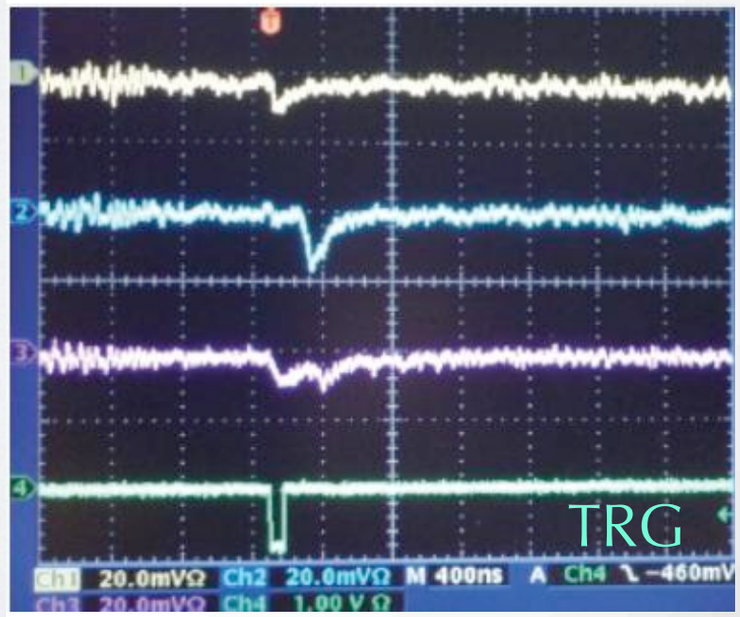
2240x545x575(mm^3)



1200 field wire
400 sense wire

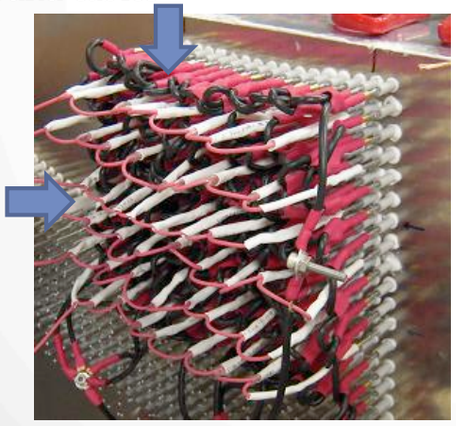
- ✓ Wire stringing during 20 days
- ✓ measurement of wire tension
- ✓ gas leak check
- ✓ HV test

Analog signal

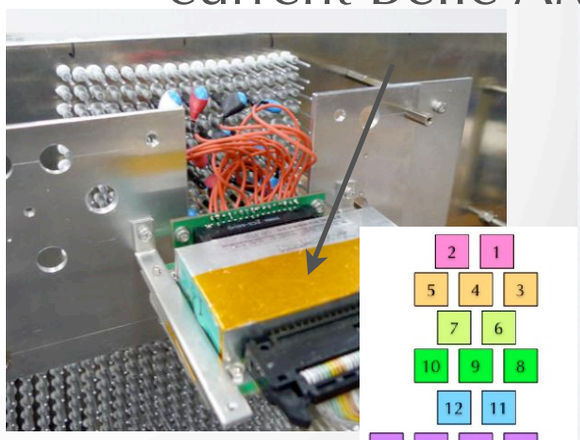


Ground cables

HV cables

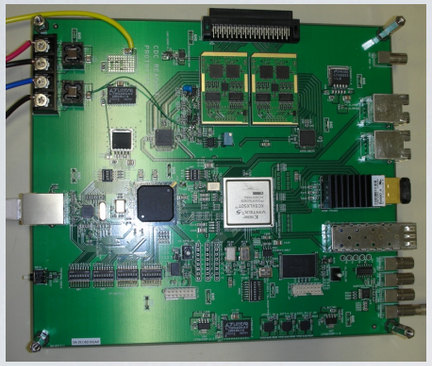


current Belle AMP



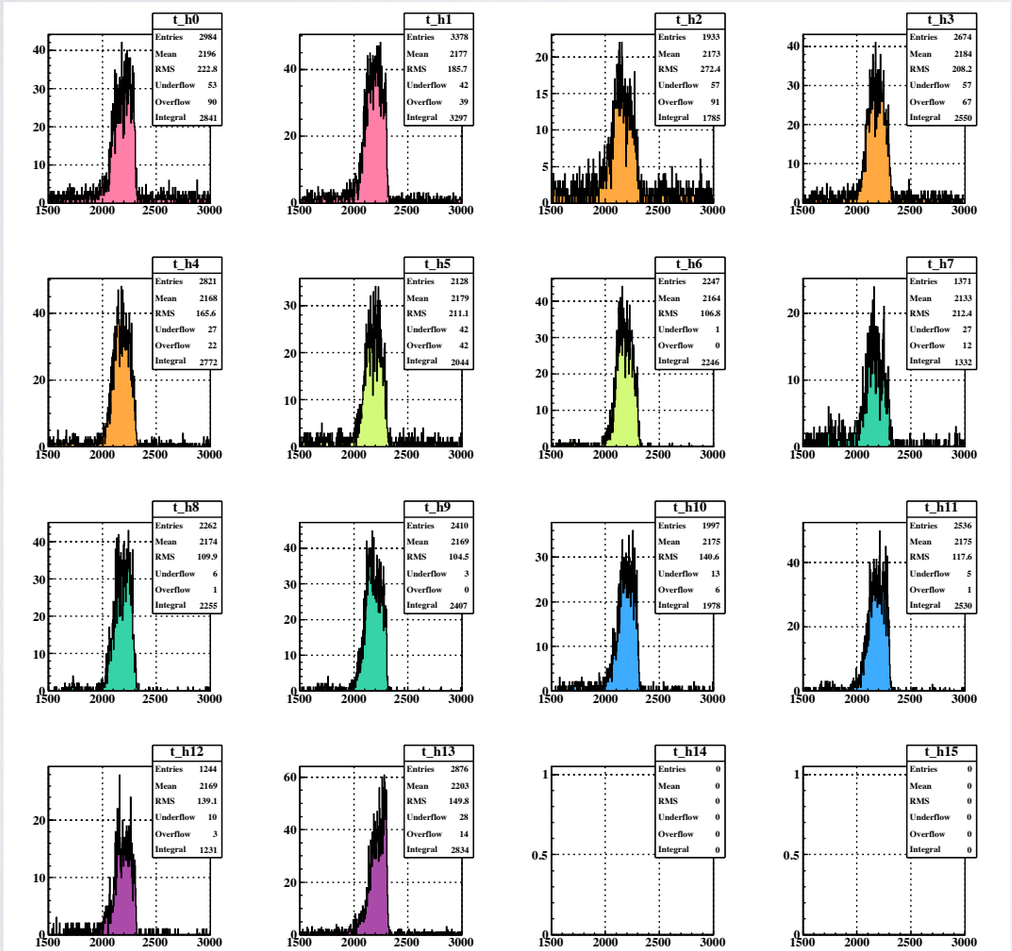
Jaebak Kim (Korea Univ.)

COSMIC RAY DATA

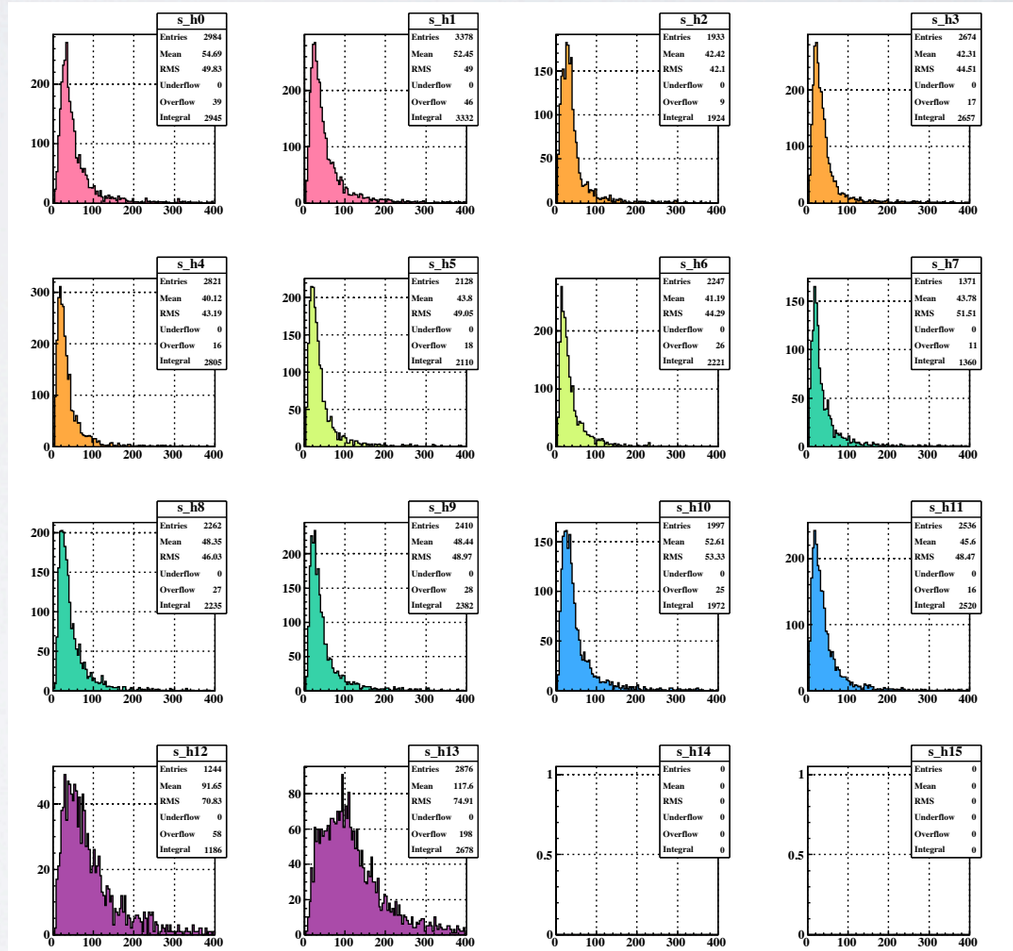


data is collected from 14ch with CDC readout board (2009 ver.)
cosmic ray data

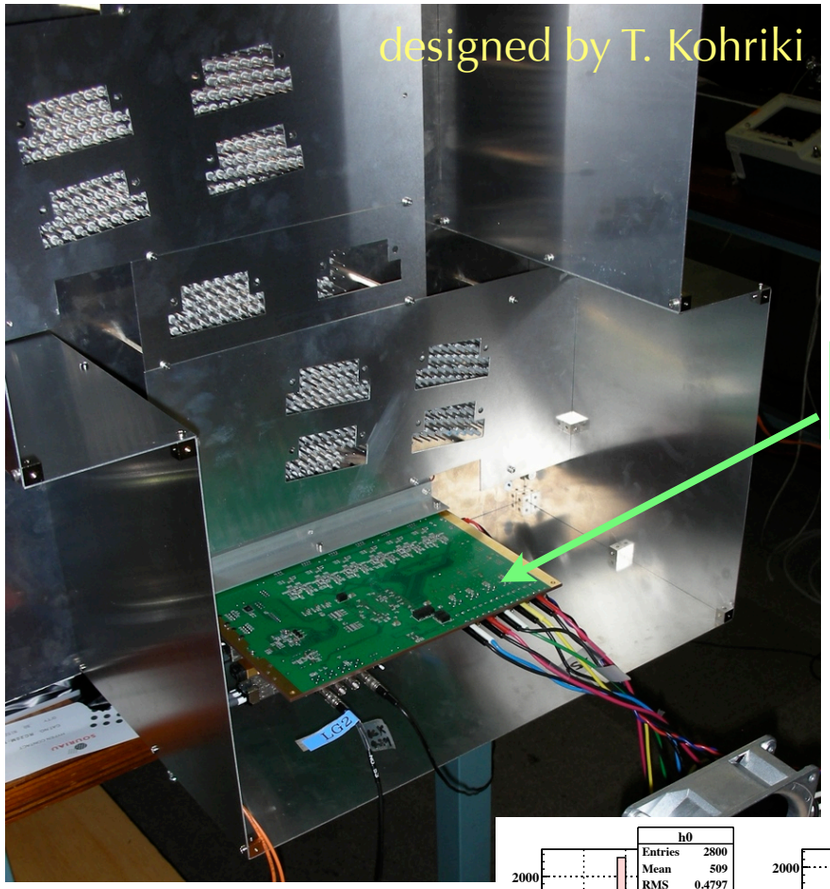
TDC



FADC sum (energy loss)



data taking done successfully

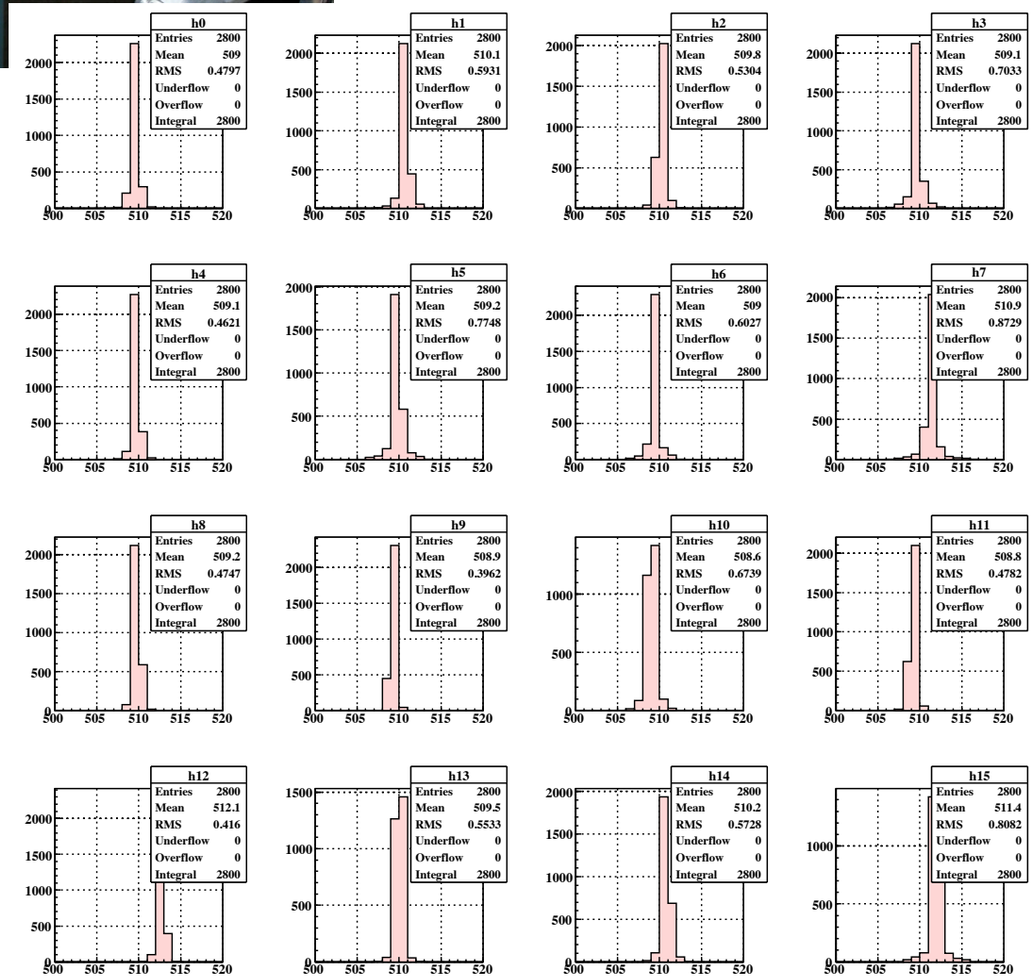


November 12, 2010

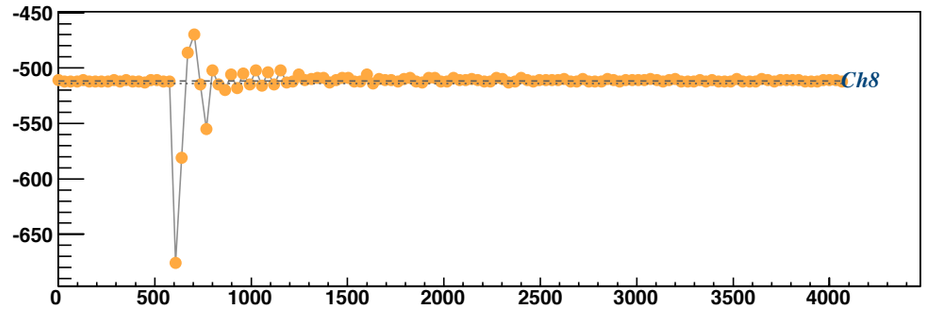
new 48ch board

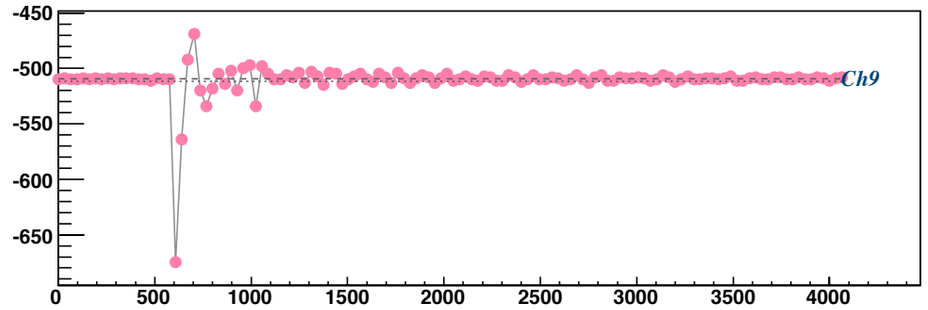
good test for assembling of real Belle II CDC.

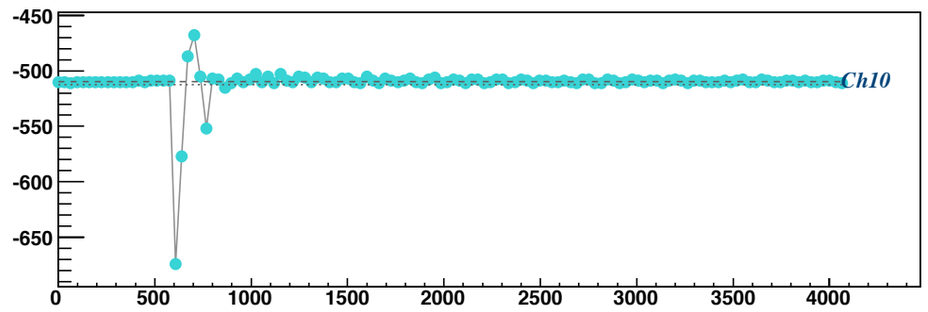
pedestal (ch0-15)

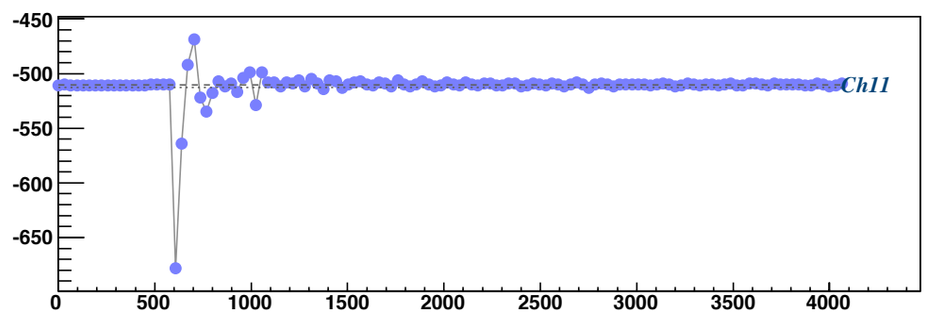


waveform sampling of test pulse









Eunil Won
(Korea Univ.)

Status of the 3D fitter

- Jaebak Kim (KU) started working on the fitter
  - understanding of the present code (by B.R.Ko) done
  - started working on transforming the code into integer space
- Kyungtae Kim (KU) started working on tsim
  - received basf2 tsim from Y. Iwasaki-san recently (timing info included)
  - able to make tsim event display
-

Eunil Won
(Korea Univ.)

Things to Do

- 3D fitter
  - New basf2 CDC geometry has to be in
  - Move C++ program into integer space
  - Use timing information to reach z_0 resolution ~ O(5) cm
  - Write VHDL (**V**ery High Speed Integrated Circuits **H**ardware **D**escription **L**anguage)
  - Write identical C++ into tsim cdc
  - results will be reported in Next B2GM
- chamber fabrication
  - finish cabling in this winter
  - test with new 48ch readout board

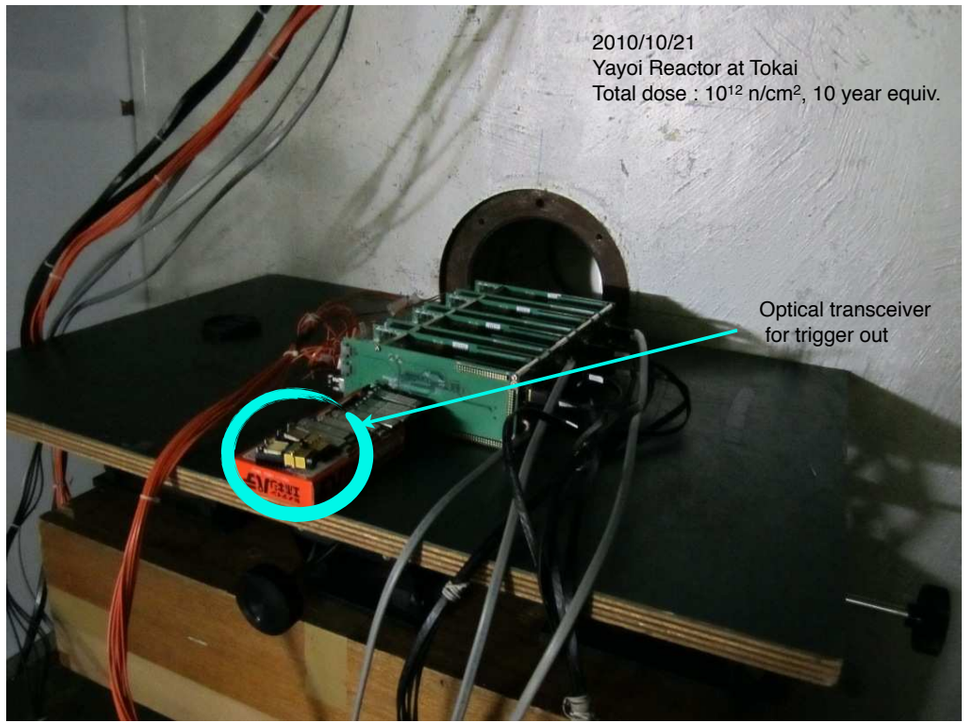
TRG in CDC

Y. Iwasaki
@
B2GM 2010/11/17

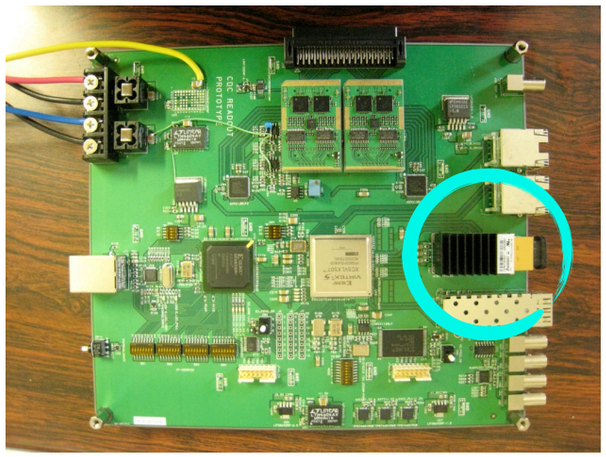
Report about neutron irradiation

Neutron Irradiation

M. Nakao
T. Higuchi
I. Nakamura



Avago HFBR-7934WZ



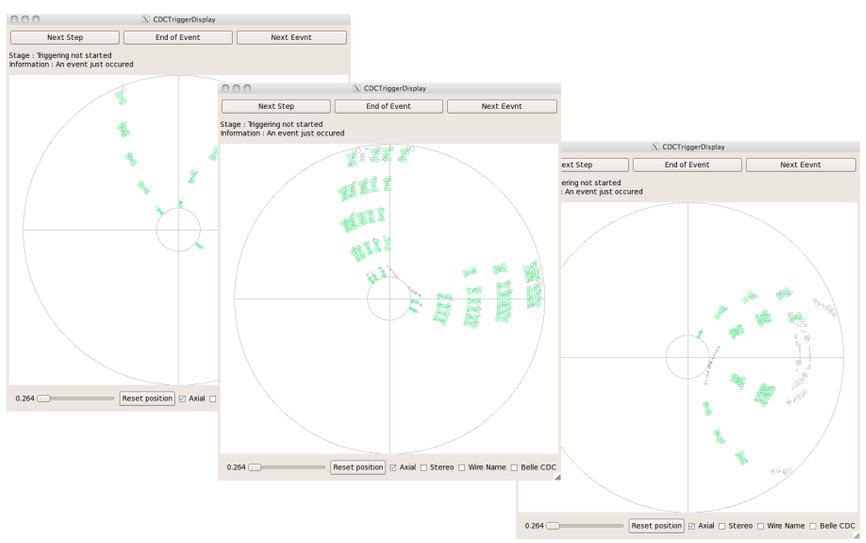
- Optical Transceiver
  - right emission recovered by power cycling
  - link with module become unstable, not recovered by power cycling
  - more investigation after the modules back

Y. Iwasaki (KEK)

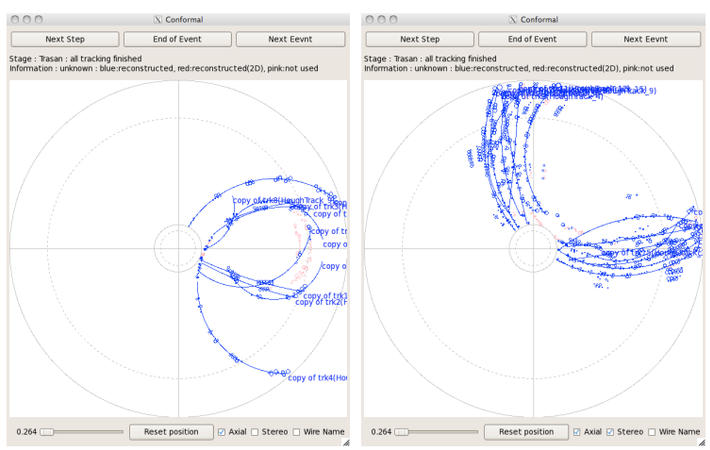
CDC Trigger Simulation

- **Basic components were installed under basf2**
- **Directory structure in the library is under discussion**
  - **Library/cdc/...**
  - **Library/trigger/cdc/...**
- **Present version can simulate up to TSF**
- **Hardware module base simulation is necessary**
  - **Especially for 3D tracking developments**
  - **Input and output of each hardware module will be simulated**
  - **Simulated input can be sent to real hardware**

CDC Trigger Event Display



Trasan Example

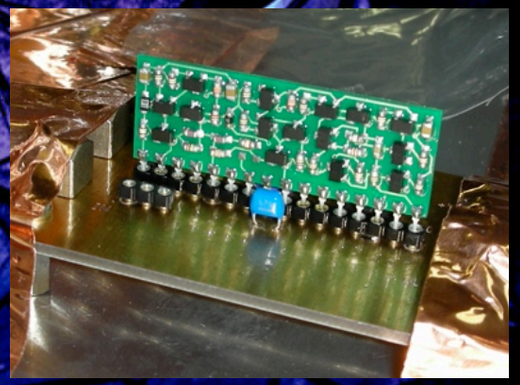


charge division

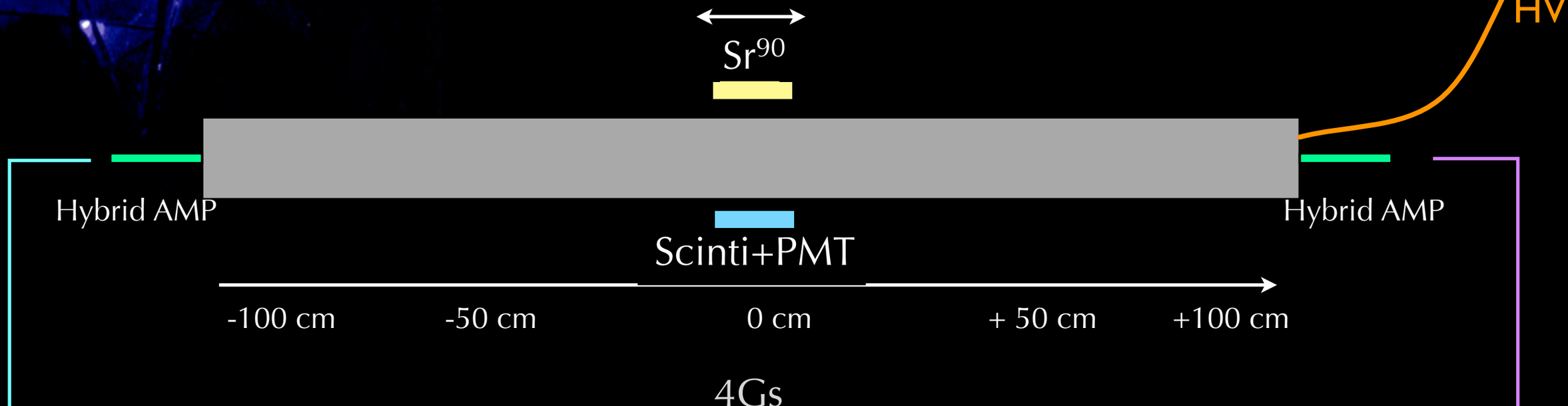
Nanae Taniguchi (KEK)

Novemver 17, 2010
7th B2GM

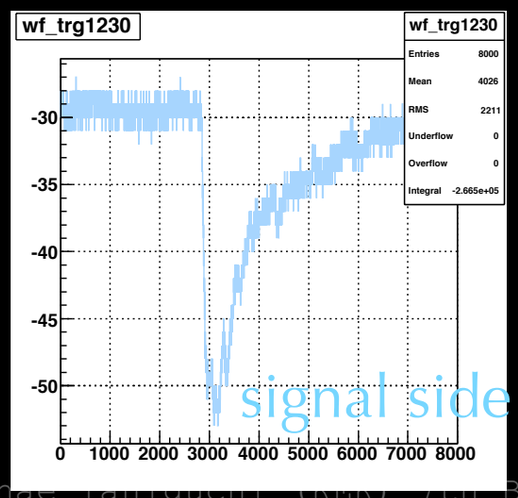
setup

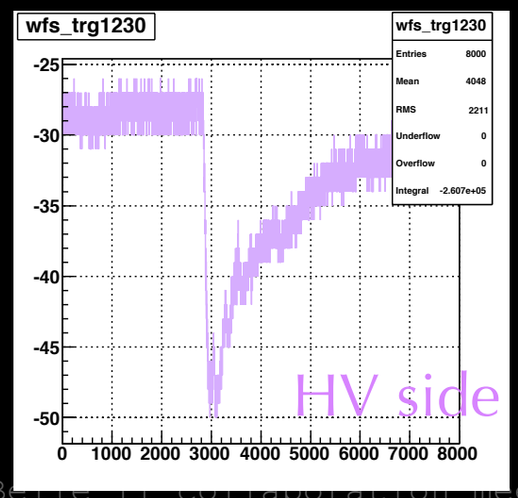


- lower input impedance hybrid AMP is developed
- study for performance with minimum modification
- wire material and diameter can not be changed
  because of multiple scattering and radiation damage



4Gs

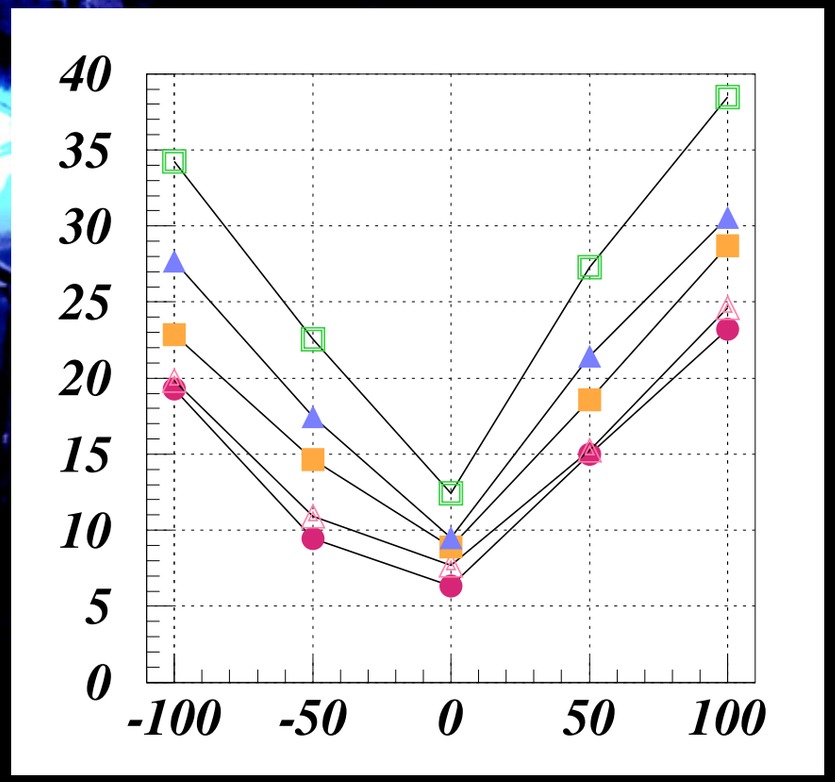


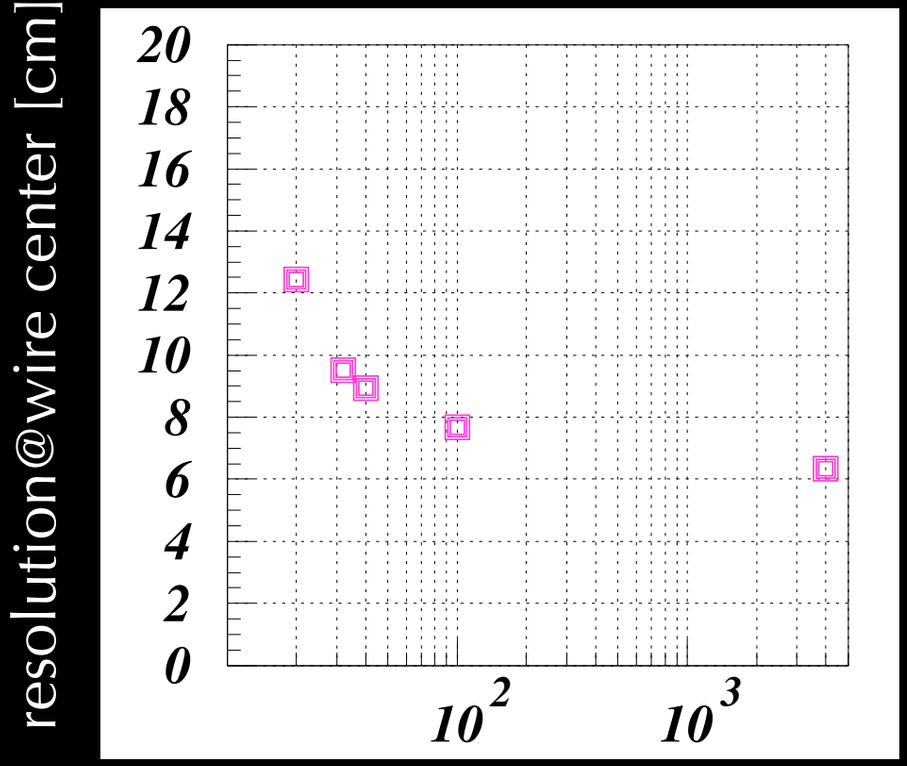


Results

HV=2.5kV

sampling rate
20MHz
32MHz
40MHz
100MHz
4GHz





- 6.3cm (4GHz sampling) is the best
- ~9cm resolution at 32MHz sampling (for CDC board)
  - ~13cm resolution with 16ch readout board (previous measurements)

conclusion of charge division

- The final results of charge division
  - study with the AMP of lower input impedance
  - 9cm resolution @~1.3 improvement (32MHz sampling)
  - requirement is ~ 4cm
- There is little possibility to do charge division
  - we will decide after confirmation of results of 3D TRG study in the end

Readout Electronics

17 Nov. 2010

Tomohisa Uchida, E-sys, IPNS, KEK

Current Status

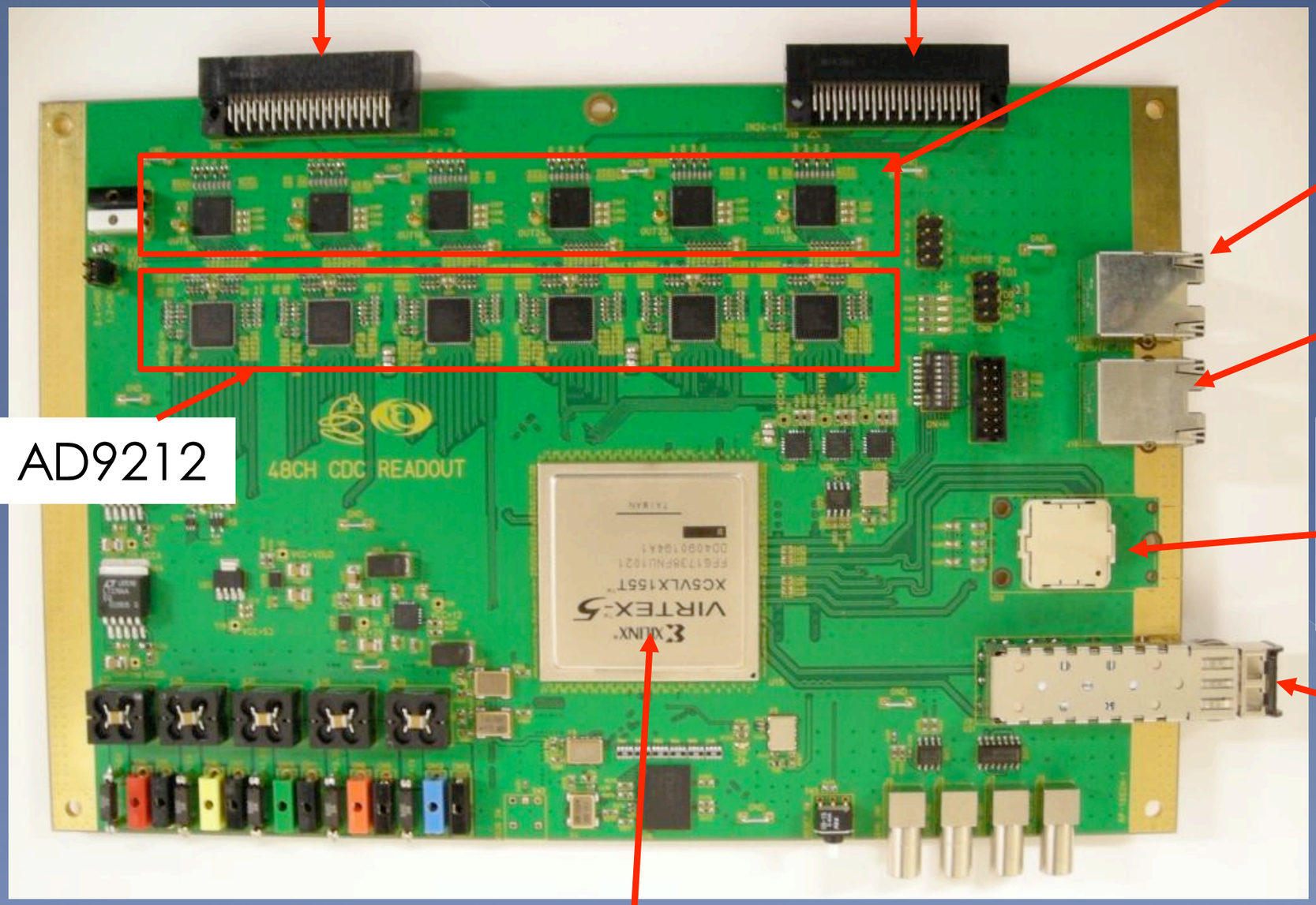
- A new board has been produced
  - Received in the last month
- Revising a ASIC(ver.2011)
  - To fix problems
  - Submit in Jan. 2011
- FPGA firmware is under development
  - test with 48ch board (ver.2010)

New readout board

48 inputs

Connector to the detector

New ASICs



Timing I/F(RJ45)

JTAG I/F(RJ45)

ADC AD9212

High speed data link
(Rocket IO)
for a trigger logic

SFP
(Ethernet port)

Signal processor (Xilinx Virtex5 FPGA)

Size = 230mm x 150mm

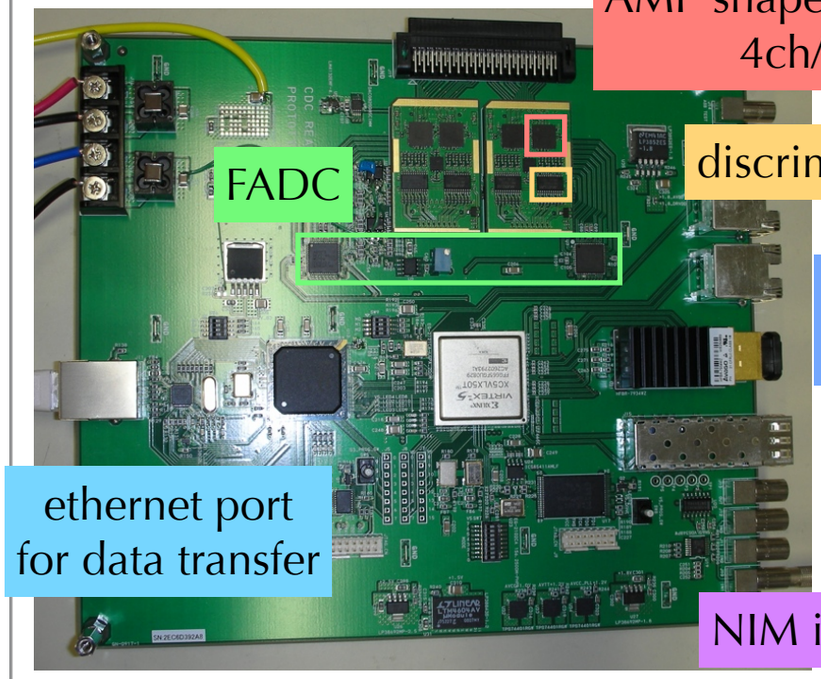
16ch readout board

AMP shaper ASIC chip
4ch/chip

discriminator

FADC

Rocket I/O
for TRG



ethernet port
for data transfer

NIM input for TRG

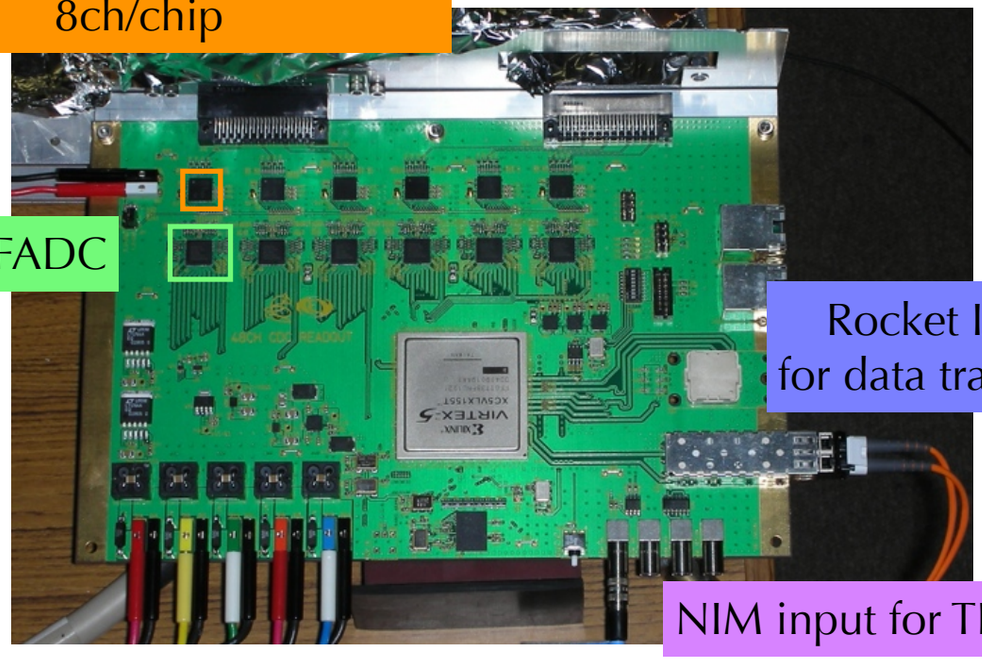
230mm x 150mm

48ch readout board

AMP shaper discriminator chip
8ch/chip

FADC

Rocket I/O
for data transfer



NIM input for TRG

230mm x 150mm

Problems found

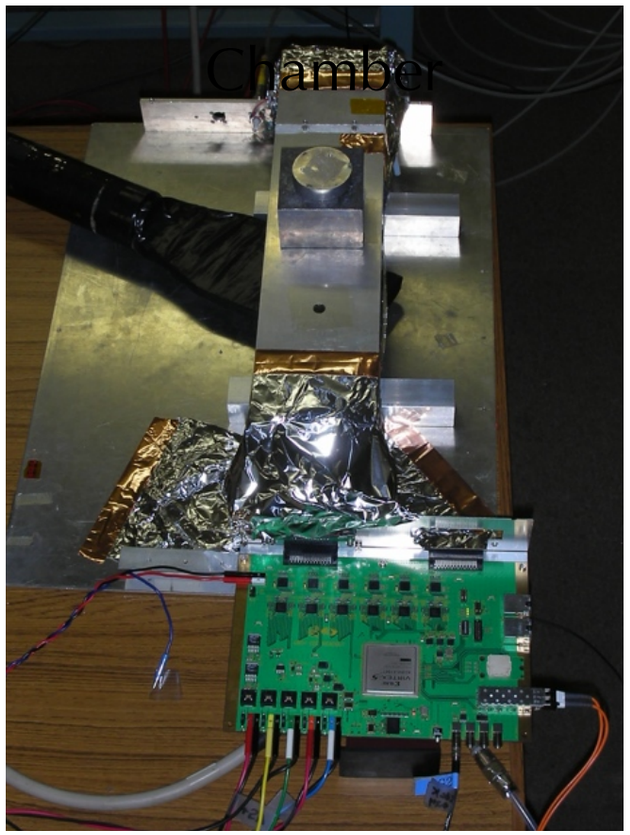
- ASIC
  - protection circuits for Electrostatic Discharge
    - Miss-implementation of diodes
    - Employ a new checking tools
  - ADC I/F voltage
    - Too high
    - Add a temporary circuit to adjust
  - Layout in chip
    - sensitive against noise
- PCB (Print Circuit Board)
  - FPGA signal connections

Test of 48 ch board

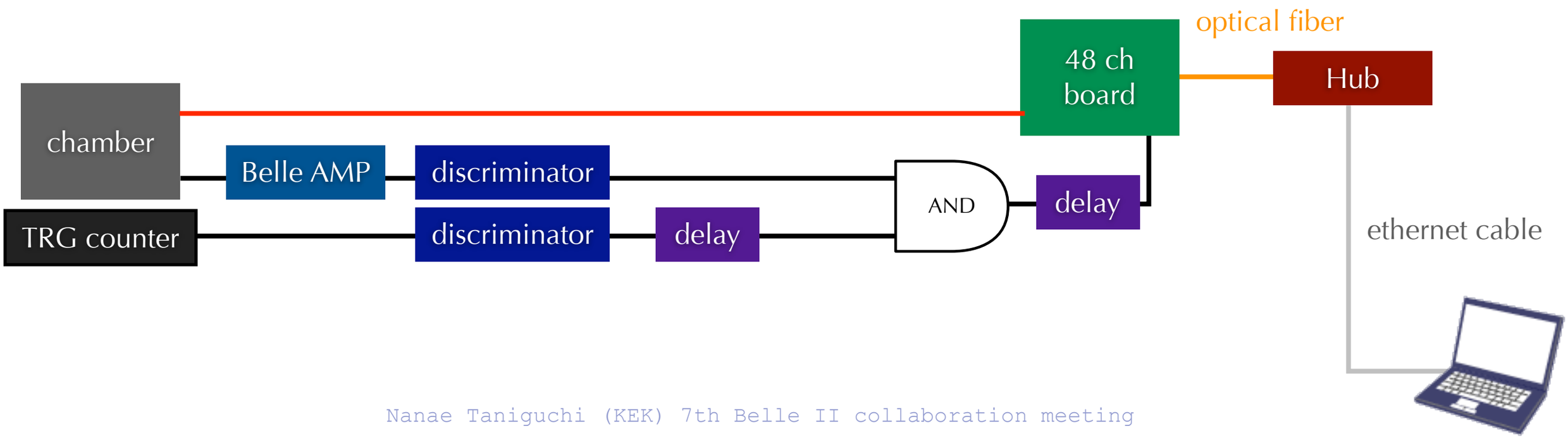
Nanae Taniguchi (KEK)

November 17, 2010
7th B2GM
CDC

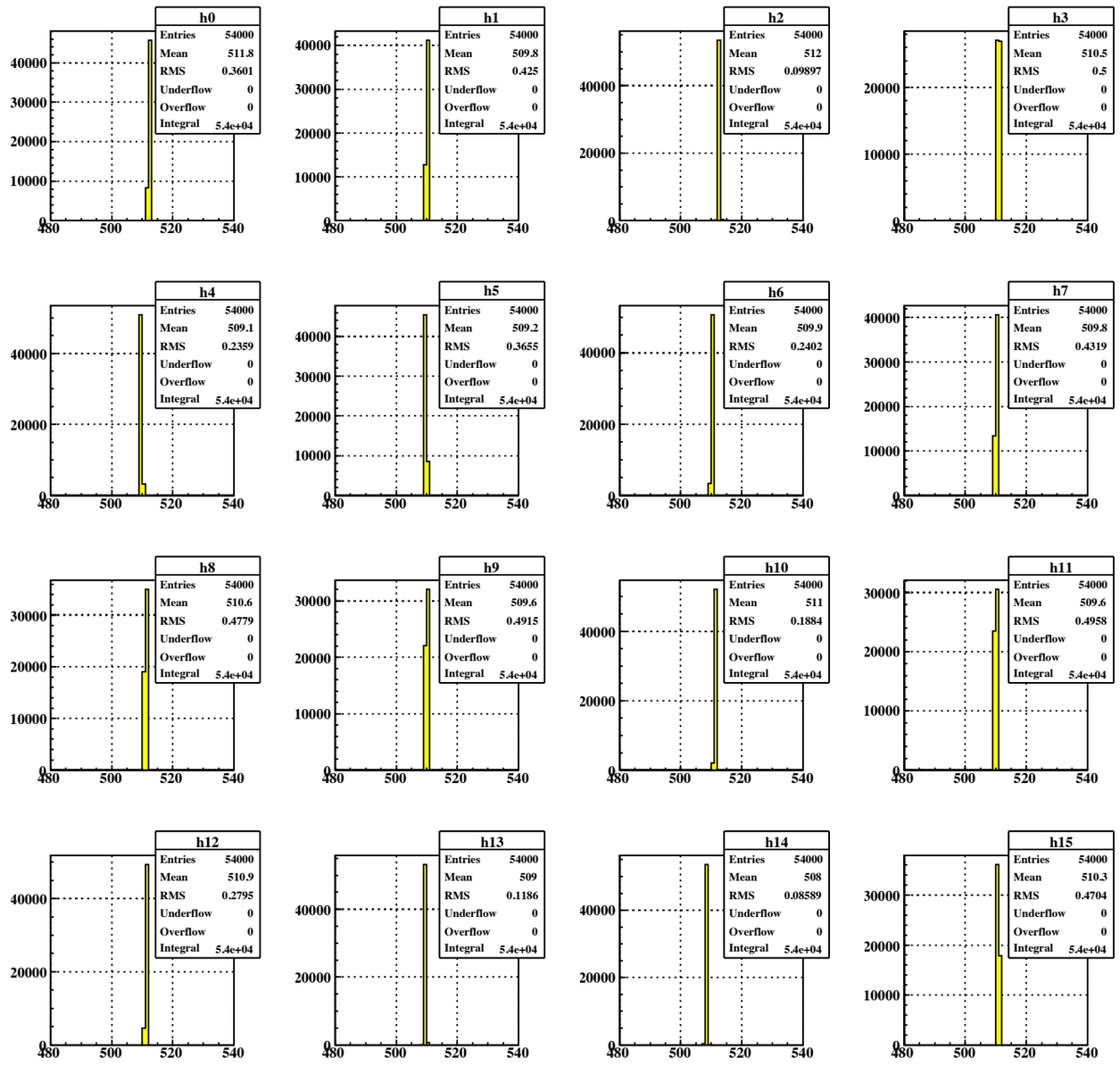
set up



- same way as previous test
  - 5-layer test chamber, 14ch can be used
  - same gas (He(50):C_2H_6(50))
  - same FPGA program (for ch16)
  - same analysis



pedestal

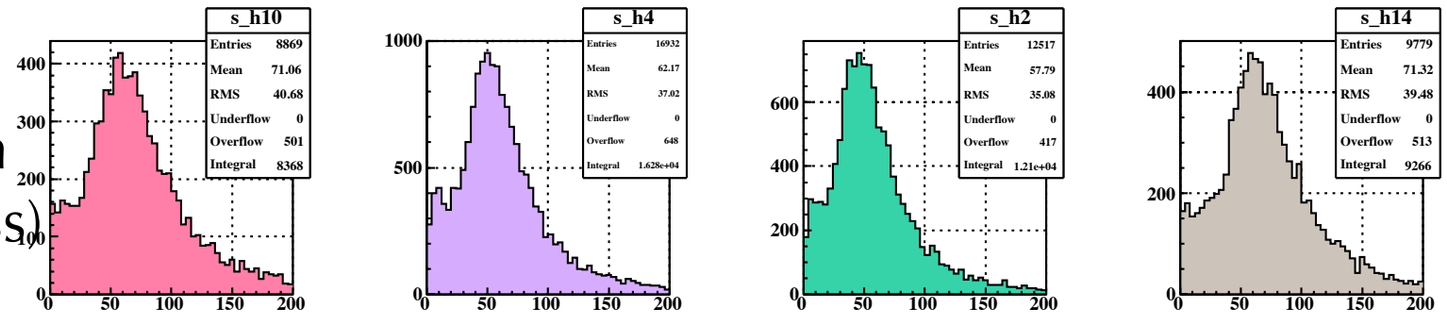


- same mean value and RMS is better than previous measurement
- there was common noise due to switching regulator in previous board
- No common noise is found

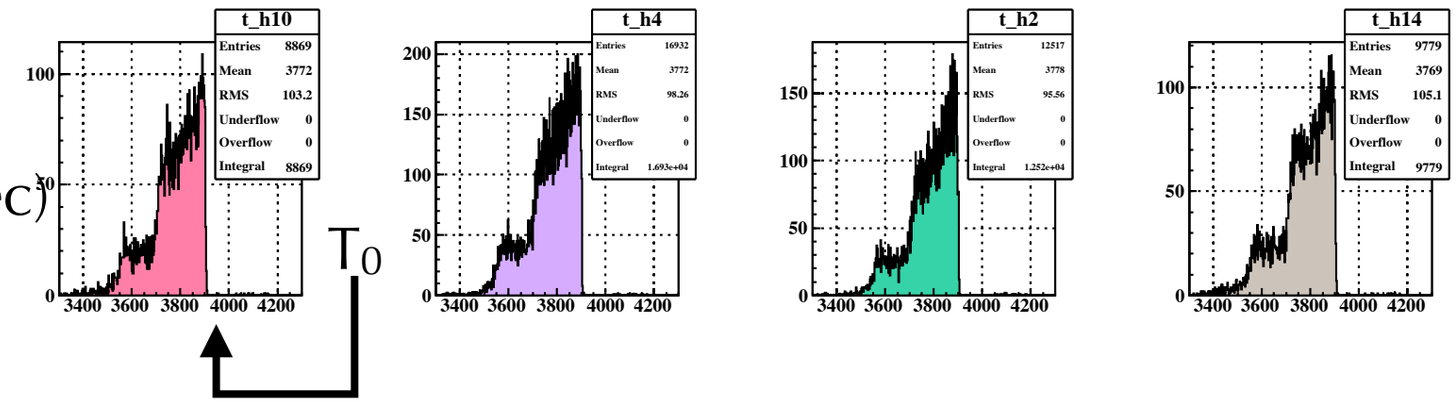
cosmic ray data

HV=2.3kV
He:C_2H_6
cosmic

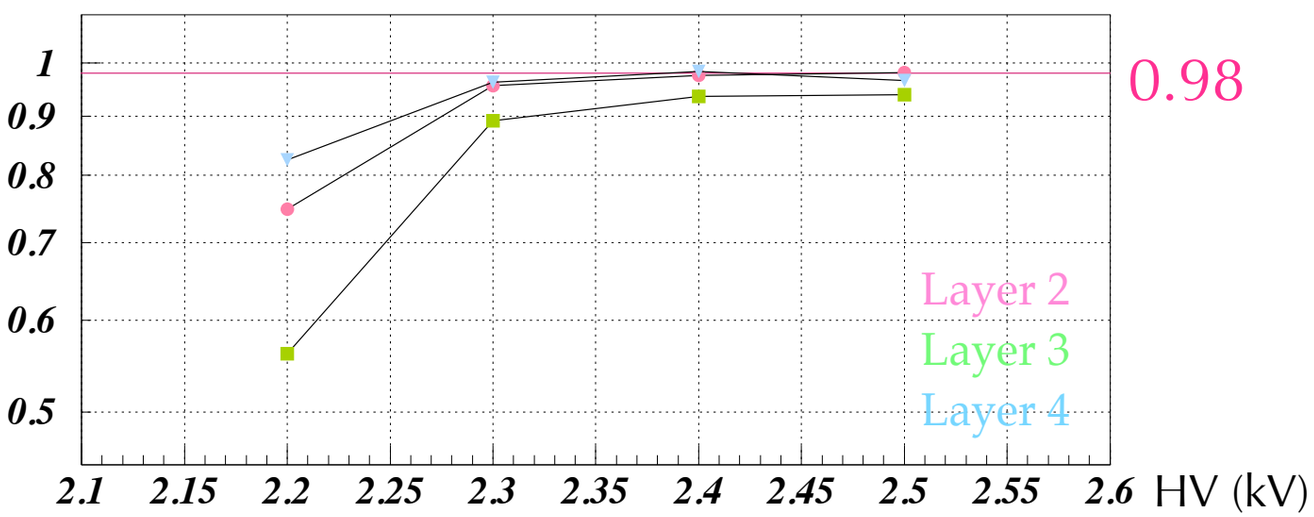
ADC sum
(energy loss)

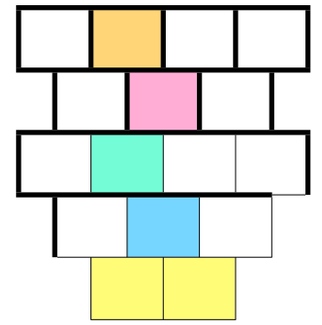


TDC
Haxis (nsec)

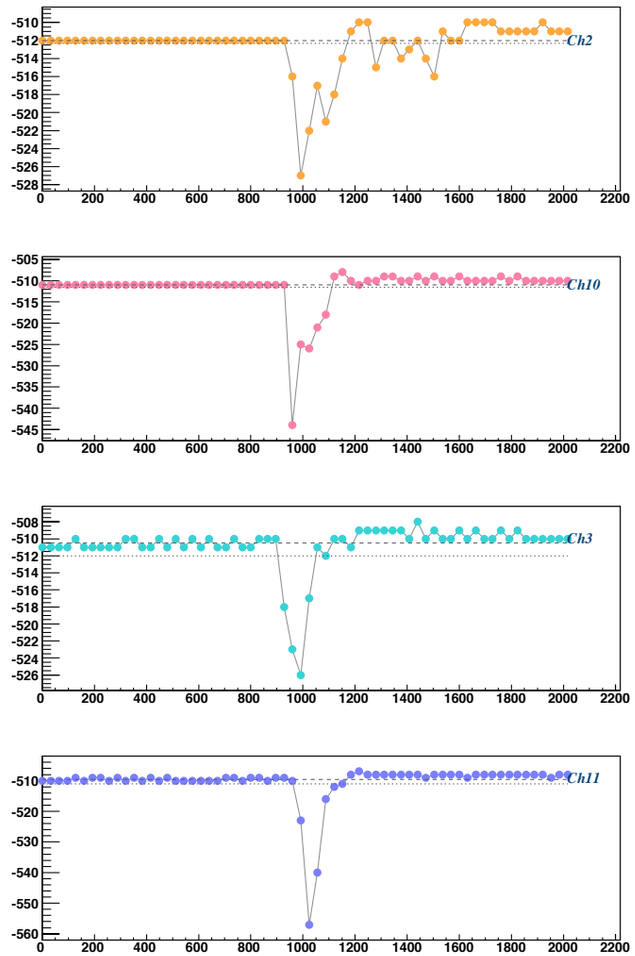


efficiency





waveform sampling



status and problem

	STATUS
pedestal	better
common noise	OK
TDC distribution	looks OK
energy loss distribution	looks OK
signal shape (after pulse)	OK
cross talk	slightly large
efficiency	lower

- lower gain
  - gain loss due to temporary circuit for adjustment
- lower efficiency
  - high threshold against low gain
  - not able to decrease threshold because of unstable digital out
- larger cross talk
  - sensitive against noise due to chip layout

summary of readout board

- KEK electronics group managed to operate
  - check, test, tune and adjust .., hard work !
- Test with 5-layer test chamber
  - Generally speaking, 48ch board works
    - lower gain, lower efficiency and unstable operation voltage should be solved in next version
    - NTU people join the test and help us
- some problems were found, but we understand the sources of the troubles
- more detail study under progress

schedule for readout board

Dec
- Design and layout for new ASIC
- development of FPGA for 48ch

Jan
- Submit production

Mar
- ASIC bare chip delivered

Apr
- test the ASIC chip

May
- Design a readout board (layout of PCB)

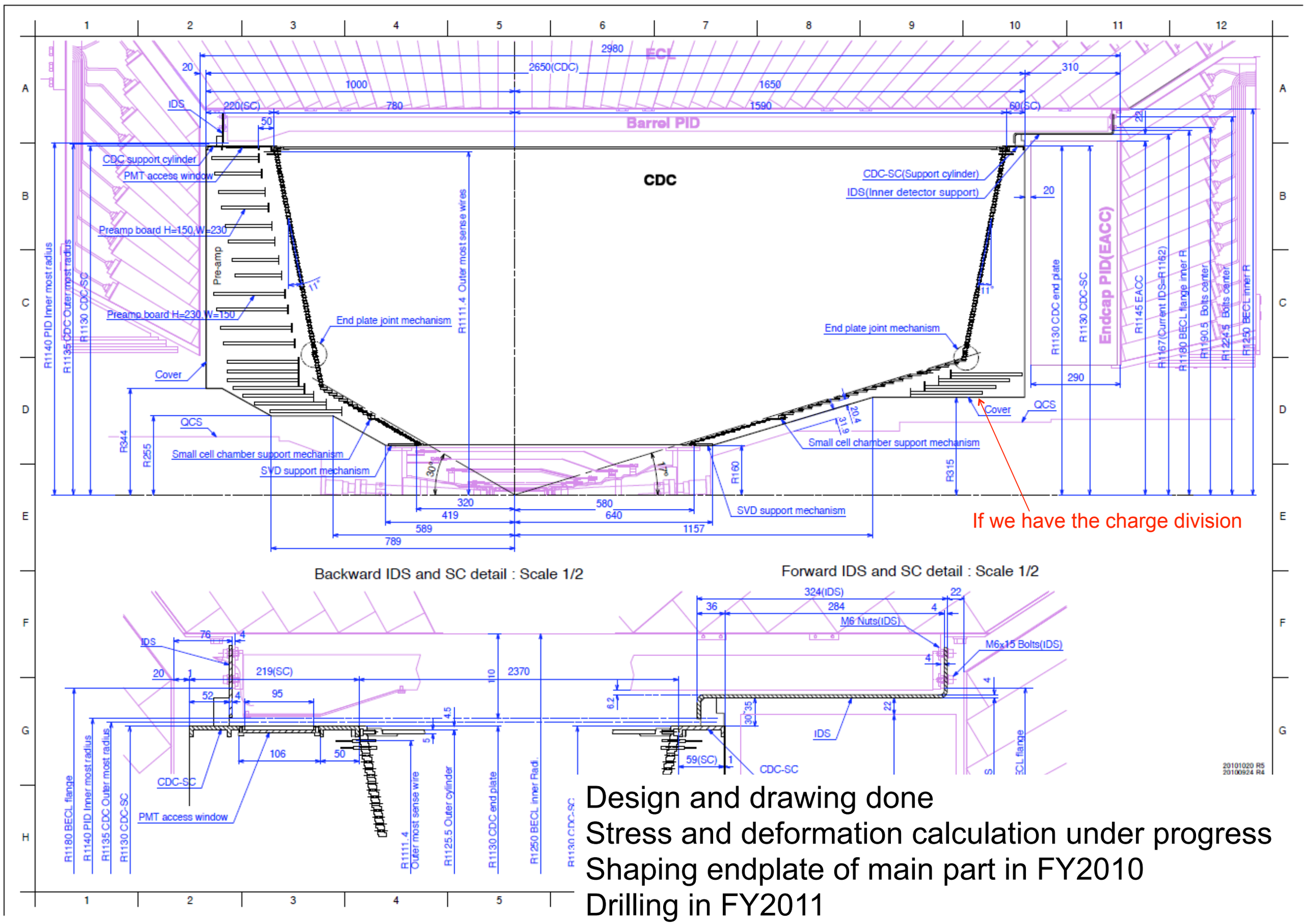
Aug
- Debug and test for readout board (ver.2011)

Structure and Schedule

Shoji Uno

KEK

2010.11.17



Design and drawing done
Stress and deformation calculation under progress
Shaping endplate of main part in FY2010
Drilling in FY2011

CDC Schedule

Items	JFY	2010				2011				2012				2013				2014			
		I	II	III	IV	I	II	III	IV	I	II	III	IV	I	II	III	IV	I	II	III	IV
Fixing outer radious	2010/06/01																				
Wire configuration design	2010/6/1-2010/6/30																				
Endplate design	2010/6/1-2010/11/30																				
Bidding of structure	2010/12/20																				
Endplate machining	2011/1/1-2011/3/31																				
Drilling	2011/6/1-2011/11/30																				
Assembling of Endplates	2011/12/1-2011/12/31																				
Wire stringing	2012/1/1-2013/3/31																				
Making small cell chamber	2012/8/1-2013/2/28																				
Insertion of small cell chamber	2013/4/1-2013/4/10																				
Tension measurement	2013/4/11-2013/4/30																				
Gas leak test	2013/5/1-2013/8/31																				
HV cabling	2013/9/1-2013/9/10																				
HV test	2013/9/11-2013/10/31																				
Signal cabling	2013/11/1-2013/11/30																				
Readout board R&D	2009/04/01-2012/9/30																				
Readout board mass production	2012/10/1-2013/9/30																				
Preamp + Cooling water	2013/12/1-2014/2/28																				
Cosmic ray Test at clean room	2014/3/1-2014/5/31																				
Installation of CDC & Test	2014/6/1-2014/6/30																				
Cosmic ray test on 1.5Tesla	2014/10/1-																				

Most critical item

Making the small cell chamber

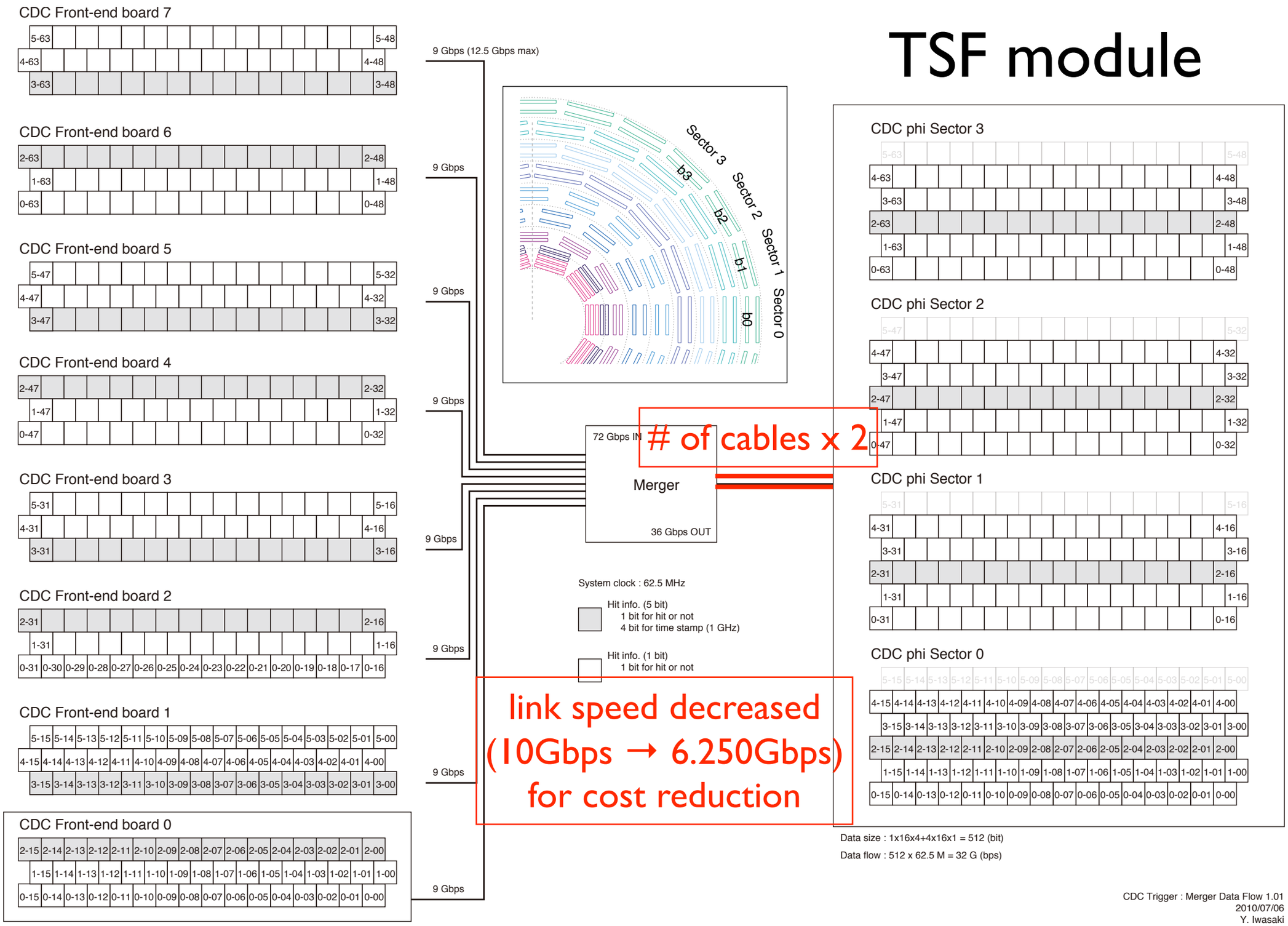
Especially , drilling 1.4mm-diameter holes of endplate

summary

- 3D trigger (L1 trigger)
  - test chamber (AUAVA) fabrication in progress
  - Fitter and TSIM in progress
- new readout board
  - new ASD ASIC
  - test with 5-layers test chamber
  - upgrade design and layout of ASD based on study
- FPGA
  - virtex-5 (3rd larger) for CDC readout board
  - vertex-6 for TRG
- structure
  - calculation of stress and deformation in progress
  - shaping endplate of main part will start in JFY2010

Y. Iwasaki (KEK)

Front-end and Merger



Power consumption

This is a preliminary result.

Full functions have not been implemented on the FPGA.

- 12W/module (250mW/ch)
  - +5V, 0.6A (ASIC)
  - -5V, 0.02A (NIM I/F)
  - +1V, 1.6A (Digital)
  - +1.8V, 1.9A (Digital)
  - +3.3V, 1A (Digital)

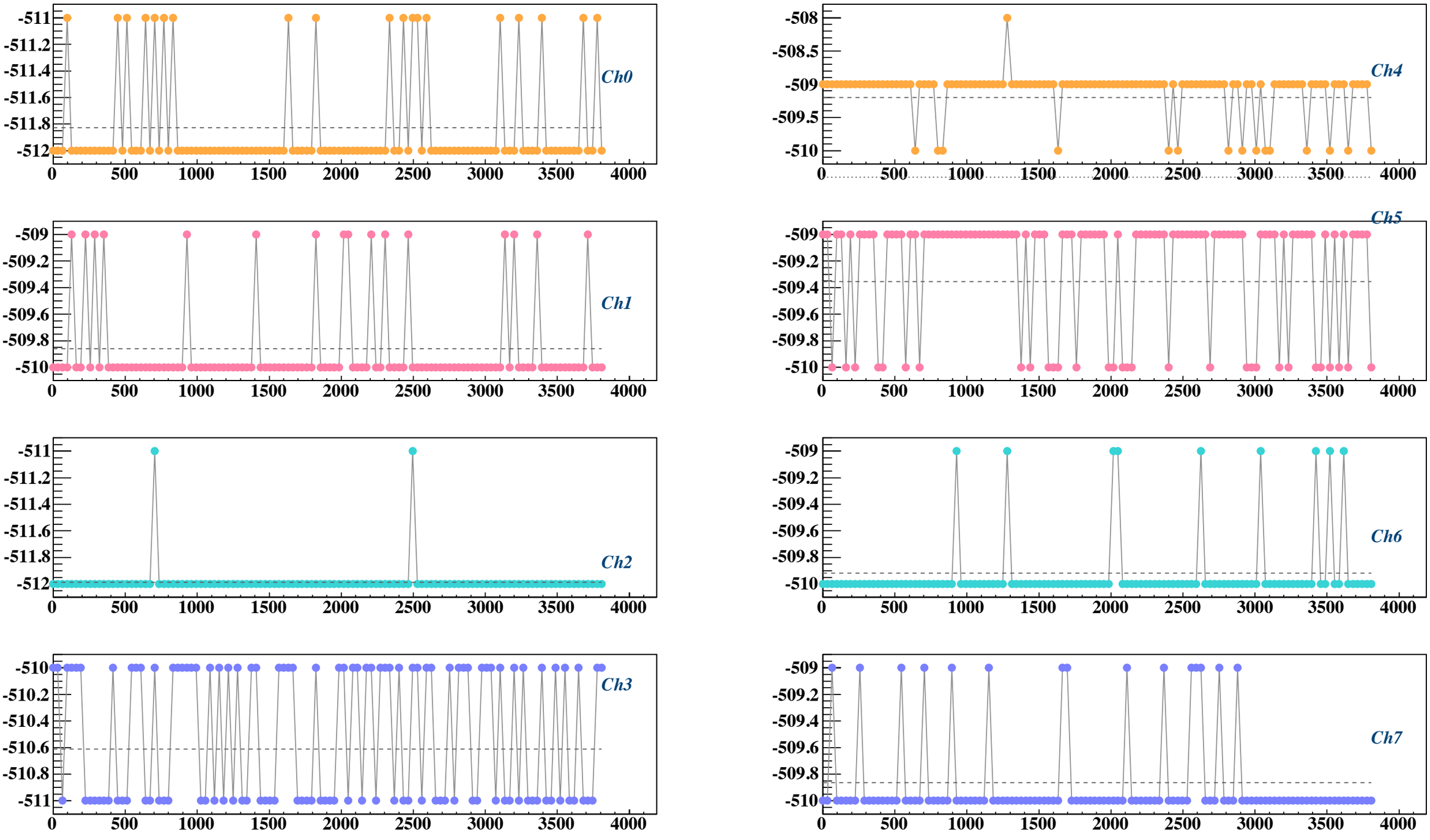
Taniguchi-san will talk the details of the test results.

pedestal

check common noise

Haxis [nsec]
Vaxis=ADCx(-1)

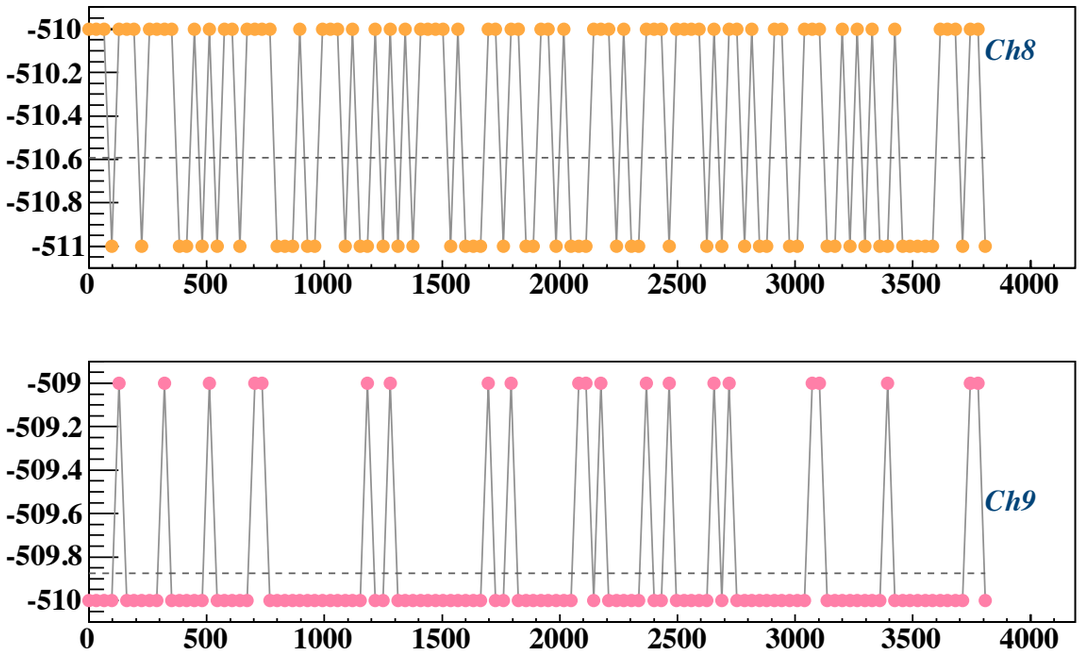
V_{th} = 130mV
w/ chamber
HV off

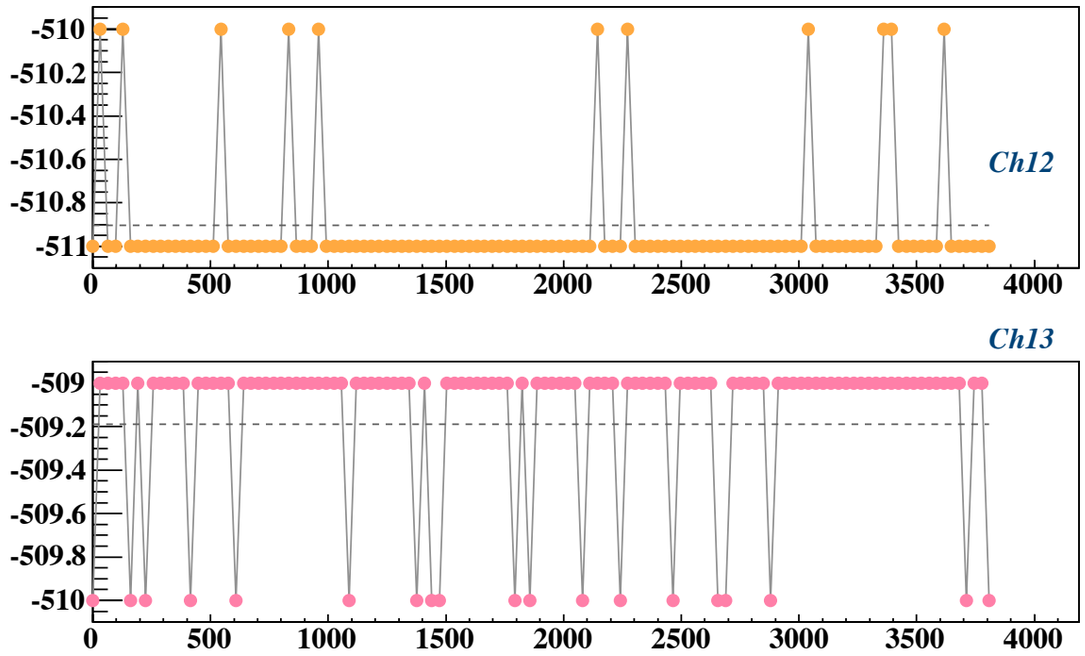


pedestal

check common noise

V_{th} = 130mV
w/ chamber
HV off

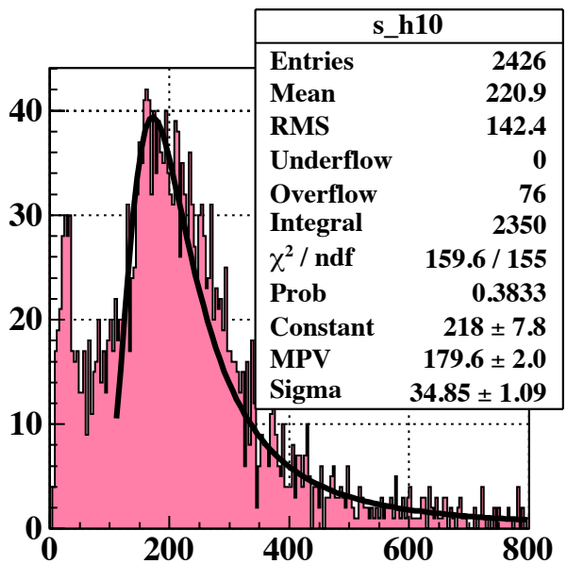


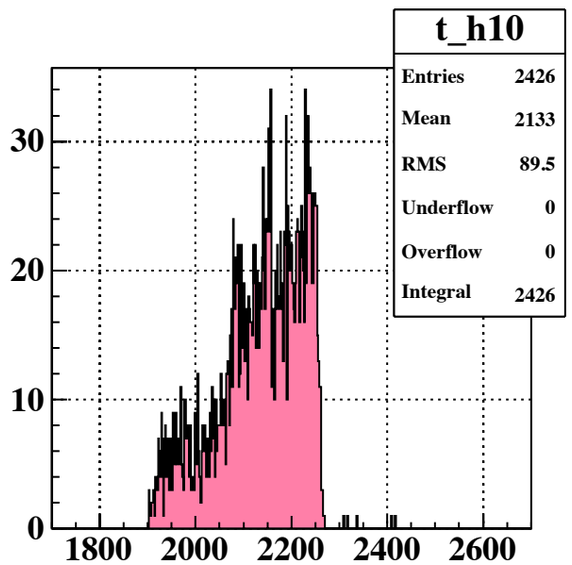


comparison

HV=2.3kV
He:C_2H_6
cosmic

2009(16ch)





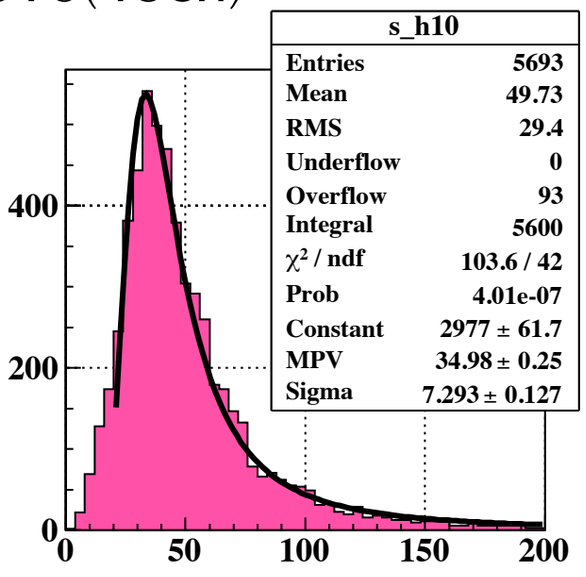
nsec

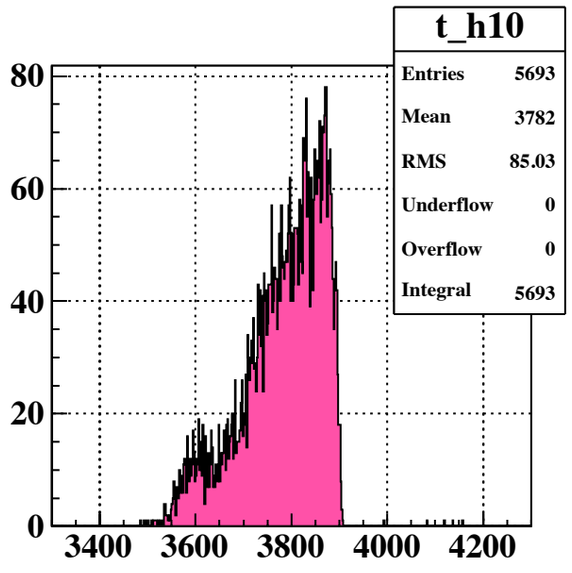
$$\frac{34.98}{179.6} = 0.20$$

- gain loss due to 50pF (~0.33)
- 1.4V/pC →1.1V/pC (0.79)
- Additional circuit for ASIC operation (~0.67)

0.33x0.79x0.67=0.17

2010(48ch)





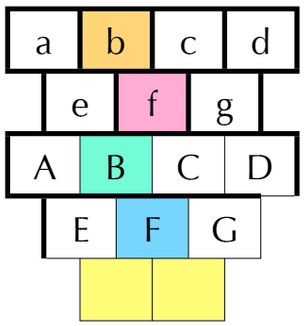
nsec

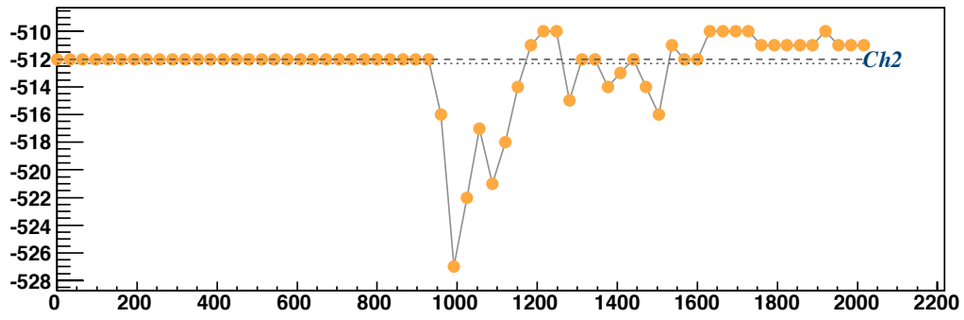
Haxis [nsec]
Vaxis=ADCx(-1)

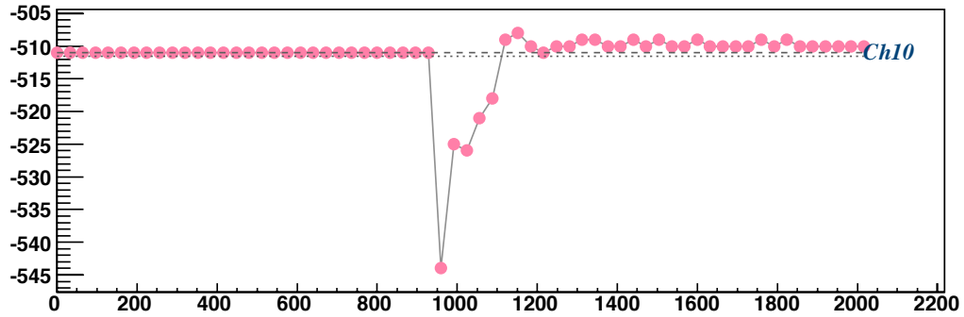
waveform sampling

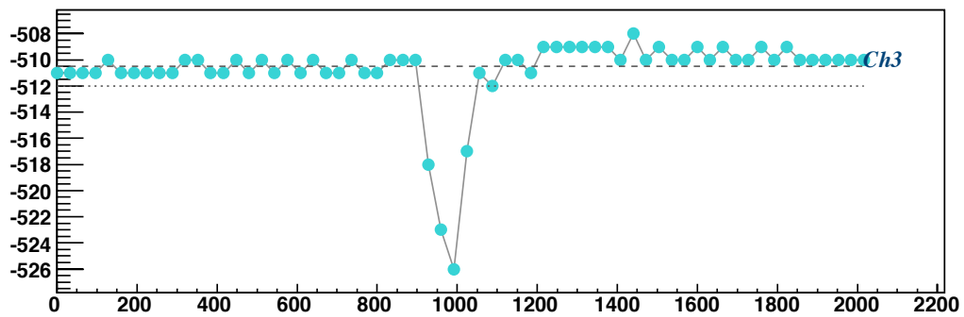
cosmic ray data

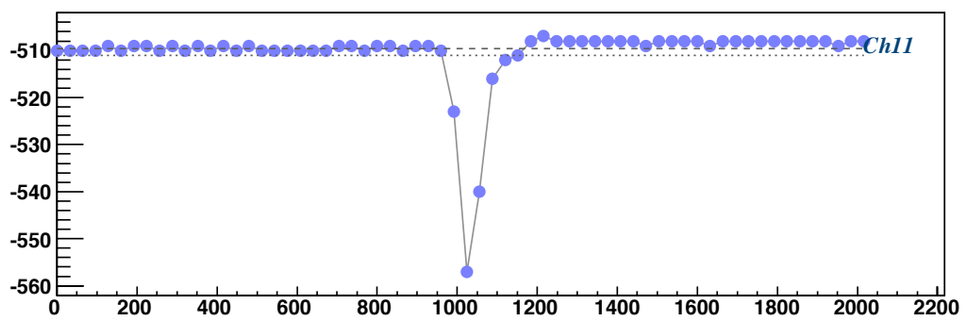
e3



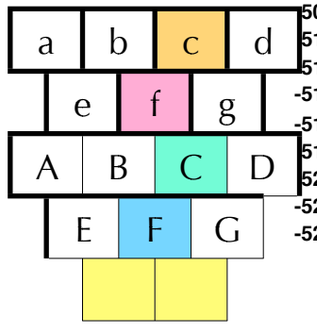


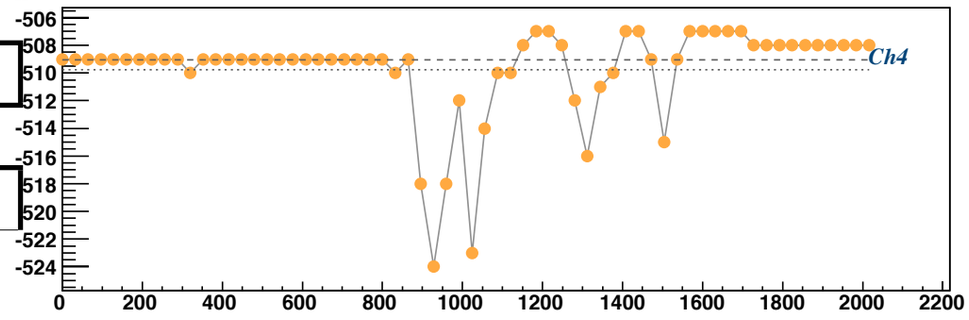


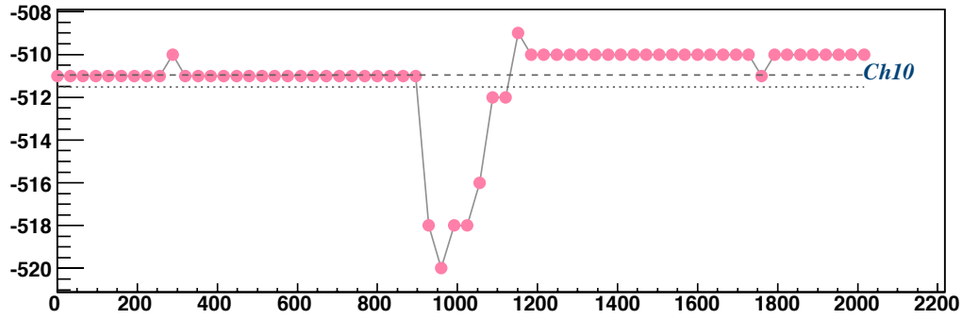


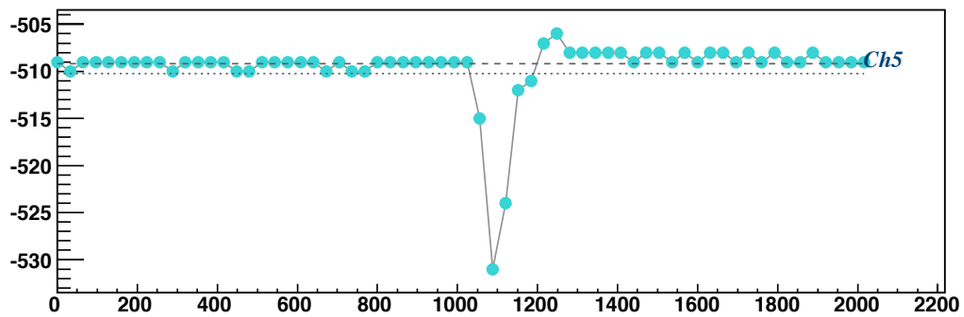


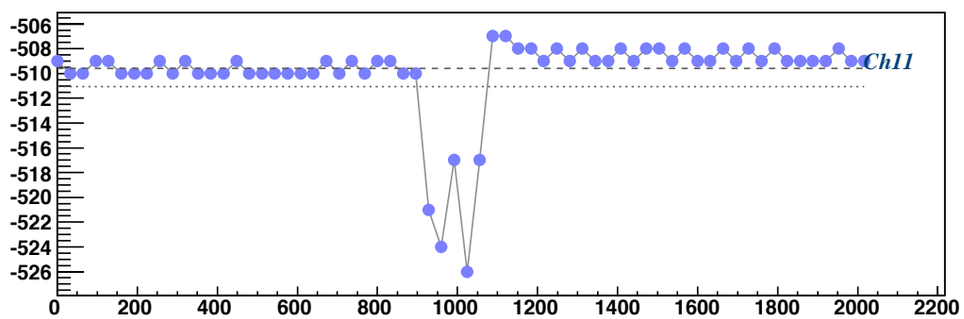
e5







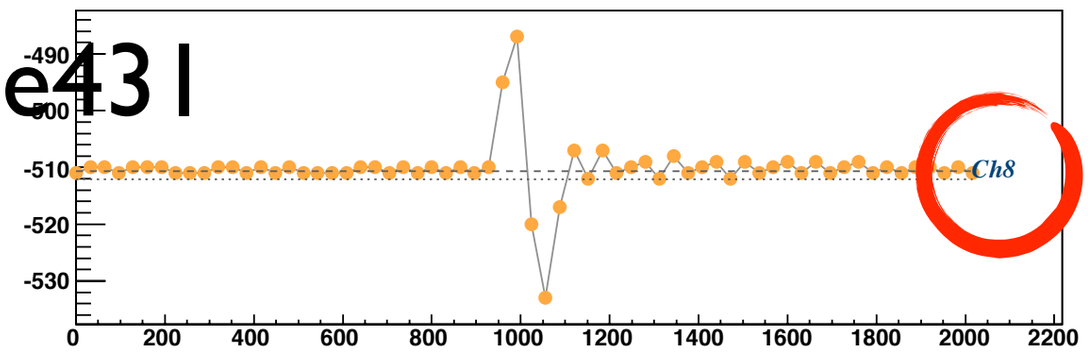


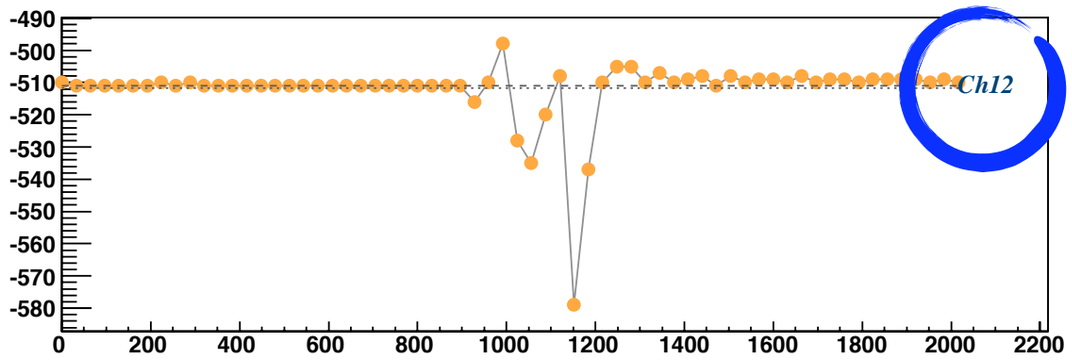


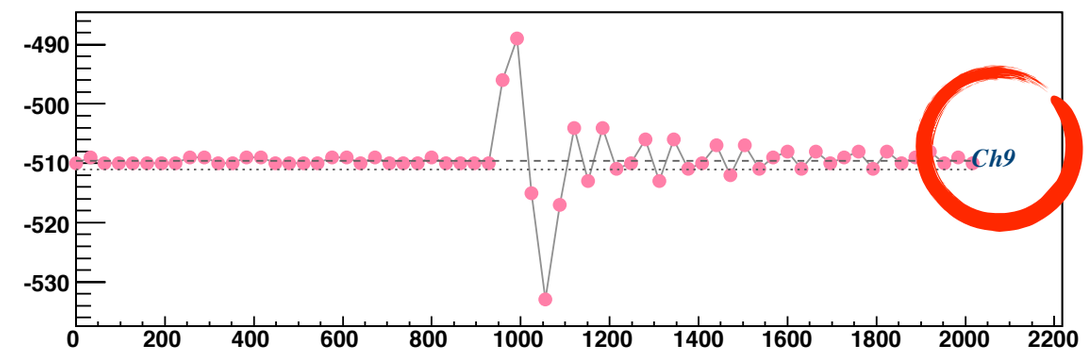
cross talk in ASD chip

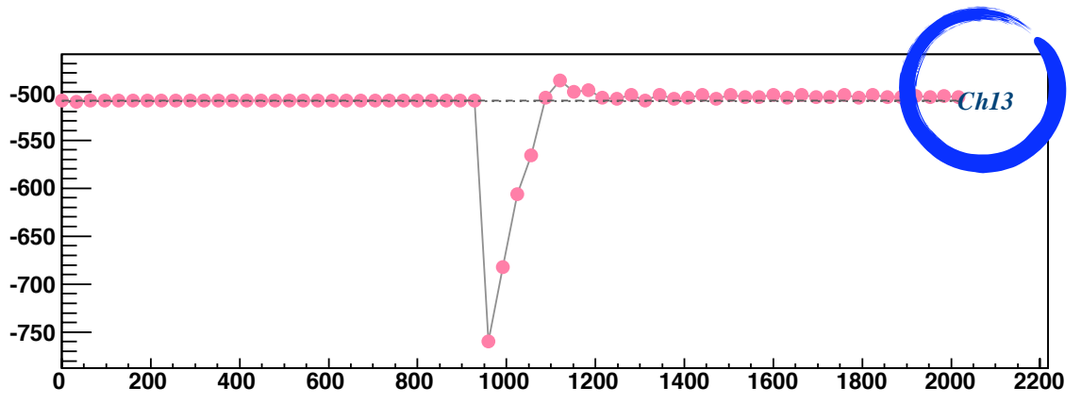
cosmic ray data

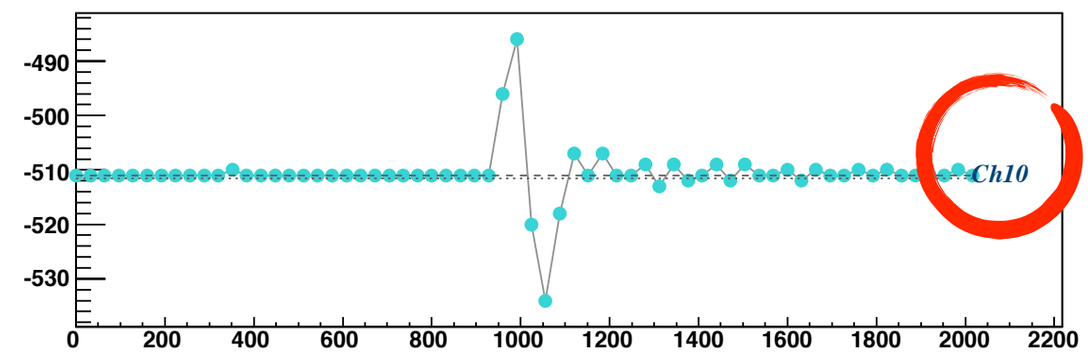
e431

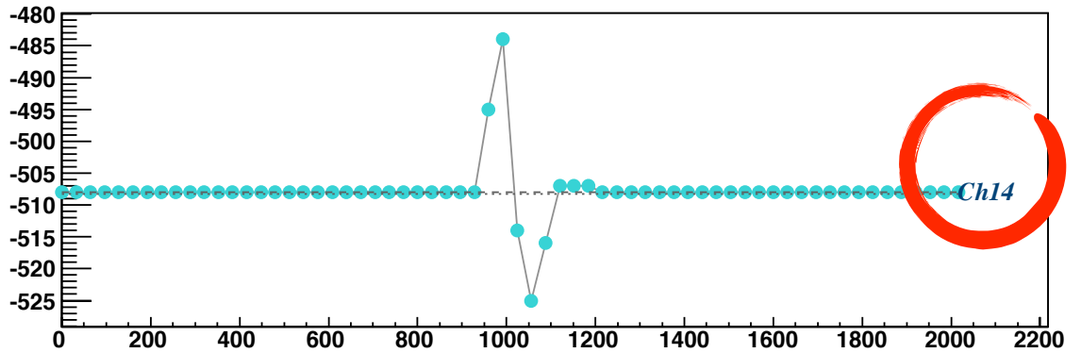


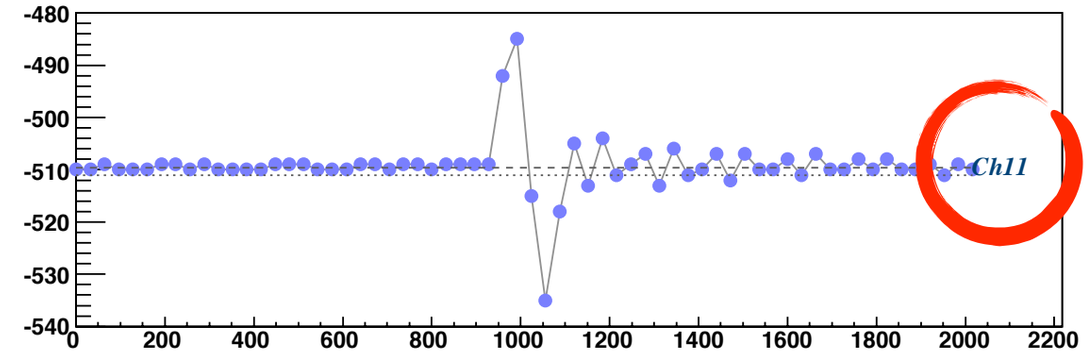


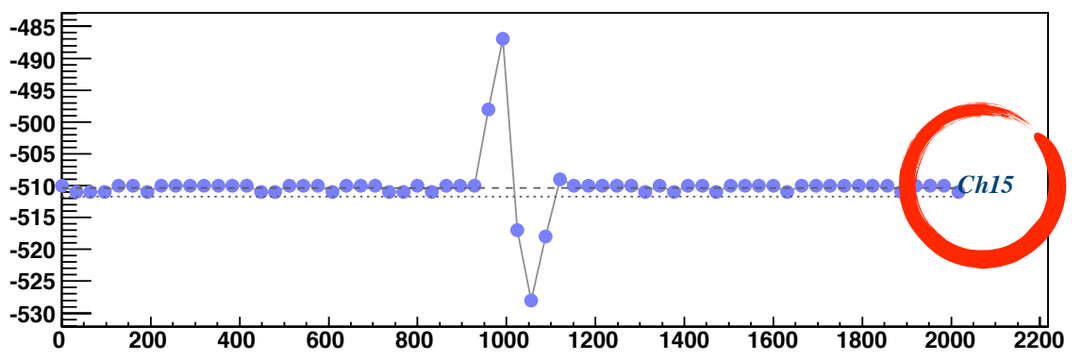












raw data

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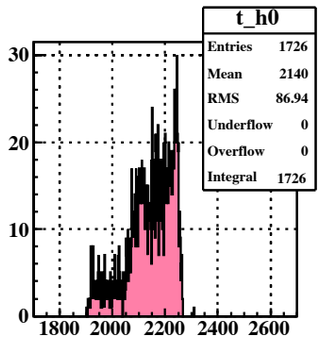
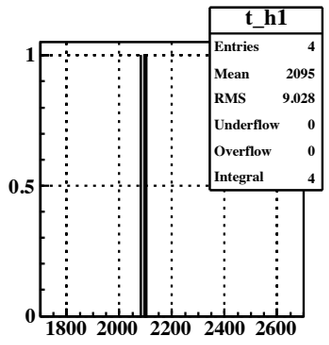
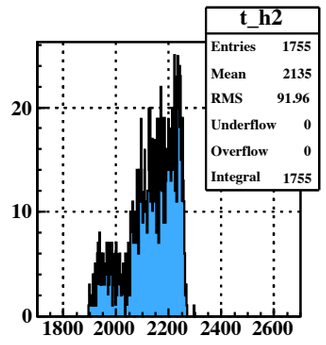
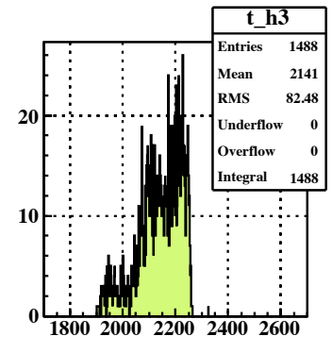
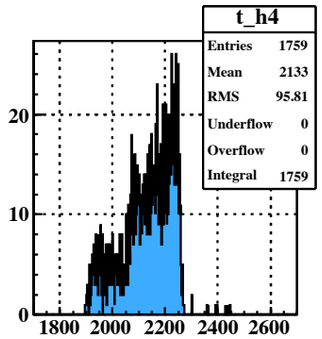
TDC distribution (ver.09)

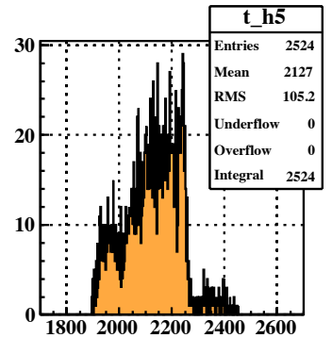


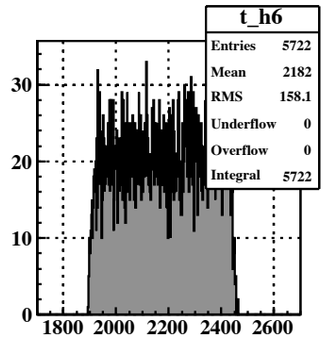


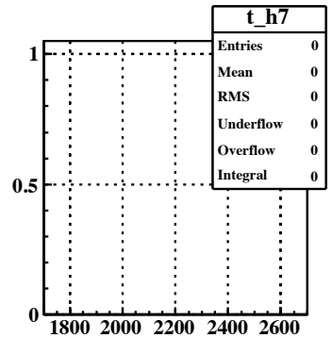


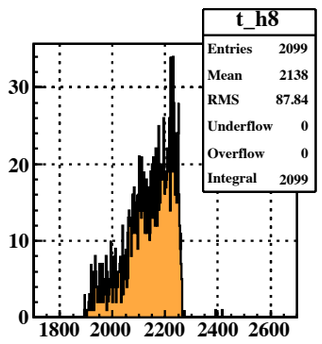


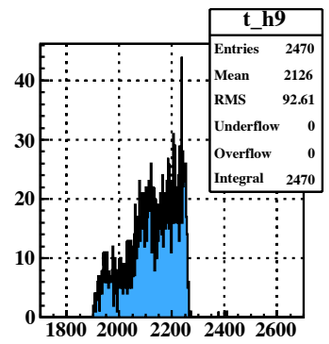


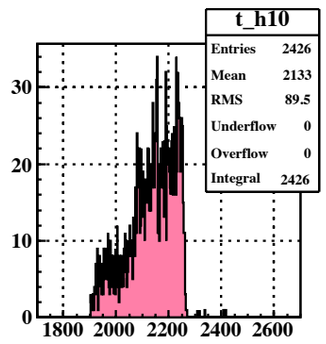


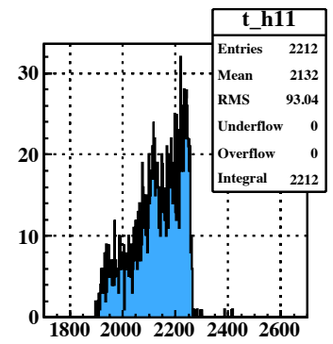


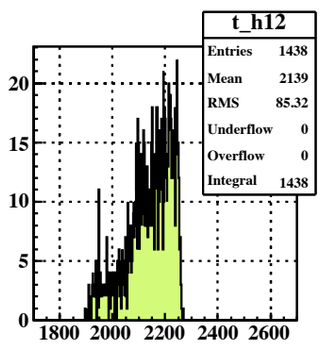


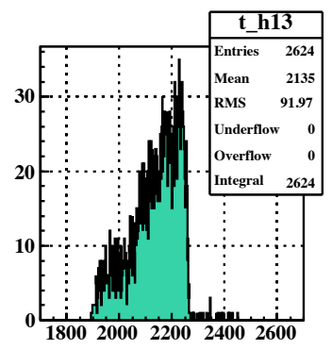


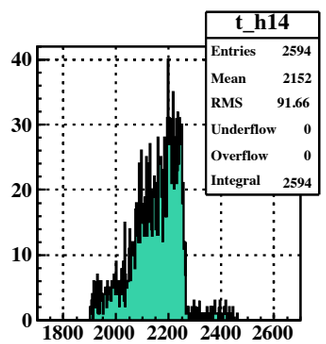


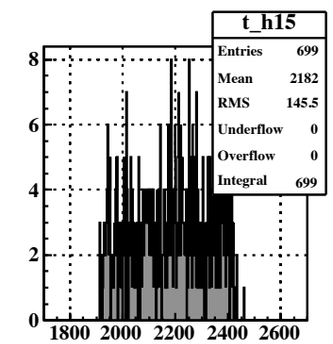






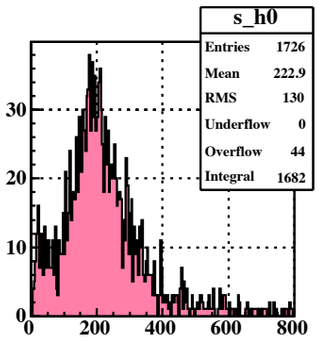


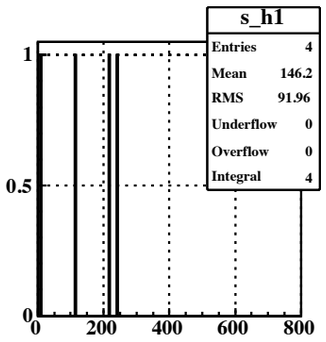


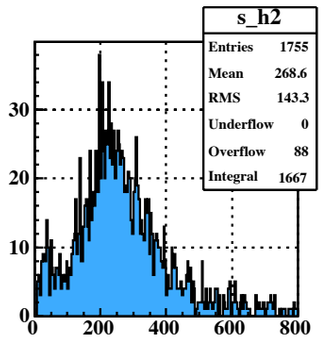


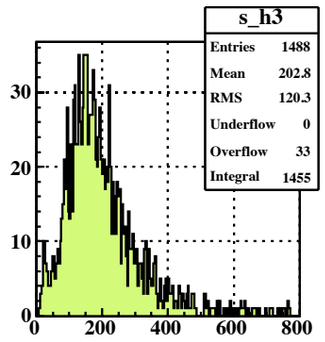
HV=2.3kV
He:C_2H_6
V_{th}=20mV
cosmic

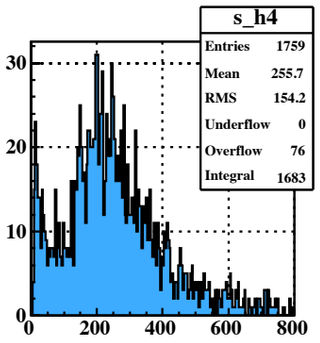
ADC sum distribution (ver.09)

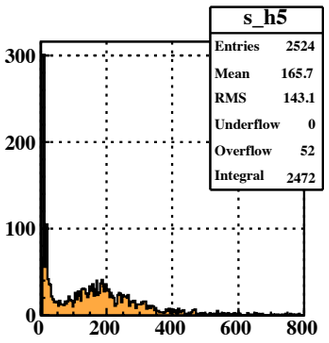


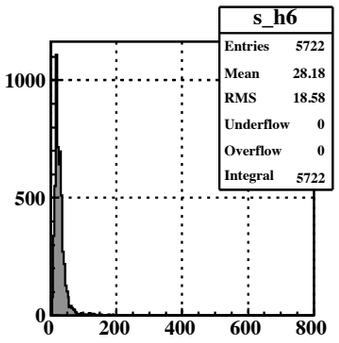


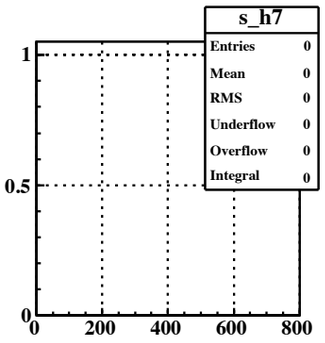


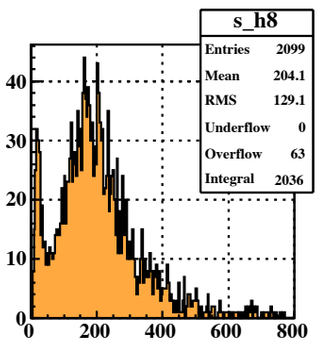


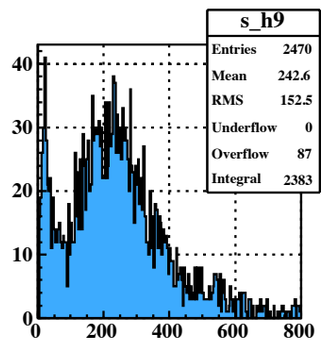


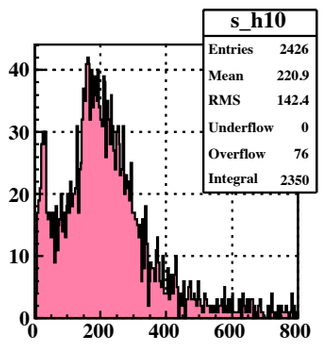


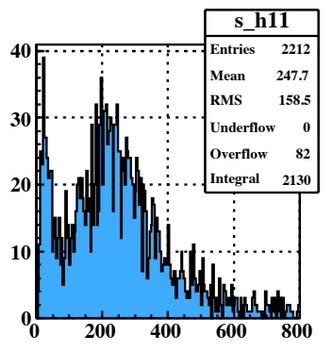


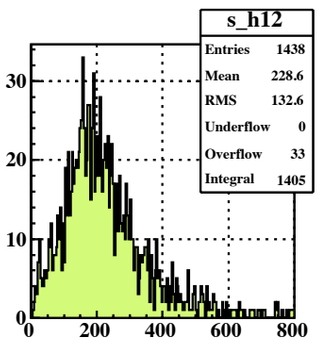


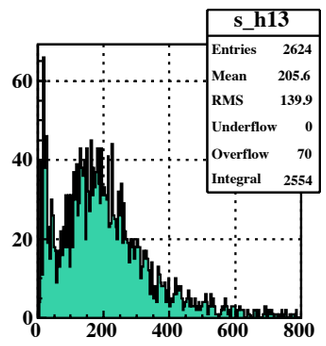


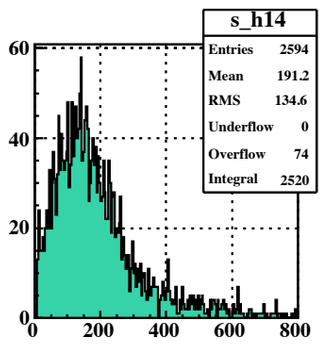


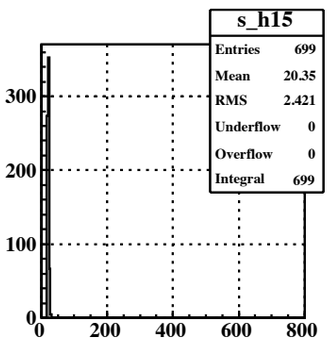












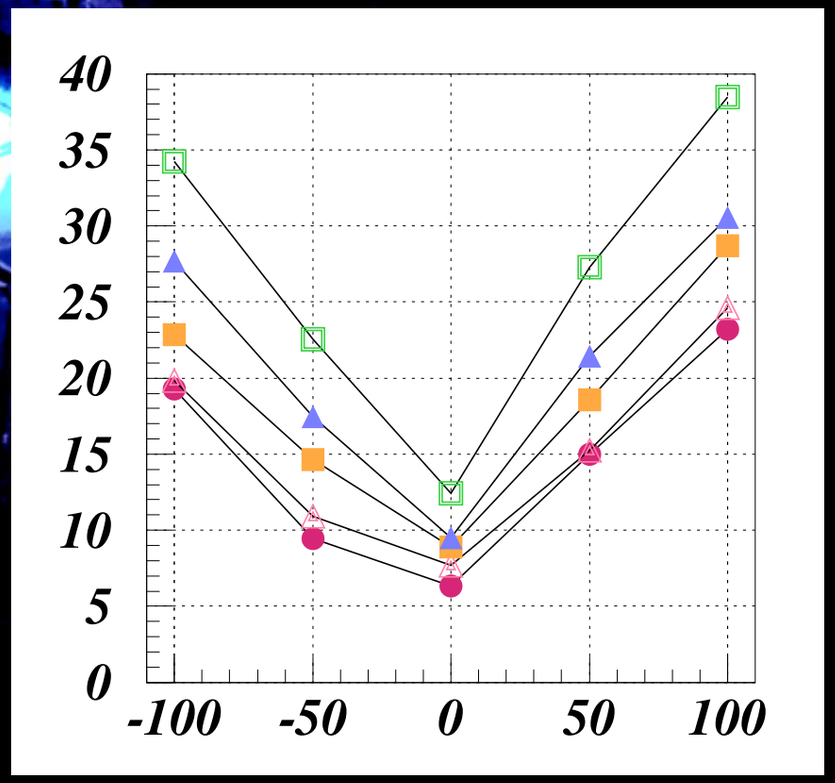
HV=2.3kV
He:C_2H_6
V_{th}=20mV
cosmic

Results

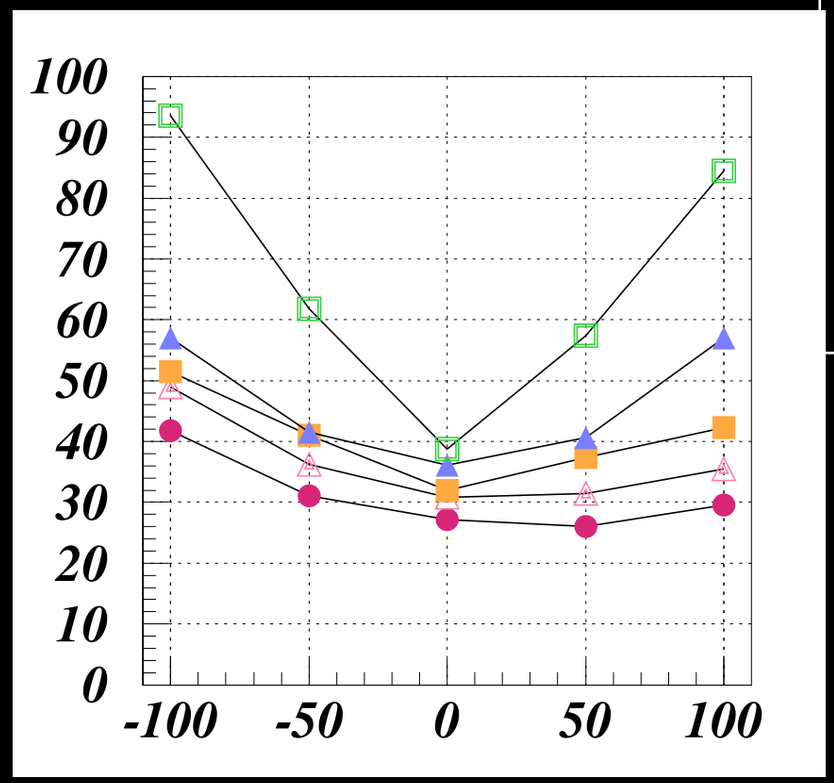
HV=2.5kV

sampling rate
20MHz
32MHz
40MHz
100MHz
4GHz

pulse height max

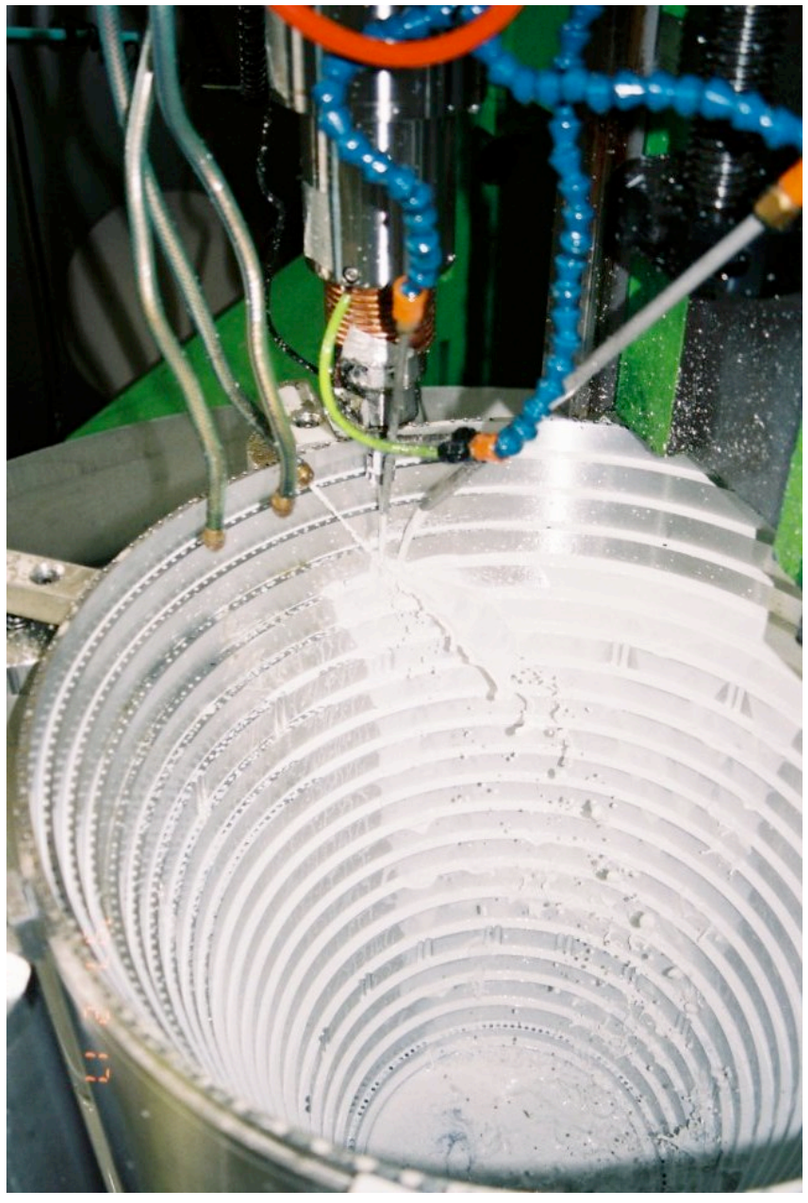


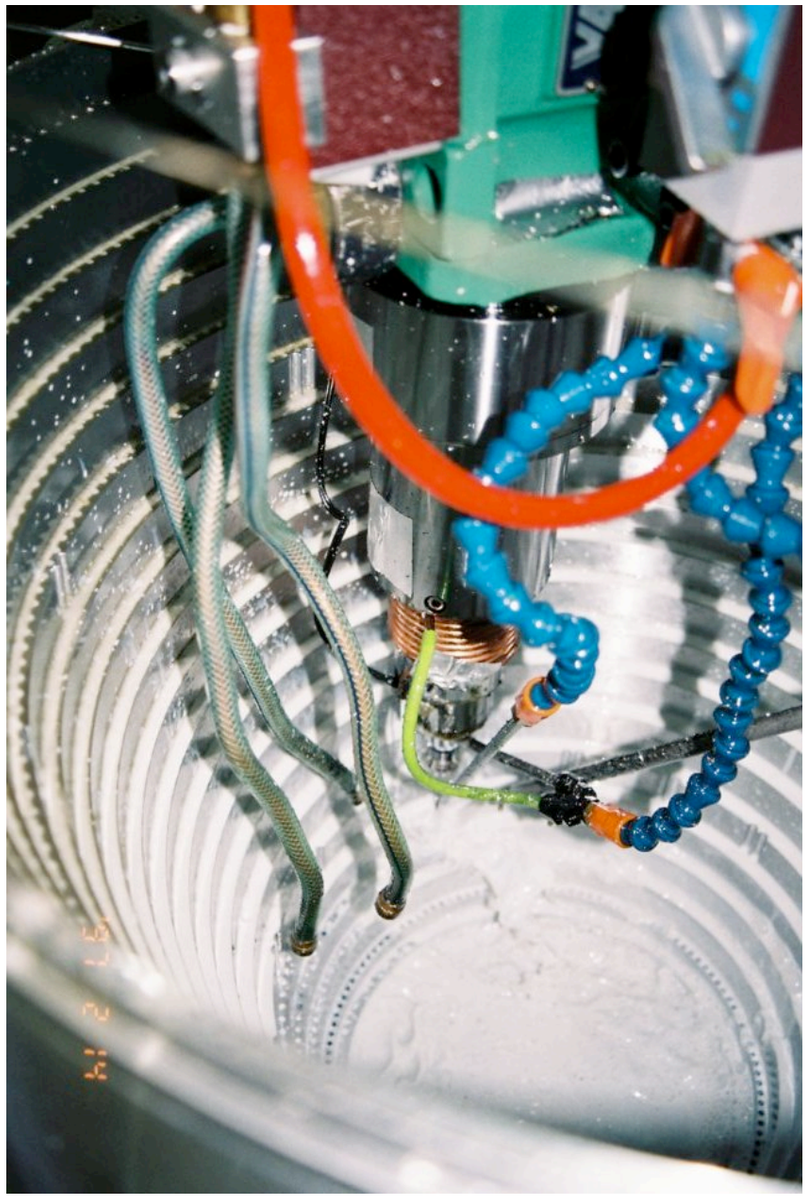
ADC sum



- better to take an asymmetry of pulse heigh max
- 6.3cm@0cm (4GHz sampling) is the best
- ~9cm resolution at 32-40MHz sampling (@0cm)
  - ~13cm resolution with 16ch readout board (previous measurements)

Photos at drilling holes for the inner endplate of Belle-CDC.
It was quite hard. It took long time to make it.

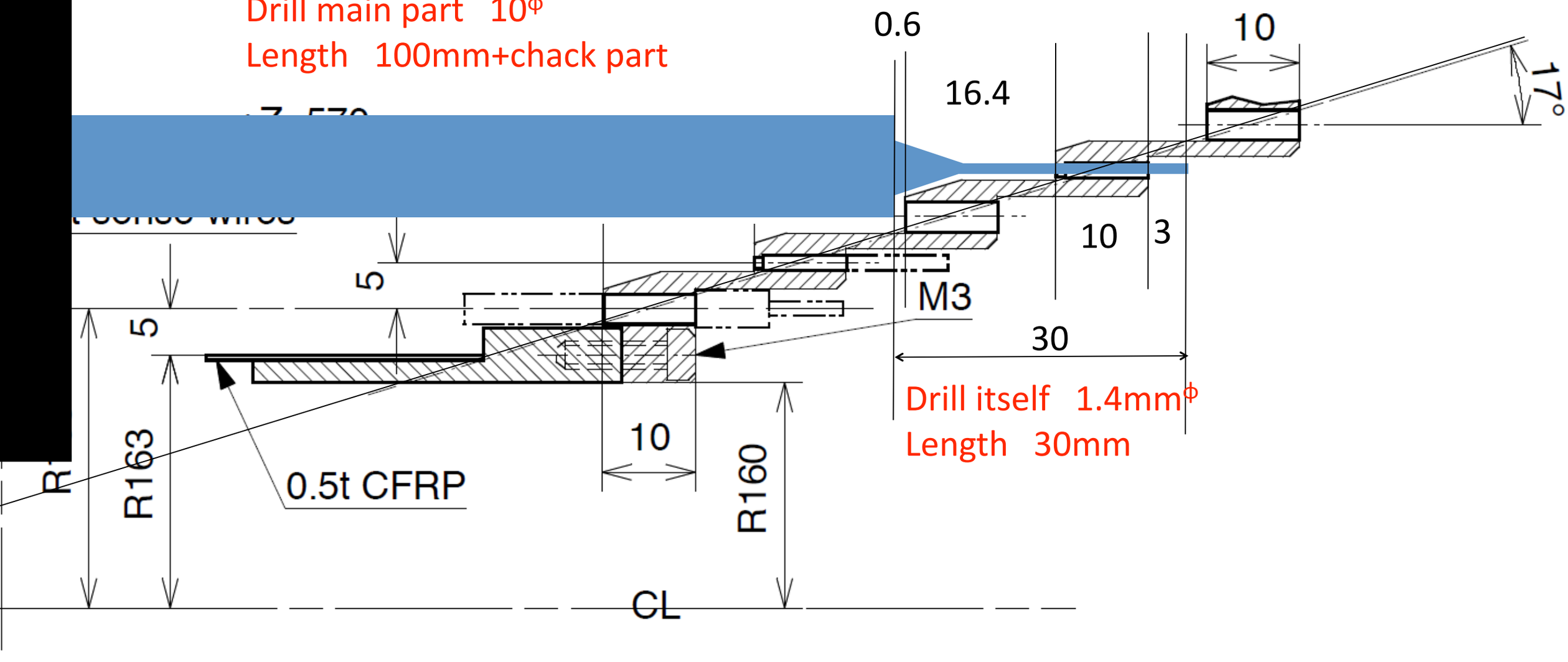




Drill for small cell part

チャック　60ϕ

Drill main part　10ϕ
Length　100mm+chack part



Drill itself　1.4mmϕ
Length　30mm

Disassembling schedule

- Roll out: Dec-9
- Common stage and standing stage: Dec-27, 28
  - –Night time: Removing CDC cables
  - –Please come and help us.
- CDC removing jig: Jan-4,5
- CDC removing: Jan-6,7,8
  - –If you are interesting, please see it.
  - –CDC will be brought to Fuji experimental hall, temporally.
- Disassembling CDC jig: Jan-10