SCTA128VG user reference
Version 1.3

1. Architecture and basic principles.

Figure 1 shows the block diagram of the SCTA128VG designed for readout of silicon and diamond detectors with capacitance from 2pF to 20pF. The chip comprises five basic blocks: front-end amplifiers, analogue pipeline, control logic including the derandomizing FIFO, command decoder and output multiplexer. Four 5-bit DACs for the bias of the analogue part of the chip and one 8-bit DAC for the calibration circuit have been implemented in the chip.

The front-end circuit is a fast transimpedance amplifier followed by an integrator, providing a semi-gaussian shaping with a peaking time of 20-25ns, and an output buffer. The peak values are sampled at 40 MHz rate and stored in the 128-cell deep analogue pipeline. Upon arrival of the trigger the analogue data from the corresponding time slot in the ADB are sampled in the S&H buffer and sent out through the analogue multiplexer.

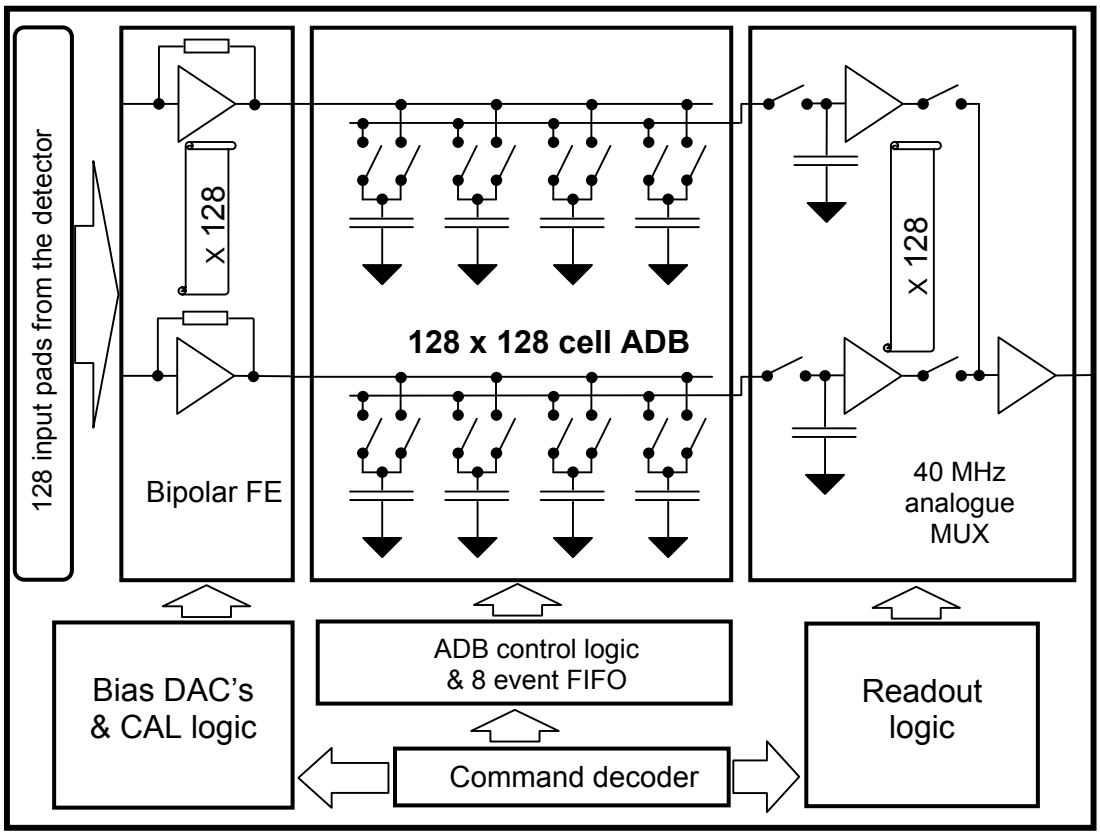

Figure1: Block diagram of the SCTA128VG chip.

2. Front End

The gain of the FE amplifier is of about 50mV/fC. The designed peaking time for nominal parameters (resistors, capacitors) is roughly 20ns. The front-end circuit is designed in such a way that it can be used with either polarity of the input signal, however the full read-out chain (NMOS switches in the analogue pipeline, output multiplexer) is optimised for the p-side strips. The dynamic range of the amplifier is designed for 12fC input, which together with the gain of 50mV/fC gives the full swing at the output of the FE in the range of 600mV. This dynamic range is guaranteed over all possible process variation (from batch to batch), temperature 0-80^{o}C, and +/-10% power supply variation, before and after irradiation.

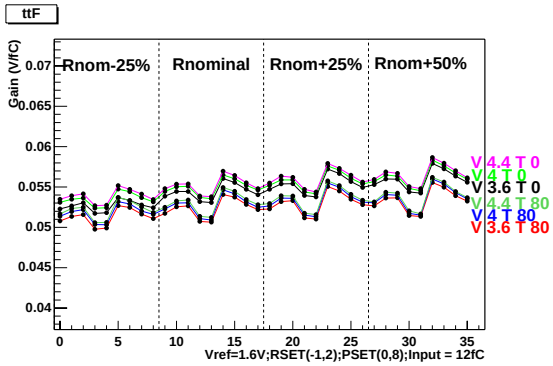

Figure 2: Evolution of gain[V/fC] with variation of the process parameters (Resistors -25% ÷ +50%, CMOS corner parameters, temperature from 0 to 80^{o}C, power supply ±10%). The variations of the process parameters are from batch to batch. For a given batch the matching of the device parameters on chip/wafer is much better.

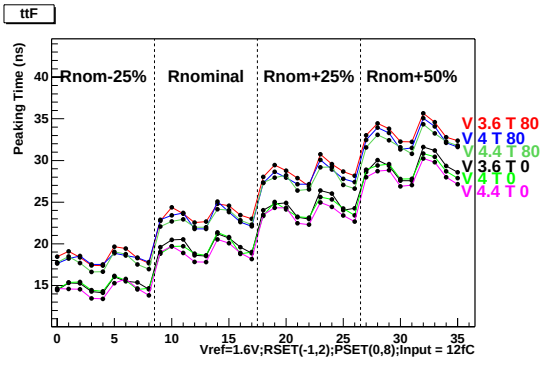

Figure 3: Evolution of peaking time [ns] with variation of the process parameters (Resistors -25% ÷ +50%, CMOS corner parameters, temperature from 0 to 80^{o}C, power supply ±10%).

We expect some variation of the circuit parameters depending on the operating conditions (temperature and supply voltages) and the variation of process parameters from run to run. In order to illustrate possible effects we show in Figure 2 and Figure 3 simulation results for gain and peaking time respectively for various combinations supply voltages, operating temperatures and corner process parameters as defined by the technology vendor. The corner parameters include also worst-case combinations of initial parameters and expected radiation effects after total dose of 10Mrad.
The checking of the performance of the circuit for 50% higher values of the resistances is only to show the robustness of the circuit (maximum expected deviation is 25%).

There are four 5-bit DACs implemented in the chip, which allow one to set the current in the input transistor, the current in the shaper, pipeline buffer and read-out amplifier. The current in the input transistor can be set within the range from 0 to 320µA using the **preamp DAC**. The nominal setting of about 200µA is foreseen for a detector capacitance in the range 15pF to 20pF. For very low input capacitance (up to 5pF) the value around 120µA should be used. The actual bias current providing a maximal signal-to-noise ratio for a given detector capacitance depends on the value of the current gain factor ß as well as on the detector leakage and the detector bias resistance. Therefore for each detector the optimum bias of the input transistor should be found experimentally. Furthermore, the current gain factor ß of the input transistor

will be degraded after irradiation which will require readjusting of the bias current for optimising the signal-to-noise ratio.

The **follower DAC** provides a reference current which is used to control bias currents in the two gain stages of the front-end amplifier. This current can be set within the range from 0 to 40μA. The nominal value of the follower current is of about 20μA. The setting of the follower current is not very critical, however, a setting different from the nominal one may be used in order to compensate changes in the circuit due to possible variation of the process parameters.

The **shaper DAC** provides a reference current which is used to control bias current in the output buffer of the front-end amplifier (in front of the ADB). This current can be set within the range from 0 to 360μA. The nominal value of the shaper current is of about 180μA. This value guarantees a good linearity and no speed loss for the 600mV fast (20ns peaking time) pulses at the output of the FE amplifier in front of the ADB. For detector, which provides a smaller signal (thin Silicon detector, diamond detectors, HPD detector) when the expected dynamic range is smaller, it will be possible to optimise this current to limit the power consumption without degradation of the buffer performance.

The reference voltage **VREF** is used in the front-end circuit as well as in the readout amplifiers so that it provides good tracking of the DC levels in output buffer of the front-end and in the readout amplifier. The nominal value of this voltage is of about 1.6V.

The bias current in the ADB readout amplifier is controlled by another 5-bit DAC (**ADB readout DAC**). This current can be set within the range from 0 to 120μA. The nominal value of the ADB readout amplifier current is of about 60μA.

3. Readout

Two SCTA128 chips can be read out via one fibre line. The readout sequence is initiated by an L1 trigger transmitted through the command lines in coded format (110). Once the trigger signal arrives, the pointed physical address of the 128-channel memory column with the sampled analogue values is stored in a derandomizing FIFO. The segment written in the pipeline corresponding to the trigger is protected and will not be overwritten before the event has been read-out or the pipeline has been reset. Up to 8 events can be stored in the derandomizing FIFO. In case of overflow the control logic issues the overflow bit, which is bundled with the physical data, and the chip needs to be reset. Since part of the ADB is spent on the derandomizer buffer the overall delay of the ADB is 118 clock cycles. For the next event to be readout the pipeline sends the data to the multiplexer which produces a serial data stream.

The second front-end chip on the same fibre waits for the first chip to finish data transmission by pausing the appropriate number of clock cycles before sending the data.

The scheme for the termination of the analogue outputs of the multiplexer in case of single and two-chip readout is shown in Figure 4. Programming of the “add1rst” and “singread” inputs does the selection of the readout mode.

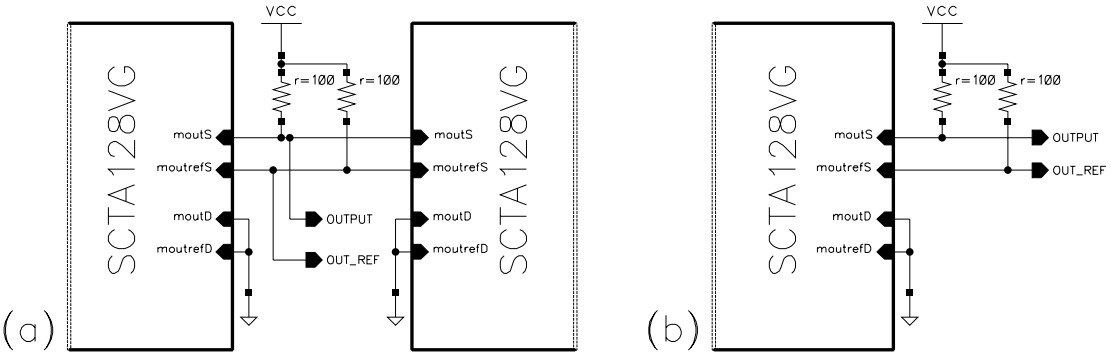

Figure 4: Output terminations for two (a), and for single chip readout (b)

When the chip is in idle state a DC level of about 2.8V appears at "moutS" and moutrefS, which allows for a faster transition when the chip starts sending data for 40 MHz operation. For two-chip readout when one chip is sending the data the other one is in "HiZ" state, when both are in idle state there is a DC level of about 2.75V at the outputs.

The value of the terminating resistor is 100 Ohm for 40 MHz readout speed and maximum (60pF) load capacitance. For lower capacitance and slower readout (the speed of the output multiplexer can be programmed between 5 and 40 MHz) a higher value of this resistor is suggested which will limit the power dissipated by the output stage.

4. Description of the readout logic

A diagram of the readout logic is shown in Figure 5. On reception of a trigger, the four-bit counter is incremented. The sequencer starts producing the necessary readout control signals provided that the counter (which reflects the buffer occupancy) is not zero, and a 'stop' is not being generated by the start/stop logic. The start/stop logic arbitrates the destination of the "readbit" according to the chip address (first or second chip on fibre) and the number of readouts to be performed (one or two). The "readbit" either passes to the multiplexer shift register, thus sequentially outputting the analogue information, or is used to generate the 'stop' signal to indicate that a new sequence should not be generated yet. When one readout sequence is completed, the four-bit counter is decremented, reflecting the fact that the buffer has had one event removed.

An analogue signal package from one chip consists of a seven bit header (1011010) followed by 128 analogue samples with physical data from the detector, a one bit buffer overflow flag, a four bit BCO counter (bco<0> bco<1> bco<2> bco<3>) and a four bit T1 counter (L1<0> L1 <1> L1<2> L1<3>). The above format of the data is independent of mode of readout (single or two chip readout). The total time for readout on one fibre for two chips is thus 2 x (7+128+1+4+4) x 25ns = 7.2 µs. The DC level for the high state ("1") is about 2.9V and for the low state ("0") is about 2.3V.

The four-bit BCO counter and L1 counter returned by the chip can be used for unique association each trigger with the physical data from the detector.

Figure 6 and 7 show a results of the simulations of 2 multiplexers consisting of full header/trailer part and 5 analogue channels (instead of 128) working with 40 MHz readout speed, loaded with 100 Ohm resistor and a parasitic capacitance of 60pF. The DC level on the "moutrefS/moutrefD" output can be used for differential sending of the data outside the detector module. The header data sent by the second chip should

not be used for any processing because it may be distorted in the moment of switching from first to second chip output.

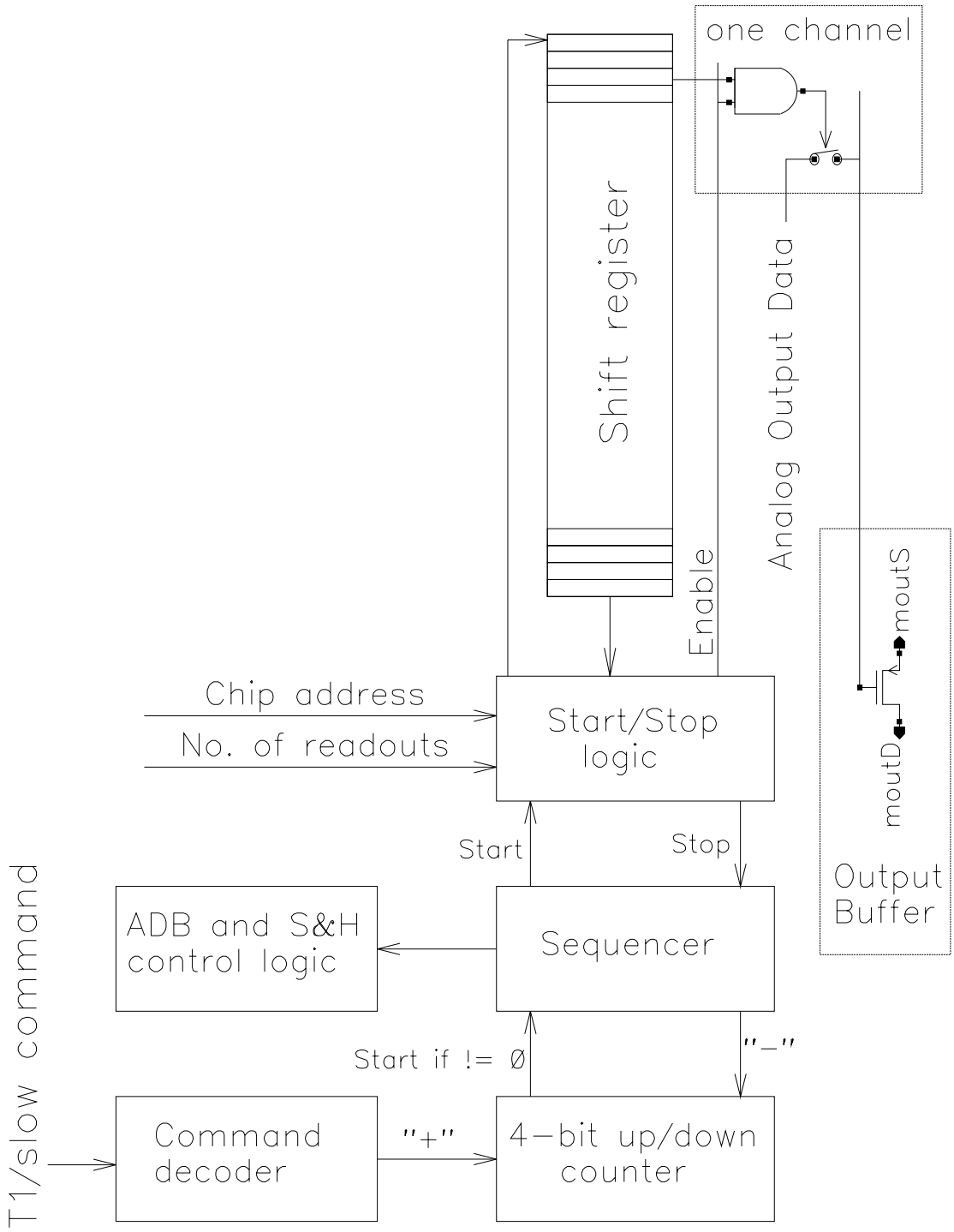

Figure 5: Block diagram of the readout logic (including ADB control)

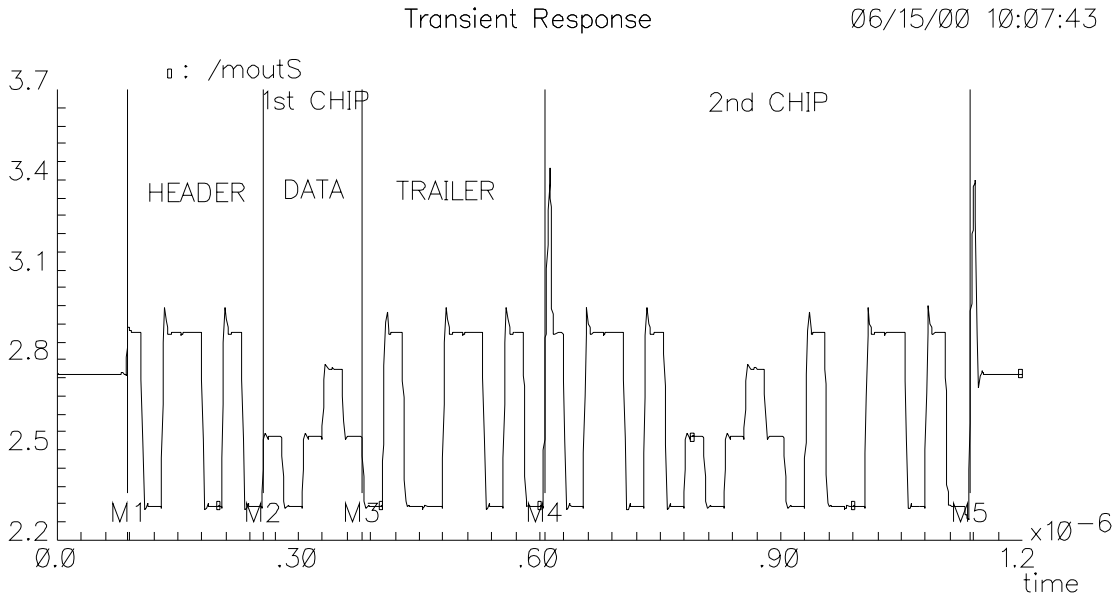

Figure 6: Simulation result of 2 chips sending data sequentially. Only 5 analogue channels have been simulated (instead of 128)

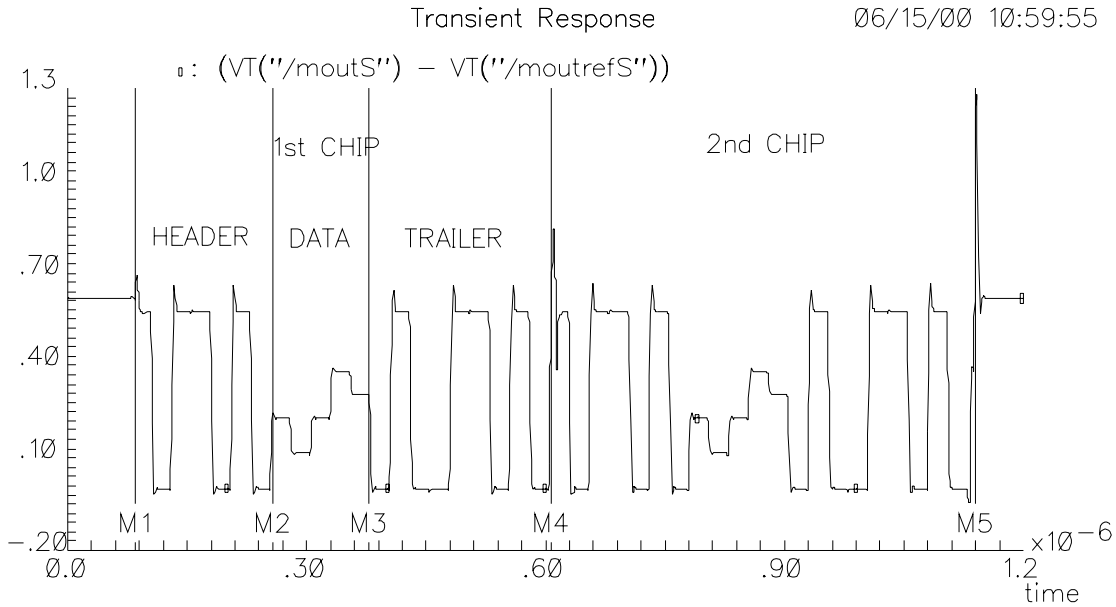

Figure 7: Simulation result of 2 chips sending data sequentially in case of differential readout.

5. Layout

The SCTA128VG chip occupies an area of 8.8 x 8.1 mm^2. The pad list of the chip is given in Table 1 and the layout is shown in Figure 8.

Table 1: SCTA128VG pad list.

Pad name	Function	Description
Gndadet!	supply	Analogue ground (0V).
Gndac!	supply	Analogue ground (0V).
Gnda!	supply	Analogue ground (0V).
Vccc!	supply	Analogue power supply (nominal 4V).
Vcc!	supply	Analogue power supply (nominal 4V).
Avdd!	supply	Analogue power supply (nominal 4V).
VREF!	input	Reference voltage (nominal 1.6V), low impedance.
A1_ring!	ring	Analogue guard ring (connect to analogue ground).
A_ring!	ring	Analogue guard ring (connect to analogue ground).
CBG	Test output	Test output of the band gap reference (allows for biasing of the chip in case of failure of the band gap reference (in this case 28kOhm resistor to gnd).
ICALPROBE	Test output	Test output of the **Calibration DAC**. Range 0 – 160mV corresponding to the Calibration signal 0 – 16fC.
IFOLLPROBE	Test output	Test output of the **follower DAC**. Range 0 –K[1]×40mV corresponding to the current 0 - 40µA. Nominal follower current is about 20µA.
ISHPROBE	Test output	Test output of the **shaper DAC**. Range: 0 - K×40mV corresponding to the FE output buffer current range 0 - 360µA Nominal shaper current is about 180µA
IPPROBE	test output	Test output of the **preamp DAC**. Range: 0 - K×80mV corresponding to the preamplifier current range 0 - 320µA. Nominal preamplifier current: 100µA - 250µA depending on the detector capacitance.
CASPROBE	Test output	Test output of **ADB read-out DAC**. Range: 0 - K×60 mV corresponding to the current range 0 - 120µA. Nominal setting for DAC is 50µA - 80µA.

[1] K=RBXBnor/RLVnor where RBXBnor is the normalised value of the extrinsic base resistor (RBXBactual/RBXBnominal) and RLVnor is the same parameter for low value resistor. Actual value for RBXB (valid for wafer/batch) can be measured from ICALPROBE pad to the ground (250 Ohm nominal). Actual value for RLV can be measured from ISHPROBE or IFOLLPROBE to ground (250 Ohm nominal).

REFPPROBE	Test output	Test output of the current reference (allows for biasing of the ADB and MUX amplifiers in case of failure of the reference (in this case 28kOhm resistor to gnd).
Test0	Input or test output	Calibration test inputs. The input can be used for providing external calibration signals when the internal calibration circuitry is not used or for probing the calibration signals if the internal calibration circuitry is used. Only one calibration line from four is available externally.
Probe_test!	Test input	Two pads internally shorted. May be used during the wafer screening to test the alignment of the chip (by measurement the resistance between).
i<0>,..,i<127>	Inputs	Inputs from detector.
moutS, moutD	Outputs	Analogue outputs, multiplexed (see Fig.2)
moutrefS moutrefD	Outputs	Reference analogue outputs, (can be used for differential receiver)
Dvdd!	supply	Digital power supply (nominal 5V).
Dvss!	supply	Digital ground (gnd).
ring_dig	ring	Digital guard ring (gnd).
CommandP CommandN	inputs	Command input (LVDS[2]). Can be tested on **CommandT** pad.
ClockP, ClockN	inputs	Clock input (LVDS).
ResetExtB	inputs	Reset input. Ex-or with internal power-up reset signal. Can be test on **ResetBT** pad. Active low.
add1rst	input	Bit to set the first and the second chip on the module. Set to high for the first chip.
singread	input	When set to high, only the first chip on the module sends the data.
TestEnable	input	Enables test outputs from logic. Pulled down to ground. Active high.
ErrorT	test output	Unrecognised command. A pulse on this output indicates that the command decoder has not recognized command. Enabled by **TestEnable.**
WPTRBT	test output	ADB write pointer bypass flag. Normally pulsed every 128 clock cycles. Enabled by **TestEnable**.
RPTRBT	test output	ADB read pointer bypass flag. Normally pulsed every 128 clock cycles. Enabled by **TestEnable.**
ClkRegT<1:0>	test outputs	Shows contents of the clock register. Enabled by **TestEnable**.
ResetBT	test output	Internal reset signal. Enabled by **Test Enable**.
CommandT	test output	Internal command signal. Enabled by **TestEnable**.

[2]There is NO terminating resistor for LVDS receivers inside the chip. It should be provided externally.

ReadoutClkT	test output	Read-out clock. Enabled by **TestEnable**.
MuxTestEnable	input	Enable test outputs for multiplexer. Pulled down to ground. Active high.
RBitBT	test output	MUX bypass flag. Enabled by **MuxTestEnable**.
EnableBT	test output	MUX enable flag. Set when chip is sending the data. Enabled by **MuxTestEnable.**

All inputs are CMOS level by default. Other kinds of inputs are described explicitly.

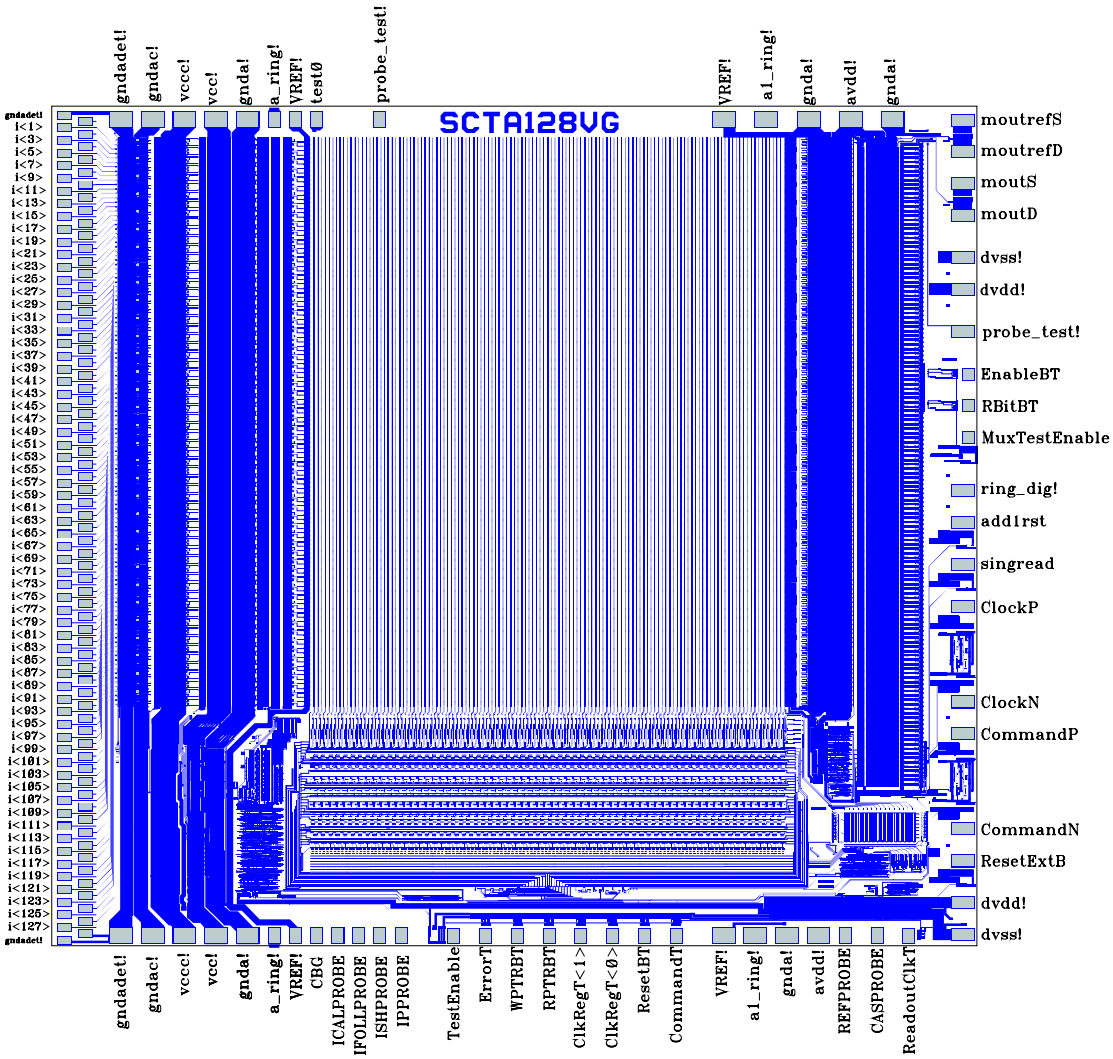

Figure 8: SCTA128VG pad layout. Size of the chip: 8.8mm length, 8.1mm height.

6. Protocol

The commands enter the chip via the serial interface as a serial bit pattern synchronous to the main clock. The data on this line is latched by the rising edge of the clock.

Table 2: SCTA commands.	
Code	**Description**
110	Level 1 trigger
01111 0001x...x (16 bits)	Soft reset (16 clock period long).
01111 0010 bbbbbx...x (15 bits) + 01111 0010 d...d (15 bits)	Load biasing DACs. NOTE: command has to be repeated twice. The first execution loads **shaper DAC** (FE output buffer DAC) using five most significant data bits (bbbbb); the second execution loads the following DACs: **preamp DAC** (5bits), **follower DAC** (5bits), **ADB readout DAC** (5bits). MSB first (d…d).
01111 0011 b...b (14 bits)	Load calibration DAC (8 bits) and delay register (6 bits), MSB first.
01111 0100 cc	Load clock register with cc. The output frequency is clock frequency divided by: 1 for cc=00, 2 for cc=01, 4 for cc=10, 8 for cc=11 (default after reset).
01111 0101 aa	Load test pulse register address with aa. When aa=00 test pulse is applied to front-end channel number 0,4,...,124, (default aa=00).
01111 1001	4 consecutive L1 triggers
01111 1010	8 consecutive L1 triggers
01111 1101	Send test pulse to front-end (16-clock period long).

aa, b...b, cc, d...d - data for registers.
x, x...x - any bit value.

Note 1: maximum number of consecutive triggers is 8 because the FIFO length is 8.
Note 2: before L1 trigger command, which comes after slow command, two extra zeros are necessary for correct execution.

7. Results from batch Z36217.

In this section we present test results obtained with SCTA128VG chips produced in 2000 year, lot Z36217. The basic parameters of the chip have been evaluated using internal calibration circuitry. The internal calibration circuitry provides a well-defined voltage step at the input of the calibration capacitors connected to every channel. Since the characteristic of the calibration DAC can be measured, the inaccuracy of the electronic calibration is related only to the deviation of calibration capacitors from the nominal value and the mismatch of the resistors used for scaling of the calibration voltage. For comparison with the results obtained with the electronic calibration, the absolute calibration of the chip in the set-up with a silicon pad detector and beta source is also presented. The gain of the output buffer of the analogue multiplexer is in the range of 0.8[V/V]. . The gain of the front-end amplifier is about 50mV/fC. Therefore the final gain of the whole read-out chain is roughly 40mV/fC. All figures

in this section showing the gain and linearity refer to the full processing chain (front-end amplifier, ADB and output multiplexer).

A. Basic parameters of the Front-End amplifier.

The basic parameters of the amplifier are speed, gain, linearity and noise performance. The pulse shape at the output of the front-end amplifier has been evaluated by scanning the delay of the calibration signal with respect to the 40MHz-sampling clock for the analogue pipeline. In order to normalise the results to the absolute time scale the measurement has been repeated for two consecutive values of the trigger delay.

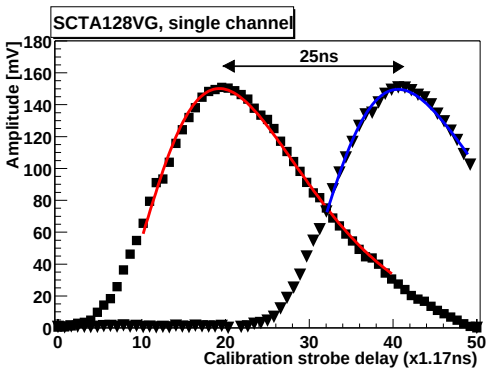

Figure 9: Pulse shapes at the output of the multiplexer obtained from the delay scan for two consecutive trigger delays.

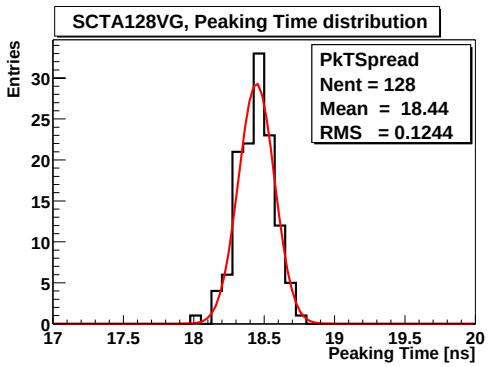

Figure 10: Distribution of the channel peaking times in one SCTA128VG chip. The RMS spread is about 0.6%.

Figure 9 shows the example of the measurement done for one typical channel of the SCTA128VG chip. The injected charge was 3.5fC. The obtained 18ns peaking time is in the expected range given by the technology process variation. The distribution of the peaking times in one SCTA128VG chip is shown in Figure 10. The RMS spread of the peaking times is in the range of 0.6%.

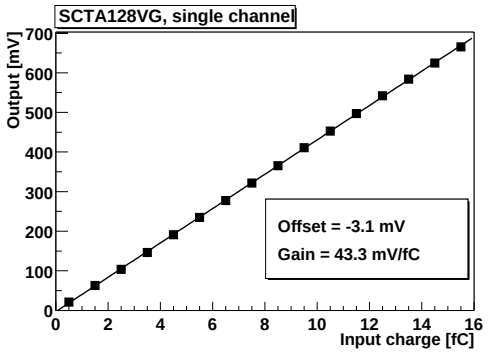

Figure 11: Gain linearity for one channel of the SCTA128VG chip.

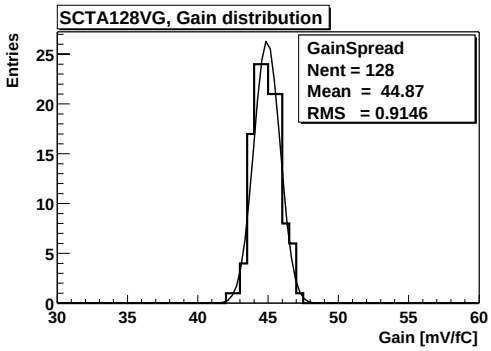

Figure 12: Distribution of channel gains in one SCTA128VG chip. The RMS spread is in the range of 2%.

Figure 11 shows the gain linearity for one channel in the chip. The gain is 43mV/fC and a good linearity is kept up to 16fC, which is the maximum range of the calibration DAC. The overall distribution of the gain in one SCTA128VG chip is presented in Figure 12. The RMS spread of the gains is about 2%, which is very good for tracking applications.

The noise measurements have been done for the whole chip working with a 40MHz clock sampling data to analogue memory and for random readout of ADB

cells. In this way any pedestal variation between ADB cells will contribute to the overall noise performance of the chip. The distributions of the ENC in one particular SCTA128VG chip for various input transistor biases are shown in Figure 13. For input transistor current ranging from 120µA up to 300µA the equivalent noise charge varies between 480 and 630e-. The RMS spreads of the ENC are in the range of 2 to 2.5%.

In order to verify the measurements with the internal calibration signal a set-up with a detector and beta source has been built. The SCTA128VG chip was connected to a SINTEF Silicon pad detector of thickness of 530µm. The detector bias voltage was set to 400V, 265V above the depletion voltage, providing sufficiently fast charge collection from the pads. The SCTA128VG chip was operating under nominal bias condition with input transistor current set to 200µA. Figure 14 shows the signal distribution from the detector exposed to beta particles. The gain extracted from this signal distribution, assuming the Landau peak corresponding to a charge of 5.7fC, is in the order of 44.2mV/fC. This has to be compared with the gain of 45.6mV/fC measured with internal calibration circuitry for the channel connected to a detector pad. A minor difference of 3% between the results of two measurements could be explained not only by the tolerance of the calibration capacitors and inaccuracy of the band-gap reference but also by a ballistic deficit for charge collected from the detector. The difference between charge collection time from the detector and charge injected from the calibration circuitry is in the range of 5ns, which is not negligible for a front-end amplifier with 18ns peaking time.

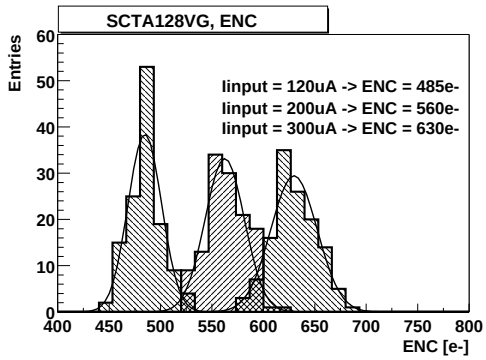

Figure 13: Distribution of ENC in a single SCTA128VG chip for different bias of the input transistor. The spread of the equivalent noise charge is in the range of 2 to 2.5%.

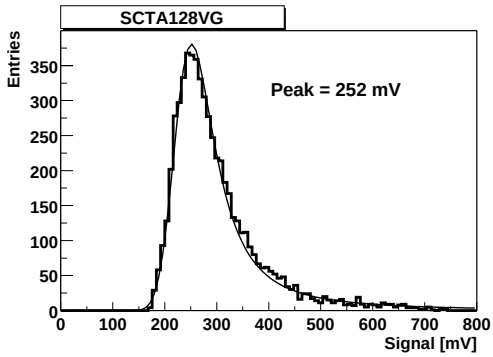

Figure 14: Histogram of data taken with silicon pad detector and a ^{106}Ru beta source showing Landau peak at 252mV.

B. Measurements with the external input capacitance

Figure 15 shows the measurements of the noise performance of the amplifier loaded with various capacitances and performed for several values of input transistor bias current. The measurement points (markers) are in good agreement with the predicted noise figures (lines). The minor difference in the predicted and measured values of about 10% for low input capacitances could be explained by the presence of the switching noise and slight (~1mV RMS) non-uniformity of the ADB pedestals, both contributing to the measurement as an excess noise. The overestimation of the noise figure for the capacitances above 22pF is probably due to the increase of the peaking time for higher capacitive loads (see Figure 16) causing longer shaping and improving the noise filtering. Making the comparison between the simulated and the measured noise figures one has to take into account the dispersion of the measured ENC due to

the variation of parameters influencing the analogue performance of the amplifier like spread of the bias currents and beta factors for the input transistors. Taking all those effects into account, one can say that the measured and predicted numbers are in quite good agreement.

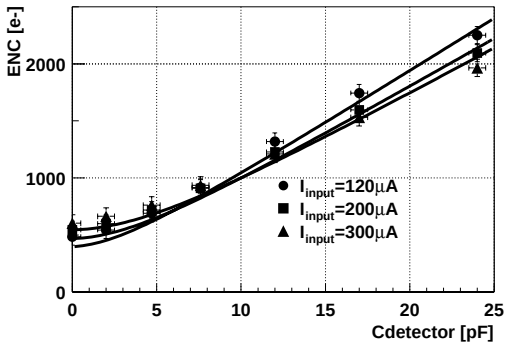

Figure 15: Noise performance of the front-end amplifier for various capacitive loads and bias conditions. Together with the measurement points (markers) the predicted noise figures using model from Chapter 3 supplemented with the correction factors have been drawn (lines).

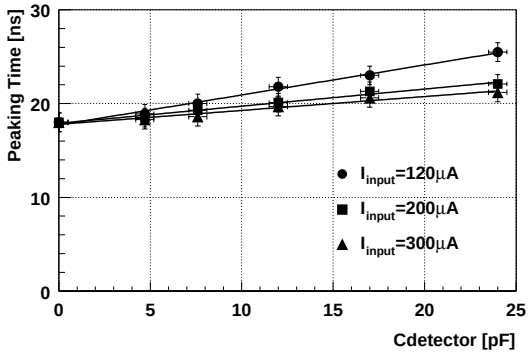

Figure 16: Peaking time of the front-end amplifier as a function of load capacitance and bias current of the input transistor.

Figure 16 shows the dependence of the peaking time of the amplifier-shaper from input capacitive load as a function of bias of the input transistor. Higher degradation of the peaking time for the lowered, below nominal, value of the transistor bias (120μA) agrees with the simulation result of the input impedance characteristic. For the nominal biases and load capacitance of about 20pF the obtained peaking time is very close to 20ns, which is a simulated value for the nominal process parameters.

C. Performance of the analogue memory (ADB).

One of the most important parameters of the analogue memory, which will define its contribution to the overall noise performance of the chip, is the uniformity of the DC offsets (pedestals) between ADB cells.

Figure 17 shows the pedestal map of 128x128 ADB cells in one chip. From the presented figure one can extract the ADB cell-to-cell variation for all channels of the chip. The distribution of the ADB pedestal spreads for all channels in one particular chip is shown in Figure 18. The 1.1mV mean value of the distribution is equivalent to 150e- ENC of extra, non-correlated contribution to the noise generated by the front-end. For a low value of the input current and a low detector capacitance the additional contribution is about 4%. For higher detector capacitance this contribution becomes negligible. One can notice the high channel-to-channel uniformity of the analogue memory confirmed by a narrow (RMS ~ 10%) distribution of the pedestal spreads (Figure 18).

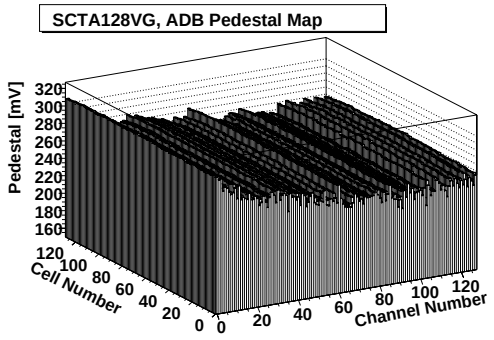

Figure 17: ADB pedestal map in one SCTA128VG chip.

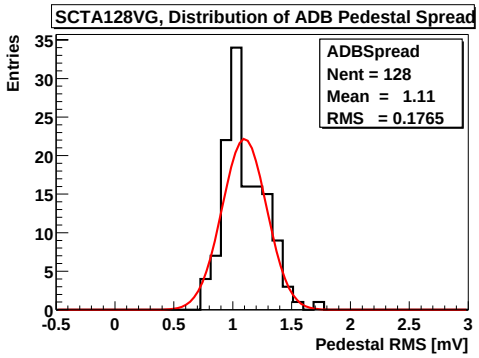

Figure 18: Distribution of ADB pedestal spread in each channel, in one SCTA128VG chip. The 1.1mV mean value of the distribution is equivalent to 150e- ENC.

D. Results of the X-Ray irradiation

Although the SCTA128VG chip is realised in DMILL radiation hard technology the radiation effects in the devices cannot be ignored. The critical issue is the noise in the front-end amplifier. A second order effect is possible degradation of matching which may affect the uniformity of the channels in terms of gain, speed and the ADB performance.

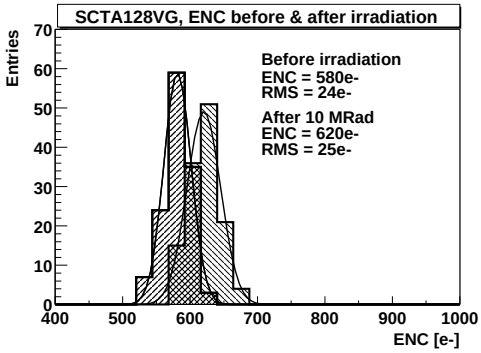

Figure 19: Distribution of ENC before and after 10Mrad. After irradiation the ENC increases by about 6%. The measurements are performed for 200µA input bias current.

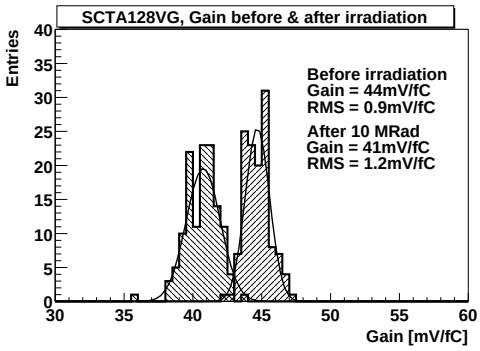

Figure 20: Distribution of channel gains before and after 10Mrad. After irradiation there is a noticeable drop of gain in the order of 7%, and an increase of gain spread from 2 to 3%.

The irradiations have been performed at CERN using a facility providing 10keV energy X-Rays at two dose rates: 8 and 33kRad/min. No annealing has been applied. During the irradiation we have evaluated the analogue parameters such as gain, noise, peaking time, and ADB uniformity as well as power consumption in the analogue and digital parts of the circuit.

Figure 19 shows the distribution of ENC in one SCTA chip before and after irradiation. The increase of parallel noise due to the BJT beta degradation is as expected and could be neglected in the case of a chip working on a detector module when the serial noise due to the capacitive load is dominant. Figure 20 shows the distribution of channel gains in the SCTA128VG chip before and after irradiation. After irradiation one can observe a 7% decrease of gain and an increase of gain spread from 2 to 3%. The evolution of power consumption during the irradiation is shown in Figure 21.

The small (8%) decrease in analogue power consumption is due to the drift of the resistors in the internal band-gap reference and could be compensated by a change of the bias DAC setting. The peaking time and the uniformity of the ADB pedestals were unaffected by the X-Ray irradiation.

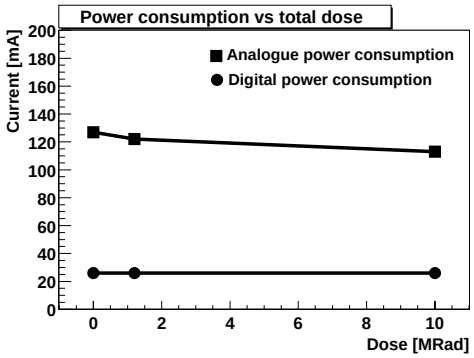

Figure 21: Evolution of analogue and digital power consumption of SCTA128VG chip during the X-Ray irradiation.

Appendix

A. **List of the pads with the coordinates [µm]**

PadName	Xmin [µm]	Ymin [µm]	Xmax [µm]	Ymax [µm]
gndadet!	0.0	0.0	120.0	60.0
i<127>	0.0	120.0	120.0	180.0
i<125>	0.0	240.0	120.0	300.0
i<123>	0.0	360.0	120.0	420.0
i<121>	0.0	480.0	120.0	540.0
i<119>	0.0	600.0	120.0	660.0
i<117>	0.0	720.0	120.0	780.0
i<115>	0.0	840.0	120.0	900.0
i<113>	0.0	960.0	120.0	1020.0
i<111>	0.0	1080.0	120.0	1140.0
i<109>	0.0	1200.0	120.0	1260.0
i<107>	0.0	1320.0	120.0	1380.0
i<105>	0.0	1440.0	120.0	1500.0
i<103>	0.0	1560.0	120.0	1620.0
i<101>	0.0	1680.0	120.0	1740.0
i<99>	0.0	1800.0	120.0	1860.0
i<97>	0.0	1920.0	120.0	1980.0
i<95>	0.0	2040.0	120.0	2100.0
i<93>	0.0	2160.0	120.0	2220.0
i<91>	0.0	2280.0	120.0	2340.0
i<89>	0.0	2400.0	120.0	2460.0
i<87>	0.0	2520.0	120.0	2580.0
i<85>	0.0	2640.0	120.0	2700.0

i<83>	0.0	2760.0	120.0	2820.0
i<81>	0.0	2880.0	120.0	2940.0
i<79>	0.0	3000.0	120.0	3060.0
i<77>	0.0	3120.0	120.0	3180.0
i<75>	0.0	3240.0	120.0	3300.0
i<73>	0.0	3360.0	120.0	3420.0
i<71>	0.0	3480.0	120.0	3540.0
i<69>	0.0	3600.0	120.0	3660.0
i<67>	0.0	3720.0	120.0	3780.0
i<65>	0.0	3840.0	120.0	3900.0
i<63>	0.0	3960.0	120.0	4020.0
i<61>	0.0	4080.0	120.0	4140.0
i<59>	0.0	4200.0	120.0	4260.0
i<57>	0.0	4320.0	120.0	4380.0
i<55>	0.0	4440.0	120.0	4500.0
i<53>	0.0	4560.0	120.0	4620.0
i<51>	0.0	4680.0	120.0	4740.0
i<49>	0.0	4800.0	120.0	4860.0
i<47>	0.0	4920.0	120.0	4980.0
i<45>	0.0	5040.0	120.0	5100.0
i<43>	0.0	5160.0	120.0	5220.0
i<41>	0.0	5280.0	120.0	5340.0
i<39>	0.0	5400.0	120.0	5460.0
i<37>	0.0	5520.0	120.0	5580.0
i<35>	0.0	5640.0	120.0	5700.0
i<33>	0.0	5760.0	120.0	5820.0
i<31>	0.0	5880.0	120.0	5940.0
i<29>	0.0	6000.0	120.0	6060.0
i<27>	0.0	6120.0	120.0	6180.0
i<25>	0.0	6240.0	120.0	6300.0
i<23>	0.0	6360.0	120.0	6420.0
i<21>	0.0	6480.0	120.0	6540.0
i<19>	0.0	6600.0	120.0	6660.0
i<17>	0.0	6720.0	120.0	6780.0
i<15>	0.0	6840.0	120.0	6900.0
i<13>	0.0	6960.0	120.0	7020.0
i<11>	0.0	7080.0	120.0	7140.0
i<9>	0.0	7200.0	120.0	7260.0
i<7>	0.0	7320.0	120.0	7380.0
i<5>	0.0	7440.0	120.0	7500.0
i<3>	0.0	7560.0	120.0	7620.0
i<1>	0.0	7680.0	120.0	7740.0
gndadet!	0.0	7800.0	120.0	7860.0
gndadet!	201.0	60.0	321.0	120.0
i<126>	201.0	180.0	321.0	240.0
i<124>	201.0	300.0	321.0	360.0
i<122>	201.0	420.0	321.0	480.0
i<120>	201.0	540.0	321.0	600.0

i<118>	201.0	660.0	321.0	720.0
i<116>	201.0	780.0	321.0	840.0
i<114>	201.0	900.0	321.0	960.0
i<112>	201.0	1020.0	321.0	1080.0
i<110>	201.0	1140.0	321.0	1200.0
i<108>	201.0	1260.0	321.0	1320.0
i<106>	201.0	1380.0	321.0	1440.0
i<104>	201.0	1500.0	321.0	1560.0
i<102>	201.0	1620.0	321.0	1680.0
i<100>	201.0	1740.0	321.0	1800.0
i<98>	201.0	1860.0	321.0	1920.0
i<96>	201.0	1980.0	321.0	2040.0
i<94>	201.0	2100.0	321.0	2160.0
i<92>	201.0	2220.0	321.0	2280.0
i<90>	201.0	2340.0	321.0	2400.0
i<88>	201.0	2460.0	321.0	2520.0
i<86>	201.0	2580.0	321.0	2640.0
i<84>	201.0	2700.0	321.0	2760.0
i<82>	201.0	2820.0	321.0	2880.0
i<80>	201.0	2940.0	321.0	3000.0
i<78>	201.0	3060.0	321.0	3120.0
i<76>	201.0	3180.0	321.0	3240.0
i<74>	201.0	3300.0	321.0	3360.0
i<72>	201.0	3420.0	321.0	3480.0
i<70>	201.0	3540.0	321.0	3600.0
i<68>	201.0	3660.0	321.0	3720.0
i<66>	201.0	3780.0	321.0	3840.0
i<64>	201.0	3900.0	321.0	3960.0
i<62>	201.0	4020.0	321.0	4080.0
i<60>	201.0	4140.0	321.0	4200.0
i<58>	201.0	4260.0	321.0	4320.0
i<56>	201.0	4380.0	321.0	4440.0
i<54>	201.0	4500.0	321.0	4560.0
i<52>	201.0	4620.0	321.0	4680.0
i<50>	201.0	4740.0	321.0	4800.0
i<48>	201.0	4860.0	321.0	4920.0
i<46>	201.0	4980.0	321.0	5040.0
i<44>	201.0	5100.0	321.0	5160.0
i<42>	201.0	5220.0	321.0	5280.0
i<40>	201.0	5340.0	321.0	5400.0
i<38>	201.0	5460.0	321.0	5520.0
i<36>	201.0	5580.0	321.0	5640.0
i<34>	201.0	5700.0	321.0	5760.0
i<32>	201.0	5820.0	321.0	5880.0
i<30>	201.0	5940.0	321.0	6000.0
i<28>	201.0	6060.0	321.0	6120.0
i<26>	201.0	6180.0	321.0	6240.0
i<24>	201.0	6300.0	321.0	6360.0

i<22>	201.0	6420.0	321.0	6480.0
i<20>	201.0	6540.0	321.0	6600.0
i<18>	201.0	6660.0	321.0	6720.0
i<16>	201.0	6780.0	321.0	6840.0
i<14>	201.0	6900.0	321.0	6960.0
i<12>	201.0	7020.0	321.0	7080.0
i<10>	201.0	7140.0	321.0	7200.0
i<8>	201.0	7260.0	321.0	7320.0
i<6>	201.0	7380.0	321.0	7440.0
i<4>	201.0	7500.0	321.0	7560.0
i<2>	201.0	7620.0	321.0	7680.0
i<0>	201.0	7740.0	321.0	7800.0
gndadet!	491.1	1.2	691.1	141.2
gndadet!	491.1	7717.0	691.1	7857.0
gndac!	791.1	1.2	991.1	141.2
gndac!	791.1	7717.0	991.1	7857.0
vccc!	1091.1	1.2	1291.1	141.2
vccc!	1091.1	7717.0	1291.1	7857.0
vcc!	1391.1	1.2	1591.1	141.2
vcc!	1391.1	7717.0	1591.1	7857.0
gnda!	1691.1	1.2	1891.1	141.2
gnda!	1691.1	7717.0	1891.1	7857.0
a_ring!	1991.1	1.2	2091.1	141.2
a_ring!	1991.1	7717.0	2091.1	7857.0
VREF!	2191.1	1.2	2291.1	141.2
VREF!	2191.1	7717.0	2291.1	7857.0
CBG	2391.1	1.2	2491.1	141.2
test0	2391.1	7717.0	2491.1	7857.0
ICALPROBE	2591.1	1.2	2691.1	141.2
IFOLLPROBE	2791.1	1.2	2891.1	141.2
ISHPROBE	2991.1	1.2	3091.1	141.2
probe_test!	2991.1	7717.0	3091.1	7857.0
IPPROBE	3191.1	1.2	3291.1	141.2
TestEnable	3691.1	1.2	3791.1	131.2
ErrorT	3991.1	1.2	4091.1	131.2
WPTRBT	4291.1	1.2	4391.1	131.2
RPTRBT	4591.1	1.2	4691.1	131.2
ClkRegT<1>	4891.1	1.2	4991.1	131.2
ClkRegT<0>	5191.1	1.2	5291.1	131.2
ResetBT	5491.1	1.2	5591.1	131.2
CommandT	5791.1	1.2	5891.1	131.2
VREF!	6191.1	1.2	6391.1	141.2
VREF!	6191.1	7717.0	6391.1	7857.0
a1_ring!	6491.1	1.2	6691.1	141.2
a1_ring!	6591.1	7717.0	6791.1	7857.0
gnda!	6791.1	1.2	6991.1	141.2
gnda!	6991.1	7717.0	7191.1	7857.0
avdd!	7091.1	1.2	7291.1	141.2

avdd!	7391.1	7717.0	7591.1	7857.0
REFPROBE	7391.3	1.2	7491.3	141.2
CASPROBE	7691.1	1.2	7791.1	141.2
gnda!	7791.1	7717.0	7991.1	7857.0
ReadoutClkT	7991.1	1.2	8091.1	131.2
dvss!	8450.8	33.1	8650.8	133.1
dvdd!	8450.8	333.1	8650.8	433.1
ResetExtB	8450.8	733.1	8650.8	833.1
CommandN	8450.8	1033.1	8650.8	1133.1
CommandP	8450.8	1933.1	8650.8	2033.1
ClockN	8450.8	2233.1	8650.8	2333.1
ClockP	8450.8	3133.1	8650.8	3233.1
singread	8450.8	3533.1	8650.8	3633.1
add1rst	8450.8	3933.1	8650.8	4033.1
ring_dig!	8450.8	4233.1	8650.8	4333.1
probe_test!	8450.8	5733.1	8650.8	5833.1
dvdd!	8450.8	6133.1	8650.8	6233.1
dvss!	8450.8	6433.1	8650.8	6533.1
moutD	8450.8	6833.1	8650.8	6933.1
moutS	8450.8	7133.1	8650.8	7233.1
moutrefD	8450.8	7433.1	8650.8	7533.1
moutrefS	8450.8	7733.1	8650.8	7833.1
MuxTestEnable	8550.8	4733.1	8650.8	4833.1
RBitBT	8550.8	5033.1	8650.8	5133.1
EnableBT	8550.8	5333.1	8650.8	5433.1