Report on measurements of voltage limiter at PP3

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INTRODUCTION

Functionality of voltage limiter at PP3 was measured. Measurements were done with barrel kapton hybrid populated with 12 ABCD3T chips. The hybrid has been irradiated.
Method of measurement: voltages (Vcc or Vdd) were monitored by an oscilloscope at the hybrid while the currents drawn by the hybrid were switched between high and low values. The measurements for analogue voltage are more or less complete. For the digital part few more things need to be checked.

SETUP

Connections:

- hybrid to PPB1: thin (50um Al) LM tape, 3m long
- PPB1 to PP2: 9m of very thin conventional cable
- PP2 to PP3: 25m of thin conventional cable
- PP3 to LV3: a cable with 0.2 Ohm resistance for power lines (both ways) which corresponds to the resistance of minimal length (30m) of thick conventional cables

Capacitors:

Values of the decupling capacitors on PPB1 were 4.7μF for power lines and 1μF for sense lines.

Limiter:

The schematics of the limiter is shown on the figure Fig 1. below. The limiting voltage is set by resistors Re and Rf: Vlim = 2.5V(1+Rf/Re) + 0.65V.
Limiting voltage for Vcc was set to 4.4V using Rf = 33kOhm and Re = 68kOhm.
Limiting voltage for Vdd was set to 5.1V using Rf = 43kOhm and Re = 56kOhm.

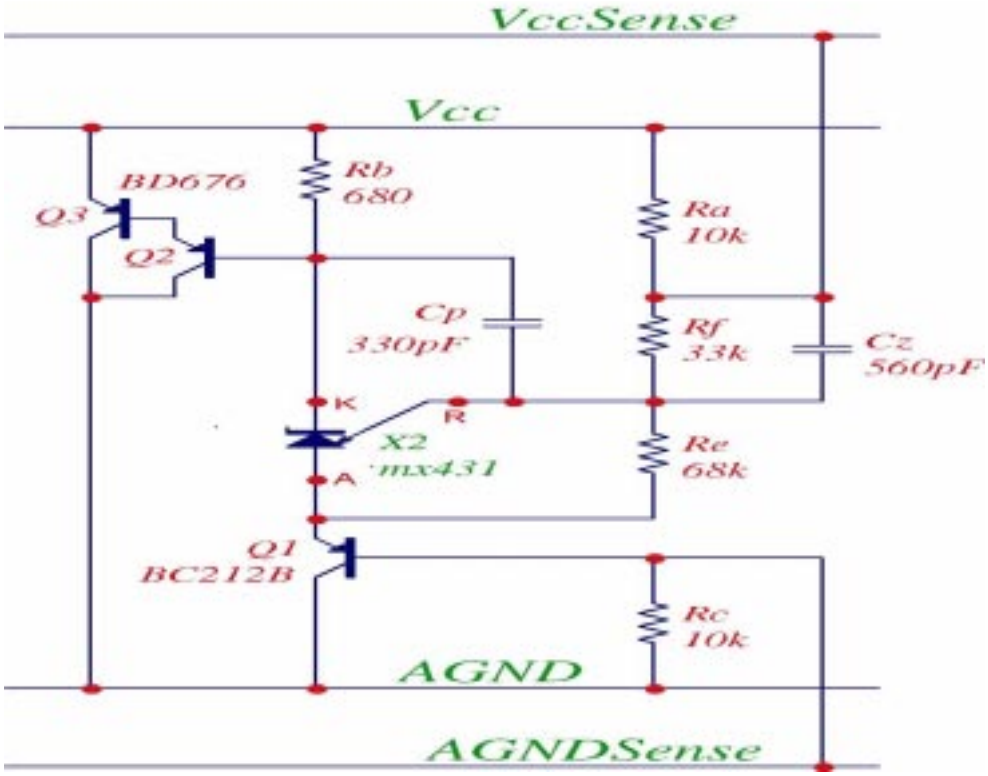

Fig 1. Schematics of the limiter for Vcc. The circuit for the Vdd is the same but with different values of resistors Rf and Re.

MEASUREMENTS:

1. Analogue voltage

Current was switched between high and low values (High ~ 820mA, Low ~ 230mA) by changing the preamp current DAC settings (from all 1 to all 0 at Ishaper set to 30uA). The resistors in the limiter for analogue voltage were chosen so that it switched on if Vcc > 4.4V at the module.
On the figures below the time picture of the Vcc on the module when the current is switched can be seen.

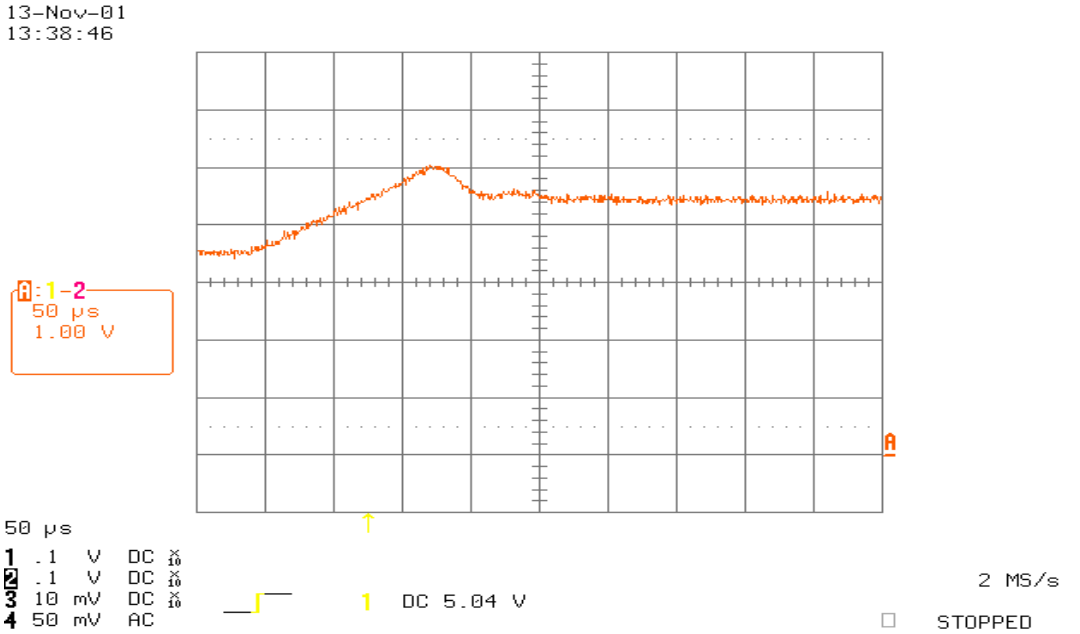

Fig 2. Vcc vs. time

The trace on Fig 2. shows the Vcc on the module. One can see that before the current switch Vcc was 3.5V (0 is at the letter A on the right side of the picture), then we see about 0.5V high, and 50µs long overshoot and then Vcc = 4.4V as defined by the limiter. The same event on the longer time scale is shown in the figure Fig 3 below. Here also the action of LV3, which corrects Vcc to 3.5 V after few milliseconds, can be seen:

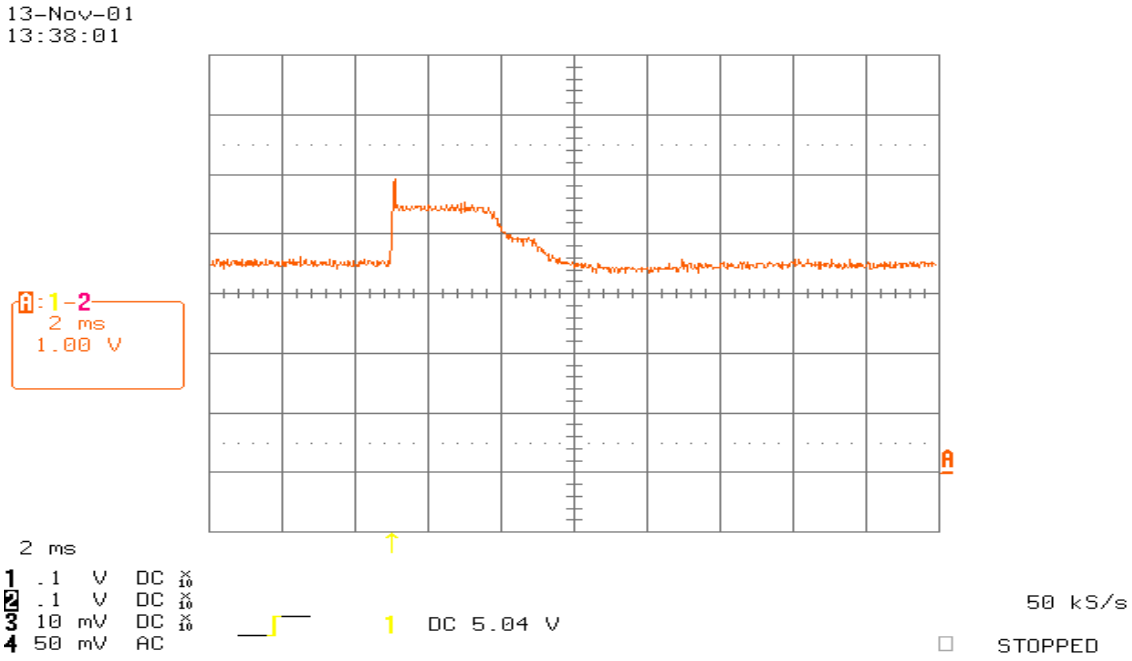

Fig 3. Vcc vs. time

One can compare measurement shown in figure Fig 2. with simulation done by Erik Margan *(*described in his document *Examination Of The Possibility Of Moving The Supply Voltage Limiter To Patch-Panel-3).* The simulated voltages and currents are shown in the figure Fig 4. One can see good agreement between measured and simulated voltage at the hybrid (Det. Module Voltage in the figure)

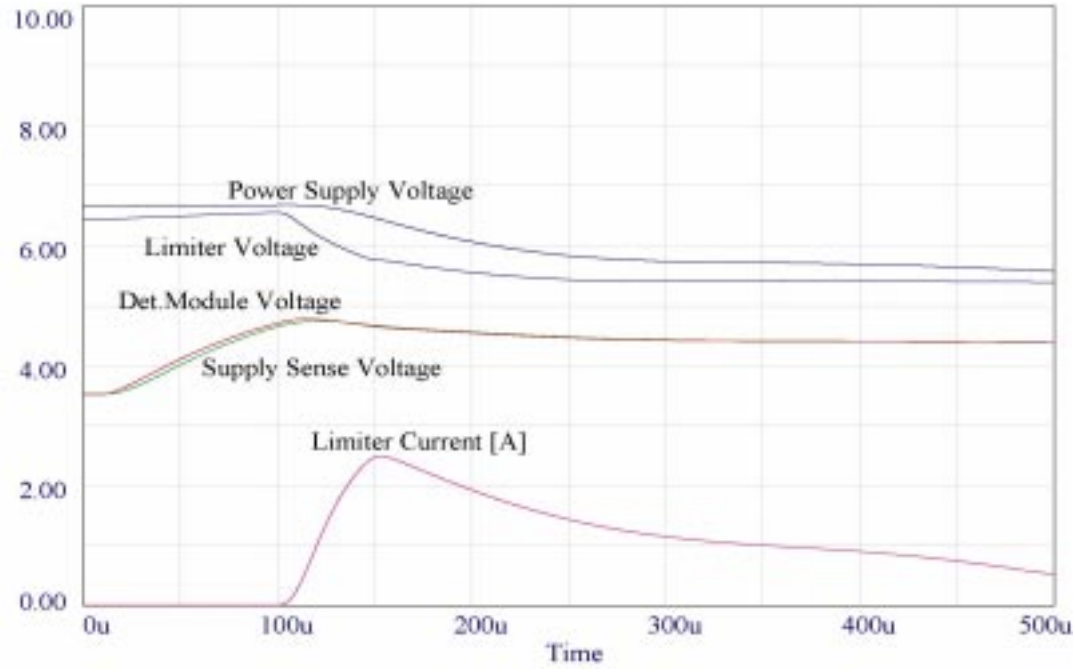

Fig 4. Simulation of voltages and currents when Icc is switched from 820mA to 230mA with time constant as measured. Det. Module Voltage (red line) is Vcc on the hybrid and should be compared with measurement.

2. Digital voltage

Digital current was switched by switching the 40MHz clock on and off.
The resistors at the limiter were Rf = 43kOhm and Re = 56kOhm (see figure Fig 1.) so that the limiting voltage was Vlim ~ 5.1V.
Running the hybrid with Vdd = 4V (Idd = 520mA) and switching the clock off did not increase the voltage on the module above the limiting value (Vlim = 5.1V). The changes of Vdd with time after switching the clock off at operating point Vdd = 4V are shown in figures Fig 5 and Fig 6. To try to set the limiter in action operating point was set to Vdd = 4.5V. These measurements can be seen at Fig 7. and Fig 8. One can see that the maximum Vdd was 5.3V which is 0.2V over the calculated limiting voltage but with the time dependence very similar to that in the figures Fig 5. and Fig 6.
Changing the Vlimit to 4.7V gives similar results, but the maximal Vdd at which the hybrid could be powered on (before the LV3 trips) was 4.4V.

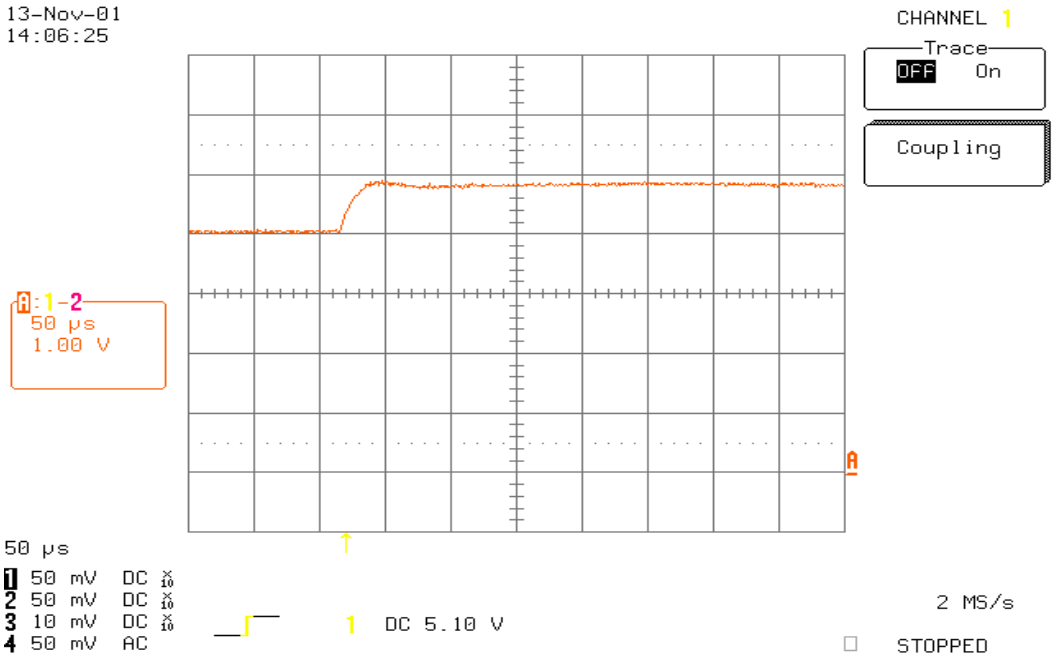

Fig 5. Vdd vs time after clock off, operating point Vdd = 4V

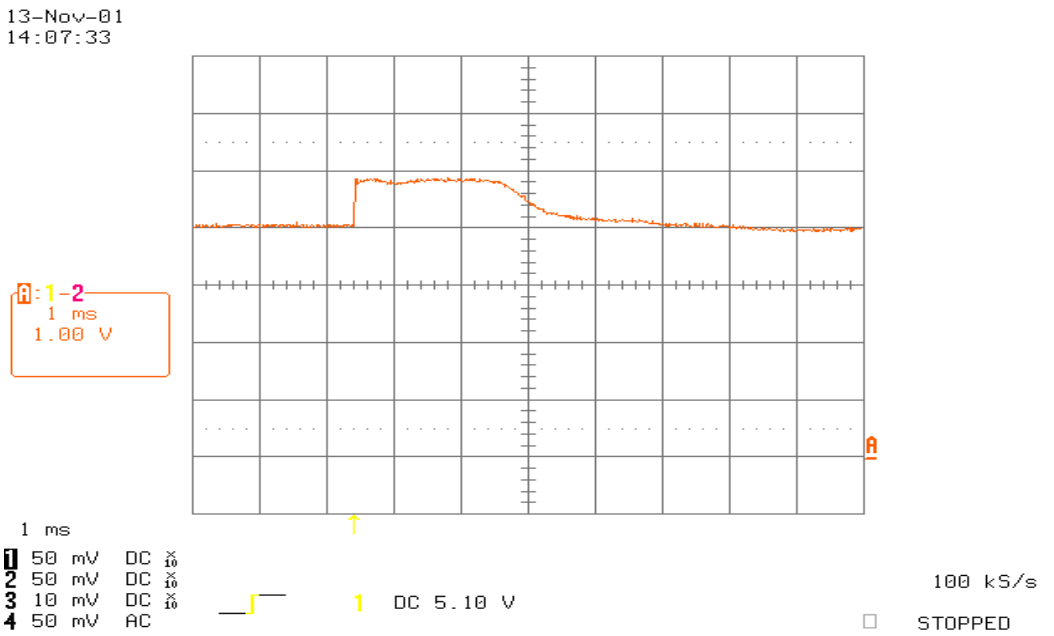

Fig 6. Vdd vs time after clock off, operating point Vdd = 4V, longer time scale.

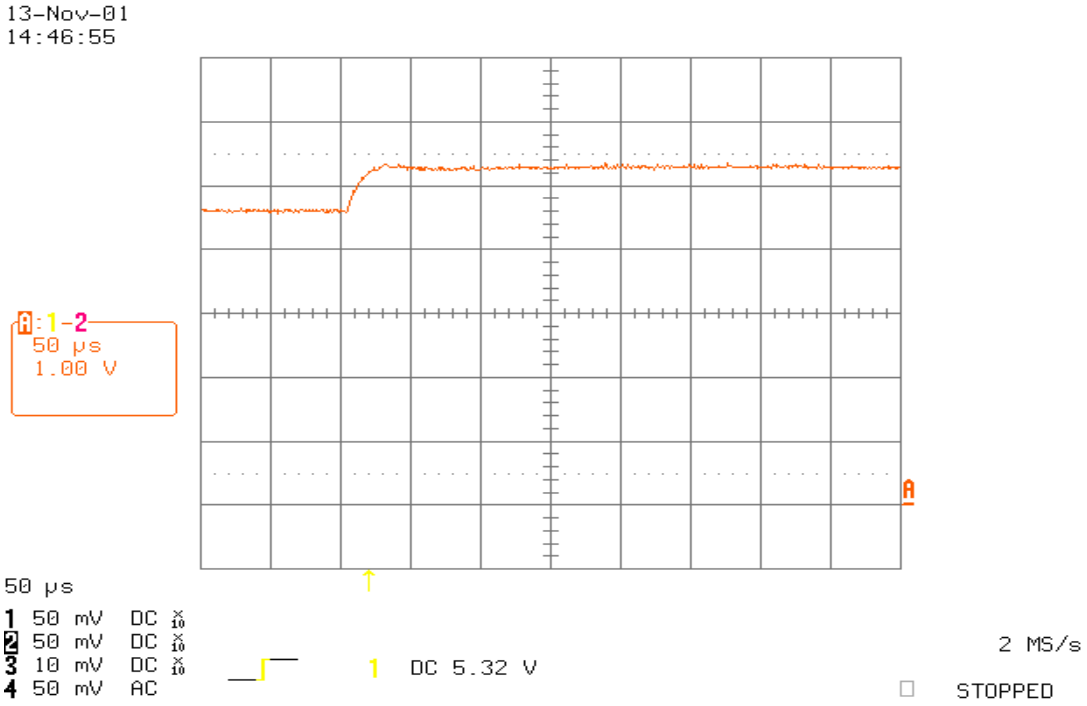

Fig 7. Vdd vs time after clock off, operating point Vdd = 4.5V

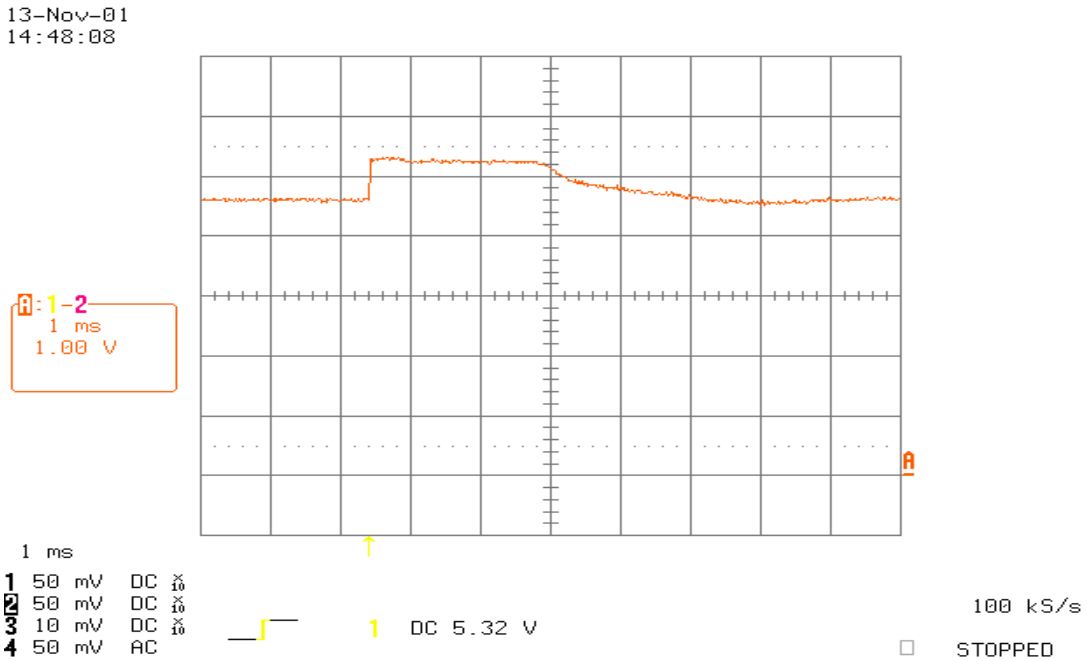

Fig 8. Vdd vs time after clock off, operating point Vdd = 4.5V, longer time scale

Simulation of Vdd limiter action also does not predict a very pronounced overshoot of hybrid voltage when Idd is reduced due to the loss of clock., as can be seen on Fig 9.

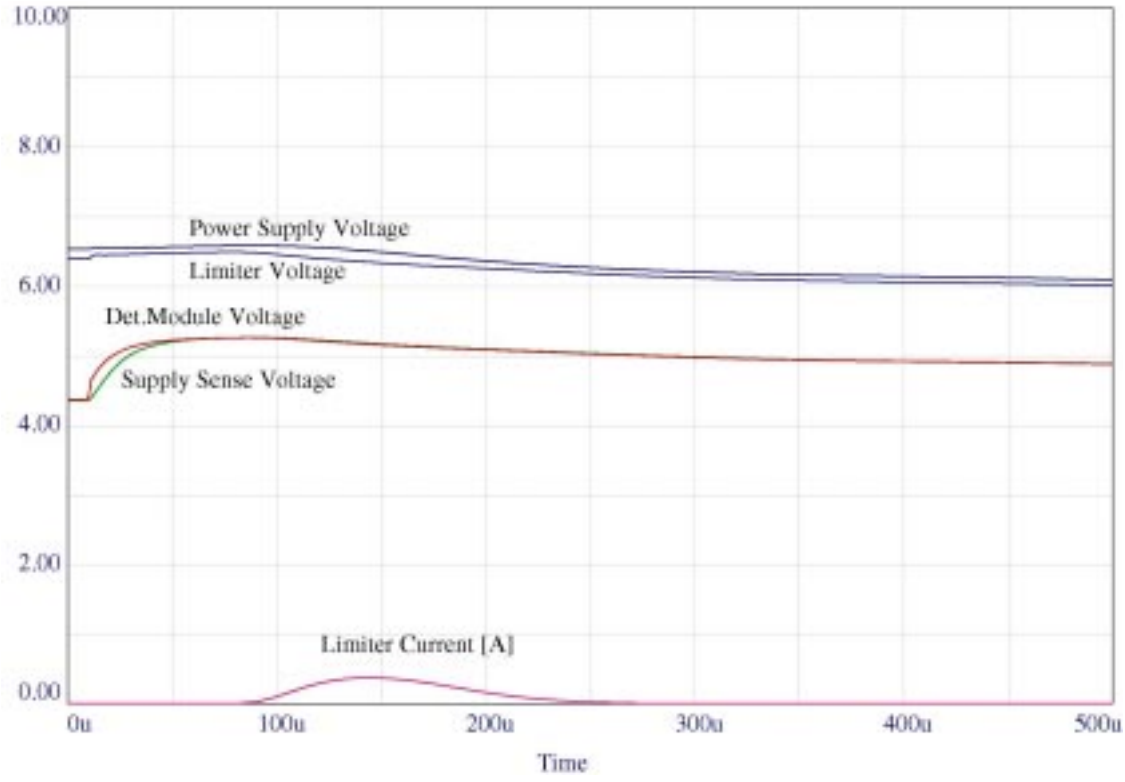

Fig 9. Simulation of switching the current from 750mA to 375mA with limiter set to Vlim = 5.1V. Det. Module Voltage (red line) is the Vdd on the hybrid (compare with Fig 7)

CONCLUSIONS

- reaction times and overshoot values do not change if the limiter is moved from PP2 to PP3 position.
- 0.5V high and 50µs long overshoot on Vcc is acceptable.
- on Vdd 0.2V more than expected form Vlim was has been measured.
- value of Vlim on Vdd lines influences the maximum Vdd at which the hybrid can be operated.
- measurements in good agreement with simulation