NINO, an ultra-fast, low-power, front-end amplifier discriminator for the Time-Of-Flight detector in ALICE experiment

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***Abstract*-- An ultra fast front-end preamplifier-discriminator chip NINO has been developed for use in the ALICE Time-Of-Flight detector. The chip has 8 channels. Each channel is designed with an amplifier with less than 1 ns peaking time, a discriminator with a minimum detection threshold of 10fC and an output stage. The output pulse has minimum time jitter (less than 25ps) on the front edge, and the pulse width is dependent of the input signal charge. Each channel consumes 27mW, and the 8 channels fit in a 2x4mm^2 ASIC processed in IBM 0.25μm CMOS technology.**

I. Introduction

The Time-Of-Flight detector is the major system for performing particle identification (PID) in the ALICE experiment. It has large azimuthal angle (+/-45^o) and full radial coverage. The detector is a cylinder of 3.7m radius located around the TPC chamber. It is made of 10 gap double stack Multigap Resistive Plate Chambers (MRPC) [1][2]. Each stack has 5 gaps of 250 μm. The total number of detector channels is 160.000. The RPC is chosen because of the very fast charge collection time (~100ps). Particle identification is made by measuring the Time-Of-Flight of the high-energy incident particles with a resolution better than 100ps. This allows particle separation between e, π, K, and p in the momentum range 1 to 4 GeV/c.

II. Requirements and Circuit Description

The very precise measurement of time, below 100ps range at the system level, requires a very fast, minimum slew rate, front-end amplifier discriminator. To minimize signal reflection and crosstalk, the input impedance has to be low and matched to the impedance of the transmission line connecting detector to front-end.

The front-end channel specifications are given in Table 1. The input stage is a very critical low noise large bandwidth circuit. We have chosen a robust current-to-voltage converter based on a balanced common gate circuit configuration. The subsequent signal amplification is performed with four identical cascaded amplifiers, which are optimized for delay and slew rate. They provide sufficient gain to operate as a discriminator. The threshold is set by a voltage difference applied on two symmetrical inputs, acting on a DC stabilization feedback circuit, which is used also as the common mode rejection circuit. A positive loop feedback circuit can be enabled to add a small hysteresis on the discriminator threshold.

TABLE I
NINO CHIP SPECIFICATIONS

Parameter	Value
Peaking time	1ns
Signal range	100fC-2pC
Noise (with detector)	< 5000 e- rms
Front edge time jitter	< 25ps rms
Power consumption	30 mW/ch
Discriminator threshold	10fC to 100fC
Differential Input impedance	40Ω< Zin < 75Ω
Output interface	LVDS

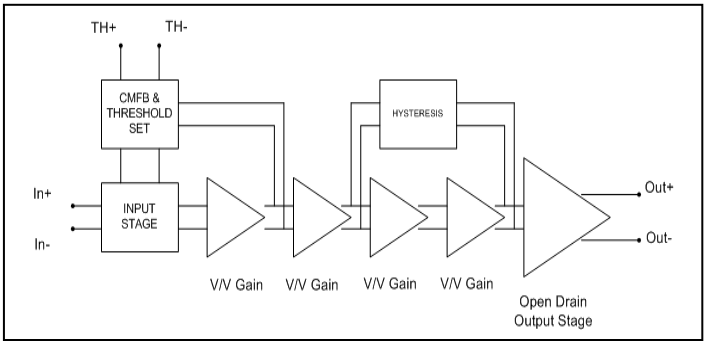

Fig. 1. Functional block diagram for one channel of the NINO chip.

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The full channel configuration is depicted in Fig. 1. From inputs to outputs a fully differential circuit is chosen to obtain a large immunity against power supply noise and ground noise.

The output stage is an open-drain differential circuit providing current switching between the two outputs of a channel. Output levels can be made compatible with commercial LVDS receivers.

A. The Input Stage

Detector signal is applied across the two inputs of a common gate differential circuit (Fig. 2).

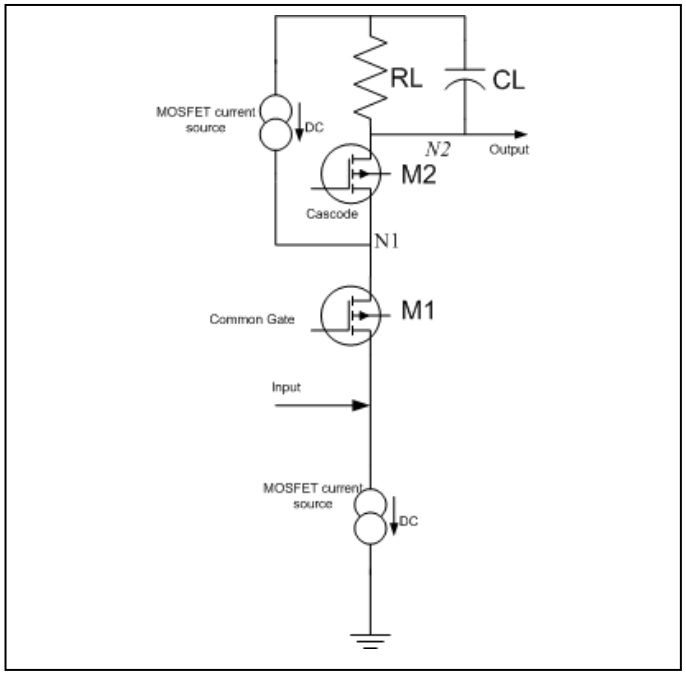

Fig. 2. Simplified schema of the input stage (one side of the differential structure)

The input impedance on each branch of the differential circuit is thus *1/gmsb* of the input transistor M1 (Fig. 2). The input charge, generated by the detector, is flowing through transistor M1 and the branch made of transistor M2 and load elements R_L and C_L. The output signal is the voltage on the output node *N2*. The structure is suited to high speed, because of the absence of feedback element acting on the signal. The frequency bandwidth is then determined by the time constant $R_L.C_L$ at node N2 and by the poles at input node and node *N1*. Typical values of time constants of the input stage are given in Table 2.

TABLE II
INPUT STAGE TIME CONSTANTS

Node	Elements	Time constant
OUTPUT	R_L, C_L	760ps
N1	Local cap, cascode	155ps
INPUT	Input Cap, 1/gmsb	550ps

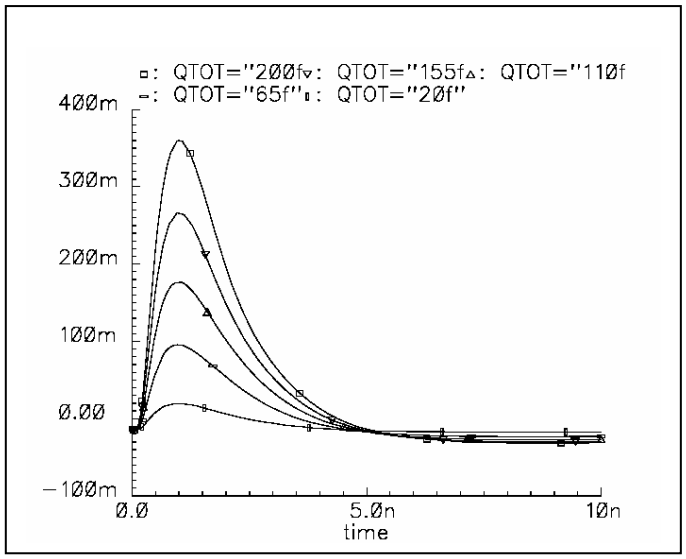

Fig. 3. Differential voltage signal at the first stage outputs, for input charge values from 20fC to 200fC. Peaking time is 1ns, gain 1.8mV/fC.

The typical signal on output of the first stage is shown in Fig. 3. The detector signal is modeled as a 200ps width current pulse. The circuit modeling for SPICE simulation includes the electrical model of the transmission line between detector and front-end.

B. The biasing circuit

A common biasing block (not shown on Fig. 1) is used to provide biasing currents and voltages to the channels in the NINO chip.

A dedicated circuit has been developed to match the channel input impedance, to an external resistance used as a reference. The matching circuit is presented on Fig. 4.

The two branches, which are biased with identical currents Io, have differences in topology: the ratio W1/W2 of transistors M1 and M2, and the resistance Rp which is inserted at the source of M1. The asymmetry results in the following expression for current Io:

$$I_0 = \frac{1}{Kn.\frac{W2}{L}}.\frac{1}{Rp^2}.(1-\frac{1}{M}) \qquad M = \sqrt{\frac{W1}{W2}}$$

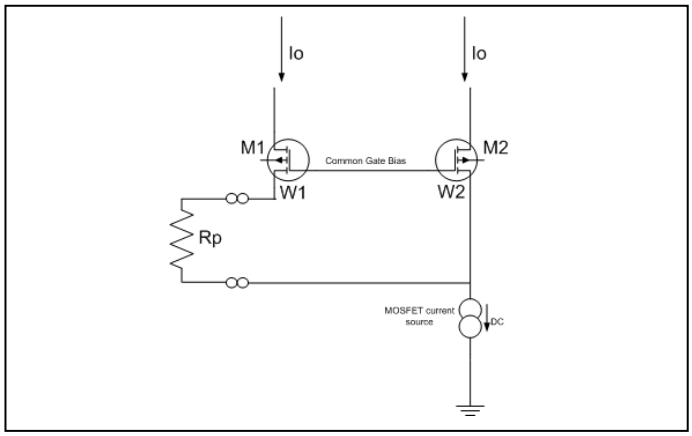

Fig. 4. Simplified schema of the biasing circuit for the input stage.

If W1/W2=4, the source impedance of the transistor M2 is expressed as:

$$1/gmsb_{M2} = \frac{1}{2\sqrt{Kn.\frac{W2}{L}.I_0}} = Rp$$

The above equations are established for circuit operating in strong inversion whereas transistors M1 and M2 are operating in moderate inversion. SPICE simulation was used to refine the ratio W1/W2.

The two input devices of the differential input stage are biased as the transistor M2 (same gate voltage and drain current). Thus impedance of the input devices is matched to the value of the reference resistance Rp.

C. Cascaded voltage gain stage

Voltage gain amplification after the input stage is provided with four cascaded identical high bandwidth differential pair amplifiers. Each amplifier has a voltage gain of 6, with –3dB bandwidth above 500MHz.

III. RESULTS

A. Simulation Outputs

The time response and the pulse width as function of the input charge, obtained from the SPICE simulation, are shown in Fig. 5.

The pulse width measurement will be used in the experiment, to estimate the input charge and correct for time walk. The pulse width is increasing as the result of the increasing saturation of the cascaded amplifiers.

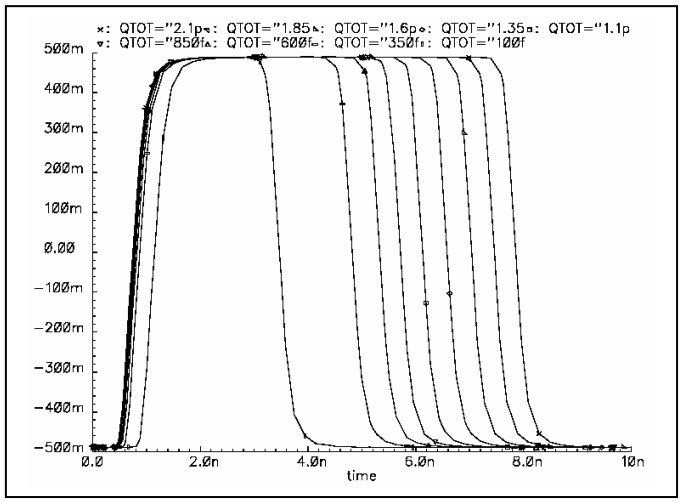

Fig. 5. SPICE simulation of the differential output signal. The input charge is swept from 100fC to 2.1pC. Threshold is set at 50fC.

B. Noise performance

Noise performance has been estimated using the noise analysis tool available with the SPICE simulator. With the detector capacitance of 10pF at the inputs, the channel differential gain is measured as 1070mV/fC. The integrated noise at the differential outputs is 570mV rms. The calculated noise referred to the inputs is then calculated as 3320 electrons rms (0.53fC). With a mean signal from the detector above 50fC, the signal-to-noise ratio (SNR) is sufficiently large to make the channel noise not critical. The circuit can operate with a threshold as low as 10fC.

The above estimates from the simulator can be compared to calculations obtained from the simplified formulations for series and parallel noises in case of detector amplifiers [3]. The dominant contribution to the series noise comes from the input device (M1 in Fig. 2). This contribution is calculated as:

$$ENC_s^2 = 4kT.\frac{2}{3}.\Gamma gm_{sb}^{-1}.\tau^{-1}.C_{\det}^2$$

where gm_{sb} is the input device transconductance, Γ the noise factor, τ the channel shaping time. With the following values for parameters:

gm_{sb}=37mS, Γ=1.5, C_{det}=10pF, τ=1ns

the value obtained for series noise is 1300 electrons (for one branch of the differential amplifier).

The parallel noise contribution comes mainly from the current source connected at the input node:

$$ENC_p^2 = 4kT.\frac{2}{3}.\Gamma gm_p.\tau$$

where gm_p is the transconductance of the MOS current source at the input node. With the following values for parameters:

gm_p=4.4mS, Γ=1.5, τ=1ns

the value obtained for parallel noise is 1660 electrons (one branch of the differential amplifier).

Summing the series and parallel contribution, and summing for both branches of the differential circuit, the total noise referred at the inputs is then 3000 electrons rms. The simulation shows a 10% higher value. The difference can be attributed to the noise contributions of other circuit components and/or to the error in the estimation of the Γ or τ parameters.

C. Experimental Results

The 2x4mm^2 NINO chip has been fabricated using a commercial 0.25 microns process (Fig. 6).

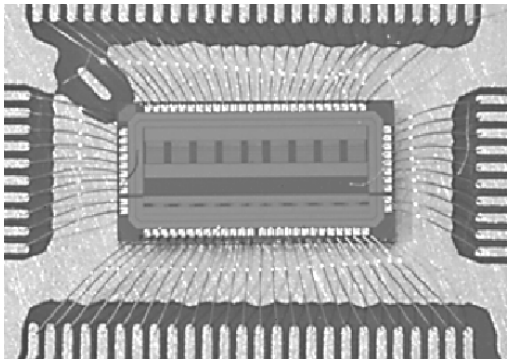

Fig. 6: The NINO chip mounted on test beam experiment PCB. Chip size is 2x4 mm^2

The chip contains 8 channels and the biasing circuit. The external biasing components are one resistor (Rp) which defines the input impedance and one resistor to define the output current. Four channels are built as described in section II, four other channels have an additional circuit which introduces an small hysteresis in the comparator stage.

The ENC noise has been measured with input capacitors from 2 to 8pF (Fig 7).

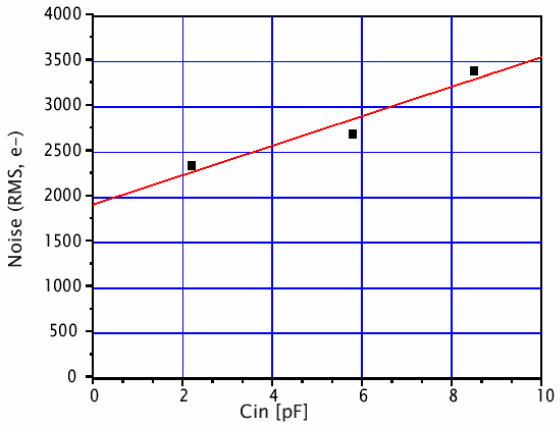

Fig.7: The NINO chip input noise measurement.

The measured noise figure indicates parallel and serie noise values of 1900el. rms and 165el. rms/pF. For the nominal capacitance of the TOF detector (10pF), the noise level is 3550 el. rms (0.57fC). The minimum threshold at which the circuit was able to operate, with no particular protection against ringing, is 10fC. For the experiment, the minimum threshold will be set at 50fC, a factor 87 above the noise floor. The detector mean signal range is 0.5-0.8pC.

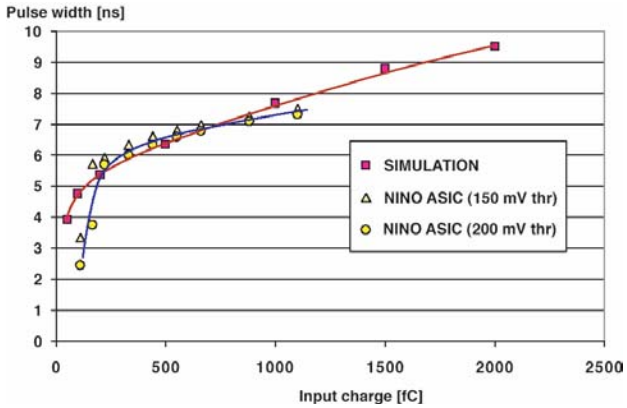

Fig. 8. Measurement of the pulse width for two threshold settings, and comparison with the simulation data.

The pulse widths obtained from measurements for two thresholds have been compared with the width obtained from simulation data (Fig. 8). The measured and simulated widths are well matched up to 1pC. Above this value, the measured signal width is smaller than the width predicted by SPICE simulation. The pulse width is increasing through the successive saturation of the amplifier stages. The difference in pulse width with large signal may be due to a simulation imperfection.

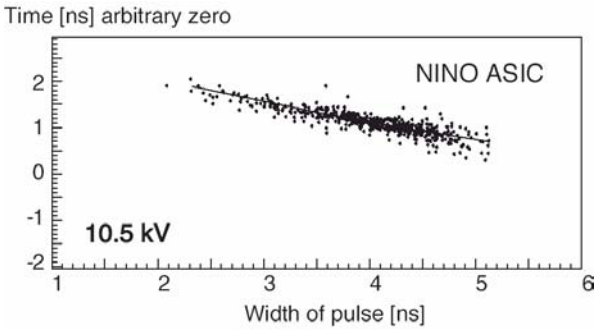

Fig. 9. Measurement of front edge time walk (arbitrary position "0" on vertical scale) versus pulse width for an input charge of 50 to 100fC, threshold set at 30fC.

The correlation of pulse width with the front edge time walk is linear, as shown on Fig. 9. The pulse width measurement can thus be used to correct for the time drift of the front edge due to the discriminator time walk.

The jitter of the front edge of the signal, which determines the time measurement accuracy has been measured on test bench and found to be 20ps rms (Fig. 10).

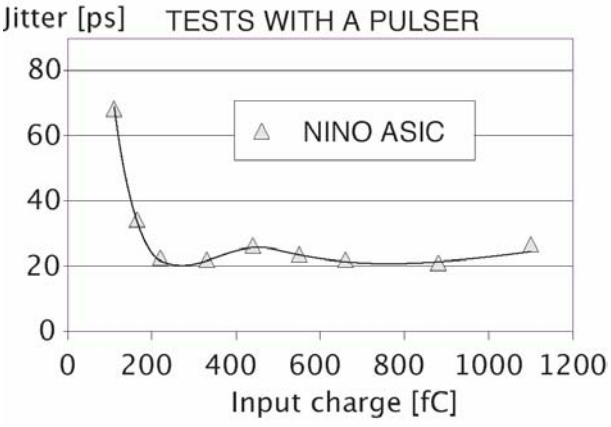

Fig. 10. Measurement of time jitter on the front edge The input charge is swept from 50fC to 1.15pC with a threshold set at 30fC.

The time jitter of a complete setup with detector and readout electronics has been measured with a test beam (Fig. 11).

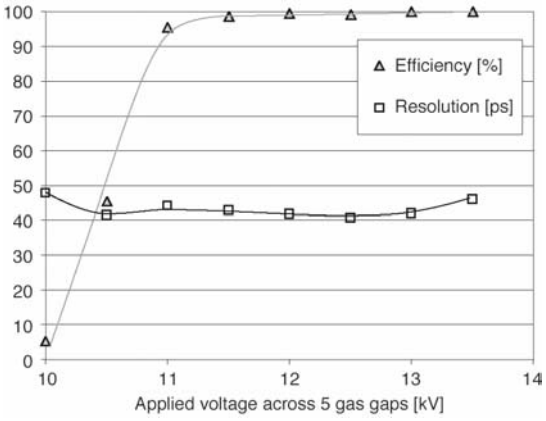

Fig. 11. Measurement of time jitter and detector efficiency, with test beam, MRPC detector and precision TDC unit.

The detector efficiency was measured above 99.9% for the MRPC detector biased with high voltage above 12kV. The system jitter was 41ps rms. The individual contributions to the system jitter were separately evaluated: 14.4ps for the beam spot, 25ps for the MRPC detector, 21.2ps for the time measurement circuit (HPTDC). and 20ps for the NINO channel, a value identical to the one obtained with the test bench measurements (Fig. 10).

IV. Conclusion

The NINO amplifier and discriminator chip has been developed for the precision time measurement required for the Time-Of-Flight detector in ALICE experiment. The present chip has 8 channels with a peaking time of 1ns with a resolution of 20ps rms. The pulse width measurement is used to do charge measurement as well as time walk correction. The threshold can be set at 10fC input charge. The power consumption per channel is 27mW, including the LVDS compatible output driver. Only one power supply and two external resistors are needed to make the circuit operational.

V. References

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[3] V. Radeka, “Low-Noise Techniques in Detectors”, Ann. Rev. Part. Sci. (1988) 38: 217-77.