PP1 PCB Test Methods, Specifications And Limits

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1) Connectivity and Capacitance Test

a) connection from the connector to the capacitance (no resistance measured)

b) short or R up to 2 MΩ between any two lines or ground

c) capcitance value test, from 10 pF to approx. 20 μF, resolution 10 pF, absolute error < 1 %.

The test sequentially activates each line and checks all other lines for possible error.
For details, see the block circuit diagram in Fig.1.

2) High-Voltage Test

a) sustained 500 Vdc test for $\sim$ 30 s on the HV-Bias line (risetime 0.5 s)

b) leakage current from HV-Bias to HV-return, $C = 15$nF at 500 V, $Z_{\text{in}} = 1\,\text{M}\Omega$, $V_{\text{in max}} = 10$ V, I_{lk} max $= 10\,\mu$A, resolution 0.3 nA.

c) leakage current from HV-Bias to Ground at 500 V, I_{lk} max $= 10\,\mu$A, resolution 0.3 nA (Z_{in} is virtual ground, amplifier $V_{\text{ofs}} < 100\,\mu$V, $I_{\text{in}} < 25$ pA).

Other lines are protected by the PCB design layout and are not tested for leakage.
For details, see the block circuit diagram in Fig.2.

3) Trace Resistance Test

4-point Kelvin resistance measurement from the connector to the LM-Tape solder pads ; each line is sequentially activated by 100 mA and the voltage drop is measured by a 2 V range, 100 μV resolution ADC, resulting in a 20 Ω range and 1 mΩ resolution, with absolute error < 0.5 %.

For details, see the block circuit diagram in Fig.3.

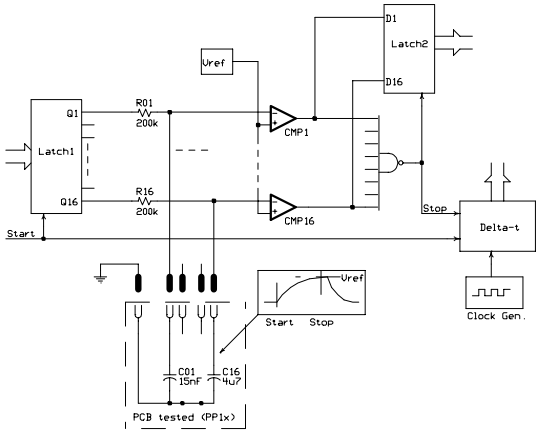

Fig.1 : Capacitance test

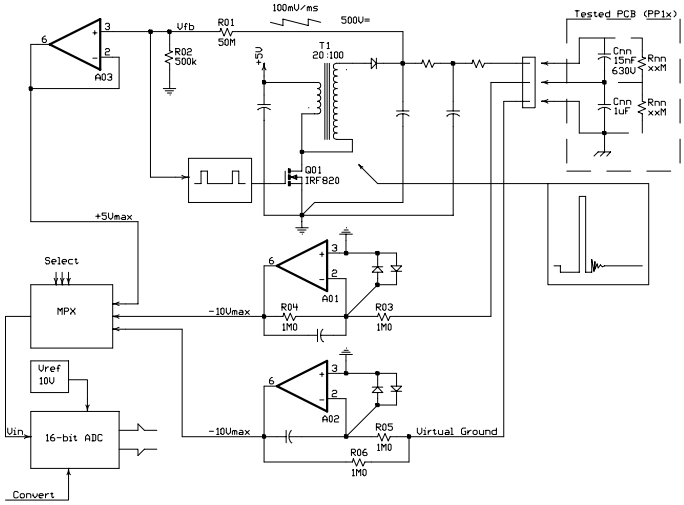

Fig.2 : High-Voltage test

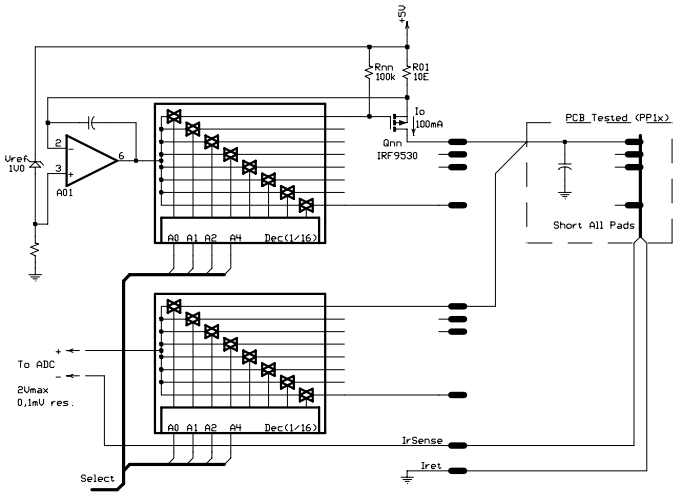

Fig.3 : Line Resistance test