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LHC-Atlas Cable Tester

Description of Drive and Sensing Channels and Expected Values

1) CTB1 (Cable Test Board 1) Circuit Diagram

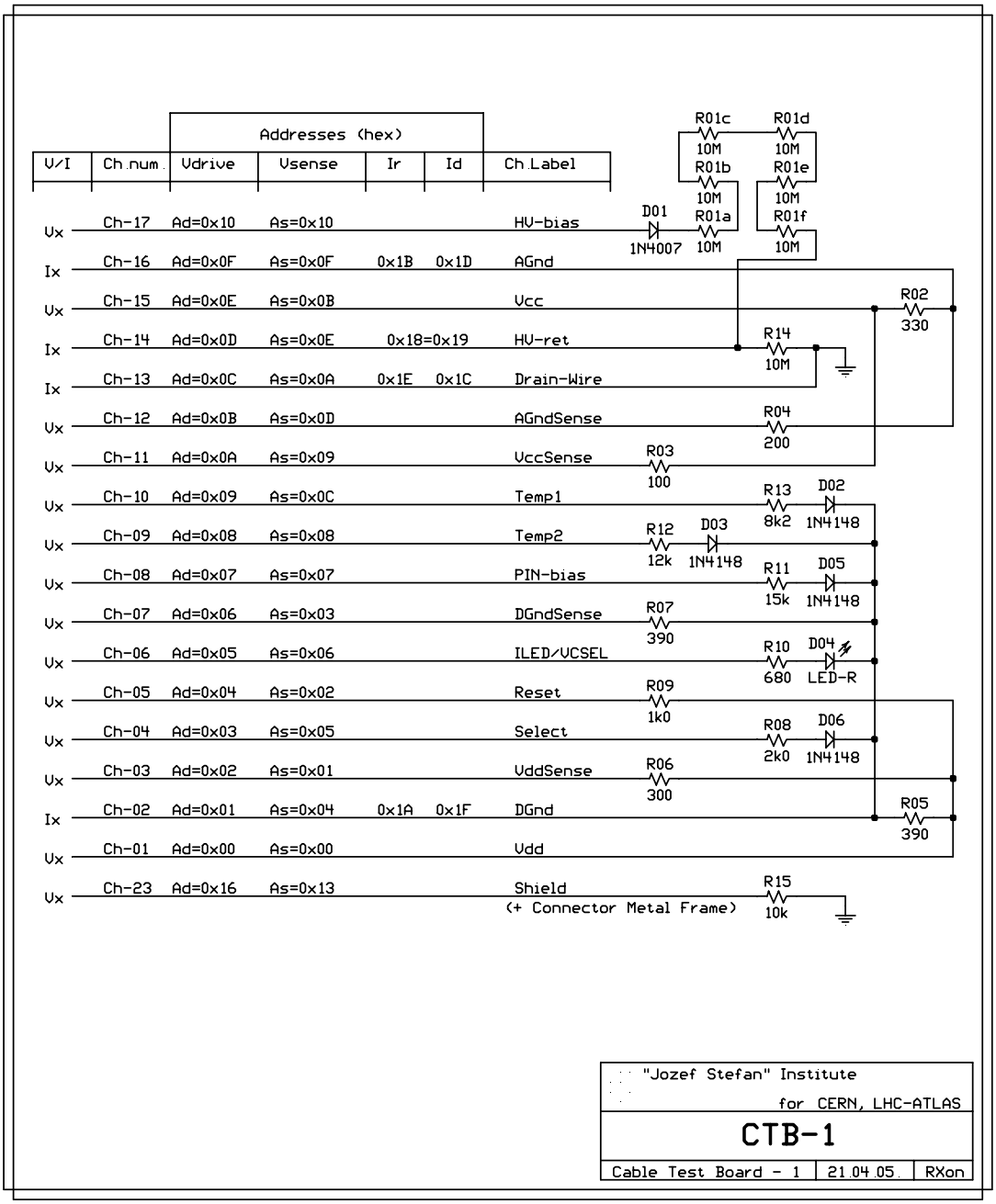

Fig.1: DummyPP1 test board. **Changes for the cable test version: a)** the HVbias resistor is increased to 60MΩ in order to preserve the same range of the leakage current amplifiers on HVret, Drain-Wire/Shield, AGND and DGND; **b)** the Reset is connected to Vdd by a 1 kΩ resistor, the diode in series has been eliminated; **c)** the diode in the ILED/VCSEL line is replaced by the LED; **d)** the Drain-Wire and the Shield are connected by a 10 kΩ resistor; **e)** there are no capacitors.

2) Measurement Principle For the Identification Procedure

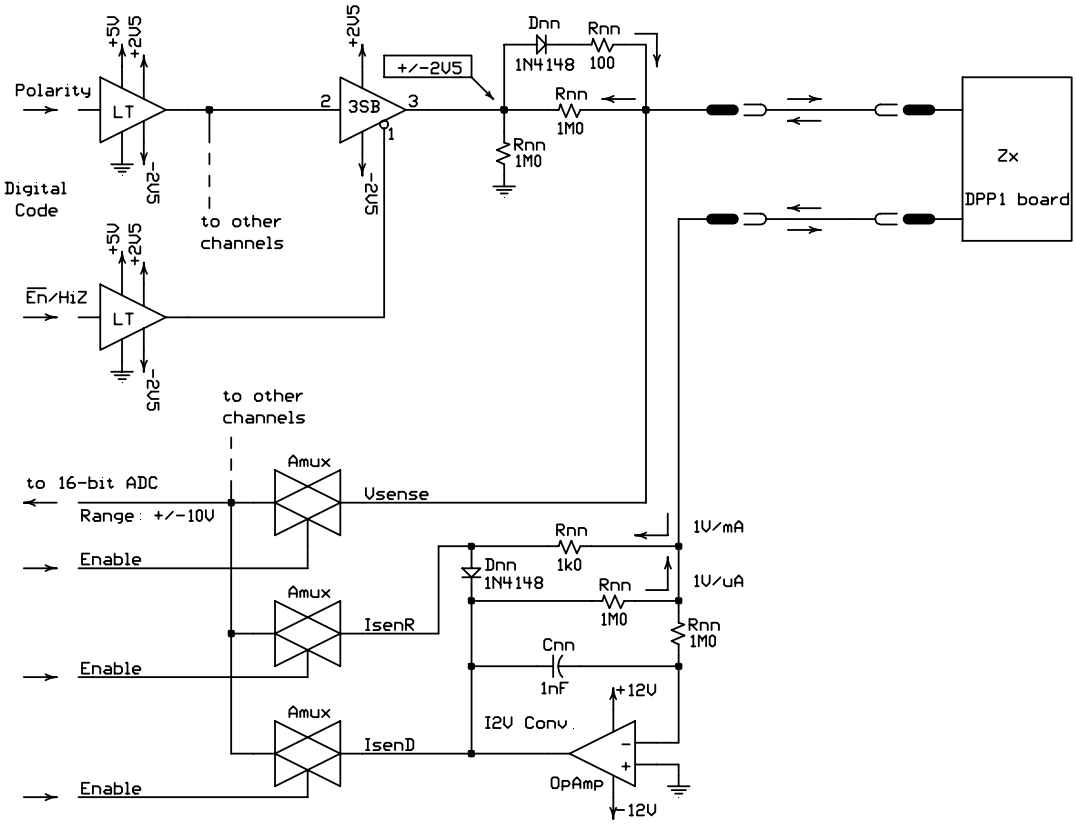

Fig.2: The identification procedure: each cable line is driven by a +2.5 V through a forward biased diode and a 100 Ω resistor and by a −2.5 V through a 1 MΩ resistor. In the high impedance mode each line is referenced to ground by a 2 MΩ resistor. The HVret line is current-sensed (zero input impedance) and the current range is set by the 1 MΩ resistor in the I-V converter amplifier. Because the ADC voltage range is ±10 V, the maximum input current is 10 µA, with the resolution of ≈ 1 nA, limited by the amplifier input offset voltage (1 mV). The AGND, DGND and Drain-Wire lines have the same sensitivity for negative input currents; for positive input currents the sensitivity is reduced to 1 mA/V by a 1 kΩ resistor in series with a diode, which can be used to compensate for the voltage drop of the driving circuit in the forward bias mode, in which the range is 10 mA and the resolution ≈ 1 µA. All other lines are voltage-sensed. The sensed voltages and currents are used to determine the resistances at the end of the cable and, in addition, any faulty impedance between any two lines. The limits of detection depend on the resisrances on the CTB1 at the end of the cable. As a general rule, a parallel resistance 100× greater that the loading resistance can be dtected.
The lines which have a diode in series with the loading resistor can be evaluated to a much greater precision in the reverse bias mode; the same is true for the lines which are not in contact. Between the AGND, DGND and Drain-Wire/Shield the sensitivity is lowest (the detection range is of the order of a few kΩ), because of the low input impedance of their current amplifiers. The tri-state buffer dirvers and the voltage multiplexers in ther off state leak typically less than 50 pA, thus their influence on the measurement is minimal.

3) Self-Calibration

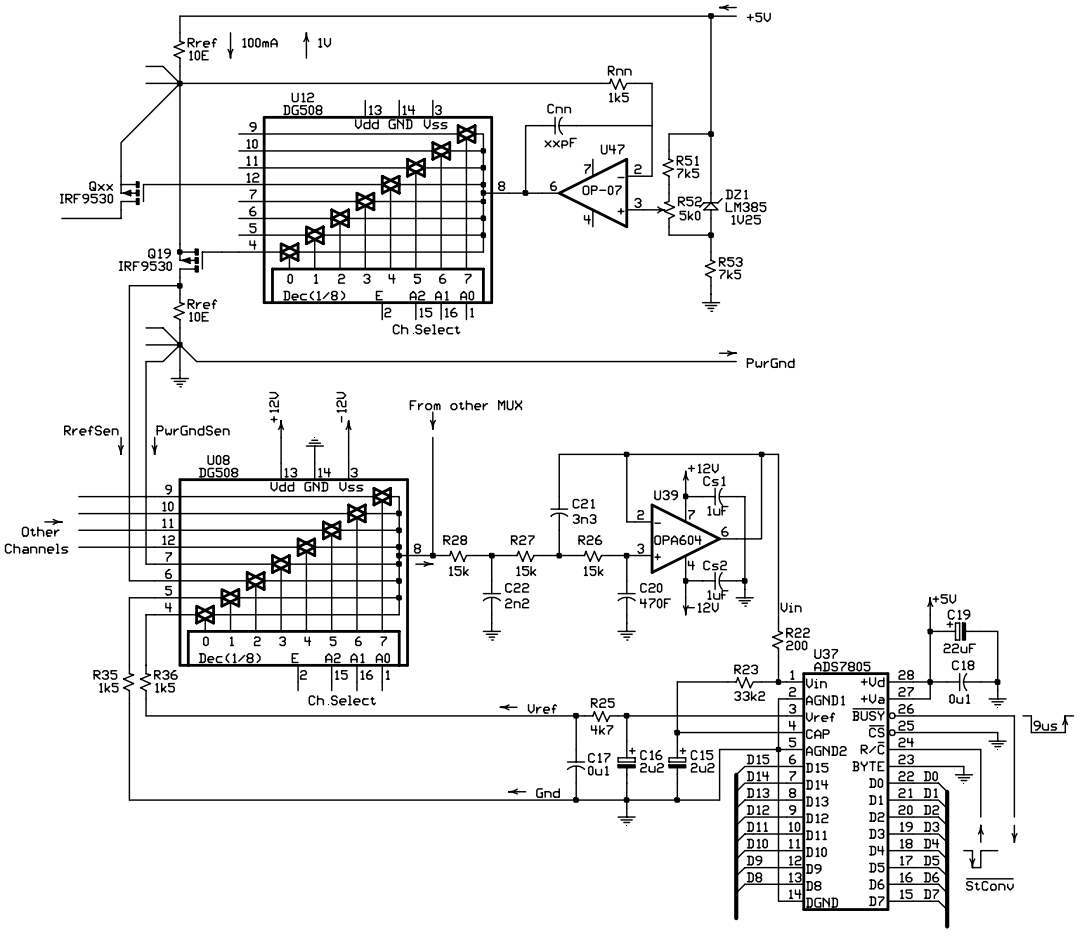

Fig. 3: The Test Box circuit includes the possibility of self-calibration, thus reducing the long-term variation of parameters. Four multiplexer channels are dedicated to this task. First the ADC's own ground level and voltage reference are measured in order to compensate for the offset and gain errors throughout the measurement chain (multiplexer, filter amplifier, ADC). For the cable resistance measurement, the current source calibration is performed by measuring the power ground level (at the point where all power currents return) and then the current is measured in form of a voltage drop on a precision 10 Ω resistor. The current is adjusted by the R52 trimpot in parallel with the LM385 1.23V reference so that there is a 1.000V drop on the upper 10 Ω resistor Rref, resulting in a 100mA output current from each drain of the P-channel MOSFET (whichever is switched on into the opamp OP-07 feedback lopp). The resulting gain and offset are used to correct the actual measuremnets. The self-calibration is executed automatically before starting a measurement. If necessary, it can be repeated upon a user request.

4) Accuracy and resolution

The 16-bit ADC has a measuring analog voltage range of ±10 V, therefore the measurement resolution is ≈ 0.3 mV (or $20/2^{16}$). The voltage offset (zero level) accuracy is under 1 mV and a similar input offset is present at the opamp, however both can be accounted for by the self-calibration procedure. For the current measurement the current-to-voltage conversion opamp has an additional 1 mV input offset, resulting in a 1 nA current offset in the reverse-bias mode and a 1 μA in the

forward-bias mode. For the HV leakage current test the current measurement precision is also limited to the 1 nA level because of the opamp input offset voltage; however, the precision of the calculated insulation resistance is impaired by the actual HV level which varies considerably as a function of the load resistantce (550 V on 1 GΩ and about 525 V on 60 MΩ), because of the "soft" regulation and a 100 kΩ series output protection resistance of the HV source.

5) Expected Results For Each Channel

Ch.01: Vdd
Forward bias mode:
Vdrive +2V5, drive address Ad=0x00 (hex), ORed with polarity bit 0x80.
Vsense address As=0x00, expected ≈ +1.5V.
Ch.03 (VddSense, address 0x01), expected ≈ +1.5V
Ch.05 (Reset, address 0x02), expected ≈ +1.2V
Curent sense I(DGND), Ch.27 address 0x1A; expected ≈ –3.88V (I=3.88mA).
No diode compensation required.
All other channels should be close to zero.

Reverse bias mode:
Vdrive –2V5, drive address Ad=0x00 (hex).
Vsense (address As=0x00), expected ≈ –1mV. Same on VddSense.
Curent sense I(DGND), Ch.32) address 0x1F; expected ≈ +2.5V (I=2.5µA).

Measurement resolution: 30kΩ equivalent resistance in parallel to Vdd-AGND and over 20MΩ between Vdd and some other lines.

Ch.02: DGND
Forward bias mode:
Vdrive +2V5, drive address Ad=0x01 (hex), ORed with polarity bit 0x80.
Vsense address As=0x04, expected ≈ 0V (current input has very low Zin).
Curent sense I(DGND), Ch.27, address 0x1A; expected ≈ –1.9V (I=1.9mA).
No diode compensation required.
All other channels should be close to zero.

Reverse bias mode:
Vdrive –2V5, drive address Ad=0x01 (hex).
Vsense (address As=0x04), expected ≈ 0V.
Curent sense I(DGND), Ch.32, address 0x1F; expected ≈ +2.5V (I=2.5µA).

Measurement resolution: very poor. This is used for I-to-V calibration only.

Ch.03 VddSense
Forward bias mode:
Vdrive +2V5, address Ad=0x02 (hex), ORed with polarity bit 0x80.
Vsense address As=0x01, expected ≈ +1.66V.
Ch.01 Vdd, address As=0x00, expected +0.94V
Curent sense I(DGND), Ch.27, address 0x1A; expected ≈ –2.4V (I=2.4mA).
No diode compensation required.
All other channels should be close to zero.

Reverse bias mode:
Vdrive –2V5, drive address Ad=0x02 (hex).
Vsense (address As=0x04), expected ≈ –1.7mV.
Curent sense I(DGND), Ch.32, address 0x1F; expected ≈ +2.5V (I=2.5µA).

Measurement resolution: 30kΩ between VddSense and Vdd; 70kΩ between VddSense and DGND or DgndSense. More than 20MΩ to some other channels..

Ch.04 Select (ClkSel)
Forward bias mode:
Vdrive +2V5, address Ad=0x03 (hex), ORed with polarity bit 0x80.
Vsense address As=0x05, expected ≈ +1.85V.
Curent sense I(DGND), Ch.27, address 0x1A; expected ≈ –0.524V (I=0.524mA).
Diode compensation: address 0x1F, expected ≈ –1.1V
All other channels should be close to zero.

Reverse bias mode:
Vdrive –2V5, drive address Ad=0x03 (hex).
Vsense (address As=0x05), expected ≈ –2.5V.
Curent sense I(DGND), Ch.32, address 0x1F; expected ≈ 0V (I=0).

Measurement resolution: 200kΩ between Select and DGND, Vdd, VddSense or DgndSense. More than 20MΩ with negative voltage.

Ch.05 Reset
Forward bias mode:
Vdrive +2V5, address Ad=0x04 (hex), ORed with polarity bit 0x80.
Vsense address As=0x02, expected ≈ +2.5V.
Curent sense I(DGND), Ch.27, address 0x1A; expected ≈ 0V (I=0).
No diode compensation required.
All other channels should be close to zero.

Reverse bias mode:
Vdrive –2V5, drive address Ad=0x04 (hex).
Vsense (address As=0x04), expected ≈ –0.5V.
Curent sense I(DGND), Ch.32, address 0x1F; expected ≈ +2.5V (I=2.5µA);

Measurement resolution: more than 20MΩ between Reset and DGND, Vdd, VddSense or DgndSense, both with positive and negative voltage.

Ch.06 ILED/VCSEL
Forward bias mode:
Vdrive +2V5, address Ad=0x05 (hex), ORed with polarity bit 0x80.
Vsense address As=0x06, expected ≈ +1.83V.
Curent sense I(DGND), Ch.27, address 0x1A; expected ≈ –0.64V (I=0.64mA).
No diode compensation required.
All other channels should be close to zero.

Reverse bias mode:
Vdrive –2V5, drive address Ad=0x05 (hex).
Vsense (address As=0x06), expected ≈ –2.5V.
Curent sense I(DGND), Ch.32, address 0x1F; expected ≈ 0V (I=0);

Measurement resolution: 70kΩ between VCSEL and DGND; more than 20MΩ with negative voltage.

Ch.07 DgndSense
Forward bias mode:
Vdrive +2V5, address Ad=0x06 (hex), ORed with polarity bit 0x80.
Vsense address As=0x03, expected ≈ +1.5V.
Curent sense I(DGND), Ch.27, address 0x1A; expected ≈ –3.9V (I=3.9mA).
Diode compensation: address 0x1F, expected ≈ –4.5V.
All other channels should be close to zero.

Reverse bias mode:
Vdrive –2V5, drive address Ad=0x06 (hex).
Vsense (address As=0x03), expected ≈ 0V.
Curent sense I(DGND), Ch.32, address 0x1F; expected ≈ +2.5V (I=2.5µA);

Measurement resolution: 30kΩ between DgndSense and DGND, Vdd, or VddSense; more than 20MΩ with negative voltage.

Ch.08 PIN-Bias
Forward bias mode:
Vdrive +2V5, address Ad=0x07 (hex), ORed with polarity bit 0x80.
Vsense address As=0x07, expected ≈ +1.95V.
Curent sense I(DGND), Ch.27, address 0x1A; expected ≈ –0.090V (I=90µA).
Diode compensation: address 0x1F, expected ≈ –0.59V.
All other channels should be close to zero.

Reverse bias mode:
Vdrive –2V5, drive address Ad=0x07 (hex).
Vsense (address As=0x07), expected ≈ –2.5V.
Curent sense I(DGND), Ch.32, address 0x1F; expected ≈ 0V (I=0);

Measurement resolution: 1.5MΩ between PIN-Bias and DGND, Vdd, or VddSense; more than 20MΩ with negative voltage.

Ch.09 Temp2
Forward bias mode:
Vdrive +2V5, address Ad=0x08 (hex), ORed with polarity bit 0x80.
Vsense address As=0x08, expected ≈ +1.95V.
Curent sense I(DGND), Ch.27, address 0x1A; expected ≈ –0.120V (I=120µA).
Diode compensation: address 0x1F, expected ≈ –0.62V.
All other channels should be close to zero.

Reverse bias mode:
Vdrive –2V5, drive address Ad=0x08 (hex).
Vsense (address As=0x08), expected ≈ –2.5V.
Curent sense I(DGND), Ch.32, address 0x1F; expected ≈ 0V (I=0);

Measurement resolution: 1.5MΩ between Temp2 and DGND, Vdd, or VddSense; more than 20MΩ with negative voltage.

Ch.10 Temp1
Forward bias mode:
Vdrive +2V5, address Ad=0x09 (hex), ORed with polarity bit 0x80.
Vsense address As=0x0C, expected ≈ +1.95V.
Curent sense I(DGND), Ch.27, address 0x1A; expected ≈ –0.175V (I=175µA).
Diode compensation: address 0x1F, expected ≈ –0.68V.

All other channels should be close to zero.

Reverse bias mode:
Vdrive –2V5, drive address Ad=0x09 (hex).
Vsense (address As=0x0C), expected ≈ –2.5V.
Curent sense I(DGND), Ch.32, address 0x1F; expected ≈ 0V (I=0);

Measurement resolution: 1.5MΩ between Temp1 and DGND, Vdd, or VddSense; more than 20MΩ with negative voltage.

Ch.11 VccSense
Forward bias mode:
Vdrive +2V5, address Ad=0x0A (hex), ORed with polarity bit 0x80.
Vsense address As=0x09, expected ≈ +1.45V.
Vcc, Vsense Ch.15 address As=0x0B, expected ≈ +1.12V.
Curent sense I(AGND), Ch.28, address 0x1B; expected ≈ –3.4V (I=3.4mA).
Diode compensation: address 0x1D, expected ≈ –4V.
All other channels should be close to zero.

Reverse bias mode:
Vdrive –2V5, drive address Ad=0x09 (hex).
Vsense (address As=0x0C), expected ≈ 0V.
Curent sense I(AGND), Ch.30, address 0x1D; expected ≈ 0V (I=0);

Measurement resolution: 10kΩ between VccSense and Vcc, 30kΩ between VccSense and AGND, or AgndSense; same with negative voltage; more than 20MΩ to some other channels.

Ch.12 AgndSense
Forward bias mode:
Vdrive +2V5, address Ad=0x0B (hex), ORed with polarity bit 0x80.
Vsense address As=0x0D, expected ≈ +1.2V.
Curent sense I(AGND), Ch.28, address 0x1B; expected ≈ –6V (I=6mA).
Diode compensation: address 0x1D, expected ≈ –6.68V.
All other channels should be close to zero.

Reverse bias mode:
Vdrive –2V5, drive address Ad=0x09 (hex).
Vsense (address As=0x0C), expected ≈ 0V.
Curent sense I(AGND), Ch.30, address 0x1D; expected ≈ +2.5V (I=2.5µA);

Measurement resolution: 20kΩ between VccSense and AGND, Vcc, or AgndSense; more than 20MΩ to other channels.

Ch.13 Shield/Drain-Wire
Forward bias mode:
Vdrive +2V5, address Ad=0x0C (hex), ORed with polarity bit 0x80.
Vsense address As=0x0A, expected ≈ 0V.
Connector housing, Ch.23, Vsense address As=0x13, expected 0V.
Curent sense I(Shield), Ch.31, address 0x1E; expected ≈ –1.9V (I=1.9mA).
Diode compensation: address 0x1C, expected ≈ –2.5V.
All other channels should be close to zero.

Reverse bias mode:
Vdrive –2V5, drive address Ad=0x0C (hex).
Vsense (address As=0x0A), expected ≈ 0V.

Curent sense I(Shield), Ch.31, address 0x1C; expected ≈ +2.5V (I=2.5µA);

Measurement resolution: more than 20MΩ to some other channels.

Ch.14 HVret
Forward bias mode:
Vdrive +2V5, address Ad=0x0D (hex), ORed with polarity bit 0x80.
Vsense address As=0x0E, expected ≈ 0V.
Curent sense I(HVret), Ch.25, address 0x18; expected ≈ –1.9V (I=1.9mA).
No diode compensation required; address 0x19, expected ≈ –1.9V.
All other channels should be close to zero.

Reverse bias mode:
Vdrive –2V5, drive address Ad=0x0D (hex).
Vsense (address As=0x0E), expected ≈ 0V.
Curent sense I(Hvret), Ch.25, address 0x18/0x19; expected ≈ +2.5V (I=2.5µA);

Measurement resolution: poor. Used for I-to-V calibration only.

Ch.15 Vcc
Forward bias mode:
Vdrive +2V5, address Ad=0x0E (hex), ORed with polarity bit 0x80.
Vsense address As=0x0B, expected ≈ 1.46V; same at VccSense Ch.11, As=0x0D.
Curent sense I(AGND), Ch.28, address 0x1B; expected ≈ –4.4V (I=4.4mA).
Diode compensation: address 0x1D, expected ≈ –5.1V.
All other channels should be close to zero.

Reverse bias mode:
Vdrive –2V5, drive address Ad=0x0E (hex).
Vsense (address As=0x0B), expected ≈ 0V.
Curent sense I(AGND), Ch.25, address 0x1D, expected ≈ +2.5V (I=2.5µA);

Measurement resolution: 30kΩ between Vcc and AGND or AgndSense; 10kΩ between Vcc and VccSense; more than 20MΩ to some other channels.

Ch.16 AGND
Forward bias mode:
Vdrive +2V5, address Ad=0x0F (hex), ORed with polarity bit 0x80.
Vsense address As=0x0F, expected ≈ 0V.
Curent sense I(AGND), Ch.28, address 0x1B; expected ≈ –1.9V (I=1.9mA).
Diode compensation: address 0x1D, expected ≈ –2.5V.
All other channels should be close to zero.

Reverse bias mode:
Vdrive –2V5, drive address Ad=0x0F (hex).
Vsense (address As=0x0F), expected ≈ 0V.
Curent sense I(AGND), Ch.25, address 0x1D, expected ≈ +2.5V (I=2.5µA);

Measurement resolution: poor. Used for calibration only.

Ch.17 HVbias
Forward bias mode:
Vdrive +2V5, address Ad=0x10 (hex), ORed with polarity bit 0x80.
Vsense address As=0x10, expected ≈ +2.3V.

Curent sense I(HVret), Ch.28, address 0x18; expected ≈ –1.5V (I=1.5µA).
No diode compensation (address 0x19 gives the same reading as 0x18).
All other channels should be close to zero.

Reverse bias mode:
Vdrive –2V5, drive address Ad=0x0F (hex).
Vsense (address As=0x0F), expected ≈ –2.5V.
Curent sense I(AGND), Ch.25, address 0x1D, expected ≈ +2.5V (I=2.5µA);

Measurement resolution: more than 50MΩ between HVbias and HVret; more than 20MΩ between HVbias and some other channels.

Ch.23 Connector housing (should be shorted to Shield)
Forward bias mode:
Vdrive +2V5, address Ad=0x16 (hex), ORed with polarity bit 0x80.
Vsense address As=0x13, expected ≈ 0V.
Curent sense I(Shield), Ch.31, address 0x1E; expected ≈ –1.9V (I=1.9mA).
Diode compensation: address 0x1D, expected ≈ –2.5V.
All other channels should be close to zero.

Reverse bias mode:
Vdrive –2V5, drive address Ad=0x16 (hex).
Vsense (address As=0x13), expected ≈ 0V.
Curent sense I(Shield), Ch.29, address 0x1C, expected ≈ +2.5V (I=2.5µA);

Measurement resolution: poor; used for checking a short between the connector housing and shield only (minimum resistance detected ≈ 0.15Ω = 1LSB, however, the hardware accuracy limits this to at least 5LSBs).
