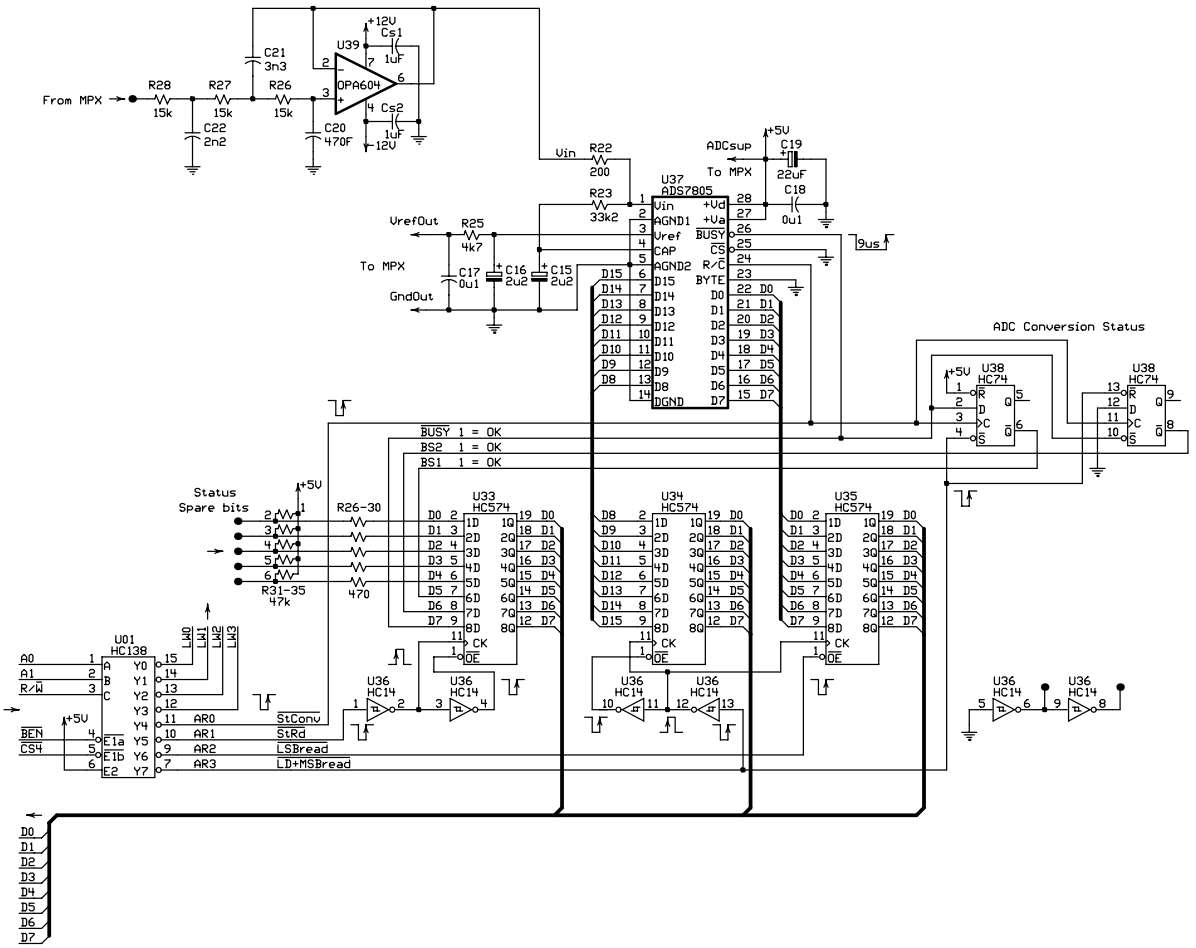

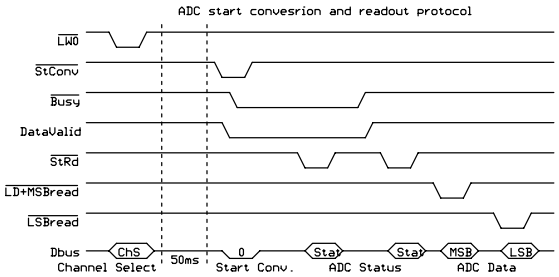

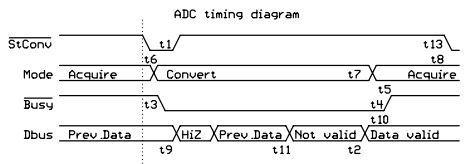

ADC timing table

Symbol	Description	min	typ	max	units
t1	Convert pulse width	40		6000	ns
t2	Data valid delay			8000	ns
t3	Busy delay			65	ns
t4	Busy Low width			8000	ns
t5	EOC to Busy High		220		ns
t6	Aperture delay		40		ns
t7	Convetsion time		7600	8000	ns
t6+t7	Through-put time		9000	10000	ns
t8	Acquisition time			2000	ns
t9	Bus relinquish time	10	35	83	ns
t10	Data valid to Busy High	50	200		ns
t11	Prev Data valid delay		7400		ns
t12	Conv from CS setup time	10			ns
t13	Time between converions	10000			ns

Institut Jožef Stefan, Ljubljana

projekt/naloga :	Cable+PP3+DPPB1 Test Box		
sestavni del :	ADC-16bit	načrtoval	E. Margan
		risal	E. Margan
pripombe :	tolerance uporov 1%	datum-0	2002.02.19.
	tolerance kondenzatorjev 20 %	datum-z	2005.05.12.
		datoteka	ADC16B.SCH