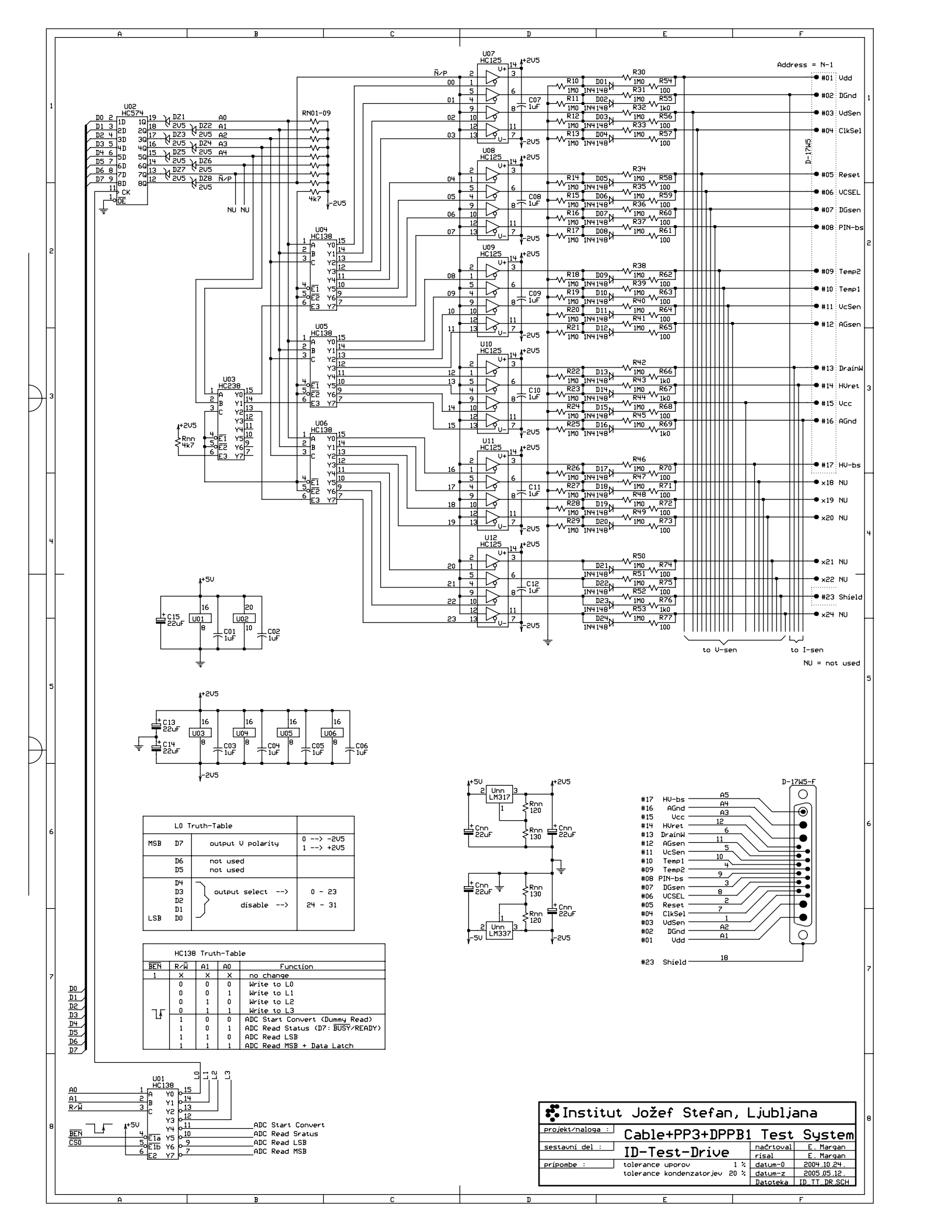

L0 Truth-Table		
MSB D7	output V polarity	0 --> -2V5 1 --> +2V5
D6	not used	
D5	not used	
D4	output select -->	0 - 23
D3		
D2		
D1	disable -->	24 - 31
LSB D0		

HC138 Truth-Table				
$\overline{BEN}$	R/$\overline{W}$	A1	A0	Function
1	X	X	X	no change
	0	0	0	Write to L0
	0	0	1	Write to L1
	0	1	0	Write to L2
	0	1	1	Write to L3
	1	0	0	ADC Start Convert (Dummy Read)
	1	0	1	ADC Read Status (D7: $\overline{BUSY}$/READY)
	1	1	0	ADC Read LSB
	1	1	1	ADC Read MSB + Data Latch

projekt/naloga :	Cable+PP3+DPPB1 Test System	
sestavni del :	ID-Test-Drive	načrtoval: E. Margan
pripombe :	tolerance uporov 1 % tolerance kondenzatorjev 20 %	risal: E. Margan datum-0: 2004.10.24. datum-z: 2005.05.12. Datoteka: ID_TT_DR.SCH

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