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Cable & Dummy-PPB1 Testing

(material for the discussion at the phone-conf. on Jan.26.05)
(updated upon the requirements set at the phone-conf. on Jan.26.05)

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General Considerations

The Dummy-PPB1 functional goals :

- serving as a cable support (until the actual PPx1 is installed in to the system)
- serving as a functional power supply load (full-load test is done elsewhere)
- allowing the PP3 filters and the cable connectivity and insulation checking, as well as the identification and verification of the correct connections ; the test procedure includes the High-Voltage sustain and leakage test and the PP3 Voltage Limiter activation threshold test.

Electrical Testing - Brief System Description + Update

The cable + PP3 + DPPB1 connection and their compnents are shown in Fig. 1. In regard to the previous version, the load resistors on the power lines have been increased in value from 33 to 330 Ω for Vcc-AGnd and from 39 to 390 Ω for Vdd-DGnd. Aslo, the cable Shield and the Drain-wire are connected to the metal base plate and not by the JST connector, so the ground contact for the DummyPPB1 is provided via the mounting screws.

The DPPB1 PCB is shown in Fig. 2, and it has the same connector types and layout as the original PPB1, although it does not have the Low-Mass-Tape solder pads area. Each channel is connected to the common ground and via the mounting screws to the base plate. Added to each channel is a SMD LED (0603 size) in series with a current limiting resistor, both added in parallel to the appropriate power resistor.

The tests are performed by a PC-driven automatic "Test-Box". The PC controls the various test parameter settings and performs the data flow control on the Test-Box local bus over a special interface, using a "virtual handshaking" protocol, which allows a passive test system to function (no need for a local microprocessor, thus also less trouble with programming and communication ; this same configuration, but with somewhat different subsystems, was used already for the PP1B/F and TPP1C/D testing). The PC is also used to display the test results and to store the data for later checks, should the need arise.

The Test Box has 3 distinctive units, each dedicated to a particular type of test:

1) The low-voltage connectivity and insulation checking unit :

- a 16-bit DAC, which sets the output drive voltage ($\pm 5V_{max}$, $Z_o = 50\,\Omega$) ;
- an input/output switching matrix, which selects the driven line one at a time, while all other lines are used as inputs, testing the return current and any eventual leakage current ;

– an array of opamps, providing the virtual ground for equalizing the potentials of the non-driven lines and serving as current-to-voltage converters for measuring the return current and any leakage from the driven line to every other one, including the ground ;

– a 16-bit ADC with a +/-10V input range, measuring the driven line output voltage and the current from all other lines ;

– the digital logic interface

The simplfied circuit diagram of this unit is shown in Fig. 3.

2) The High-Voltage sustain and leakage currcnt test unit ; this unit drives the HV-bias and HV-ret line pair by a voltage of 550 V_{DCmax}, current limited to 500 µA and an output impedance $Z_o = 10\,k\Omega$, with the turn-on risetime of ≈ 0.5 s and measures the actual drive voltage (via a 50 MΩ, 1/100 attenuator), the HV-ret current, the ground leakage current and the leakage to any other line for at least 5 s. Due to a relatively large capacitance value between the HV-boas and HV-ret (27 nF/630V on PP3),the leakage currents will need about 10-20 s to stabilize before the final 5 s measurement interval. At the end of the test the HV capacitor is discharged to less than 10 V before the test result is confirmed. The simplified circuit diagram is shown in Fig. 4.

3) The Voltage Limiter test unit ; this unit provides a current of 1 A_{DCmax}, voltage-limited to 8 V, switched to each Voltage Limiter one at a time. The actual activation threshold of the Limiter is measured via the appropriate Sense lines. The test current is applied for only a brief interval (300 ms), thus limiting the power dissipation. The threshold voltage is monitored throughout the interval and the average of the last 50 ms is stored. The simplified circuit diagram is shown in Fig. 5.

Regarding the safety, all the voltage and current limiting, as well as the test timing is implemented passively, by finite output impedance, as well as actively, by automated hardware control, monitoring the system for overload. The software only sets the initial test conditions and controls the analog-to-digital conversion. Of course, the test can be ended by software also, in case a major faulty condition is encountered. Also, the operator can always interrupt the test, returning the operating conditions to idle.

To ensure operators' safety, the system is designed so that it is possible to touch any contact, HV included, with bare hands ; although, in order to get reliable leakage readings, this should be prevented if possible.

For further safety measures, the test repetition rate is low, since each test requires the entry of the bar-code of tested cable and the operator's confirmation before the test is executed. This ensures a dead time of a few seconds between tests.

The Test Box design includes the possibility of self-checking and self-calibration, which is executed at the program start, or, if required, before any test.

The test results will be written in ASCII format, redable by any word-processing program.

The test conditions, nominal values, tolerances, error thresholds, etc., will be written on a separate ASCII file which will be read by the program on start-up. In this way, the conditions are kept away from the program and still allowing the changes to be made easily, if needed.

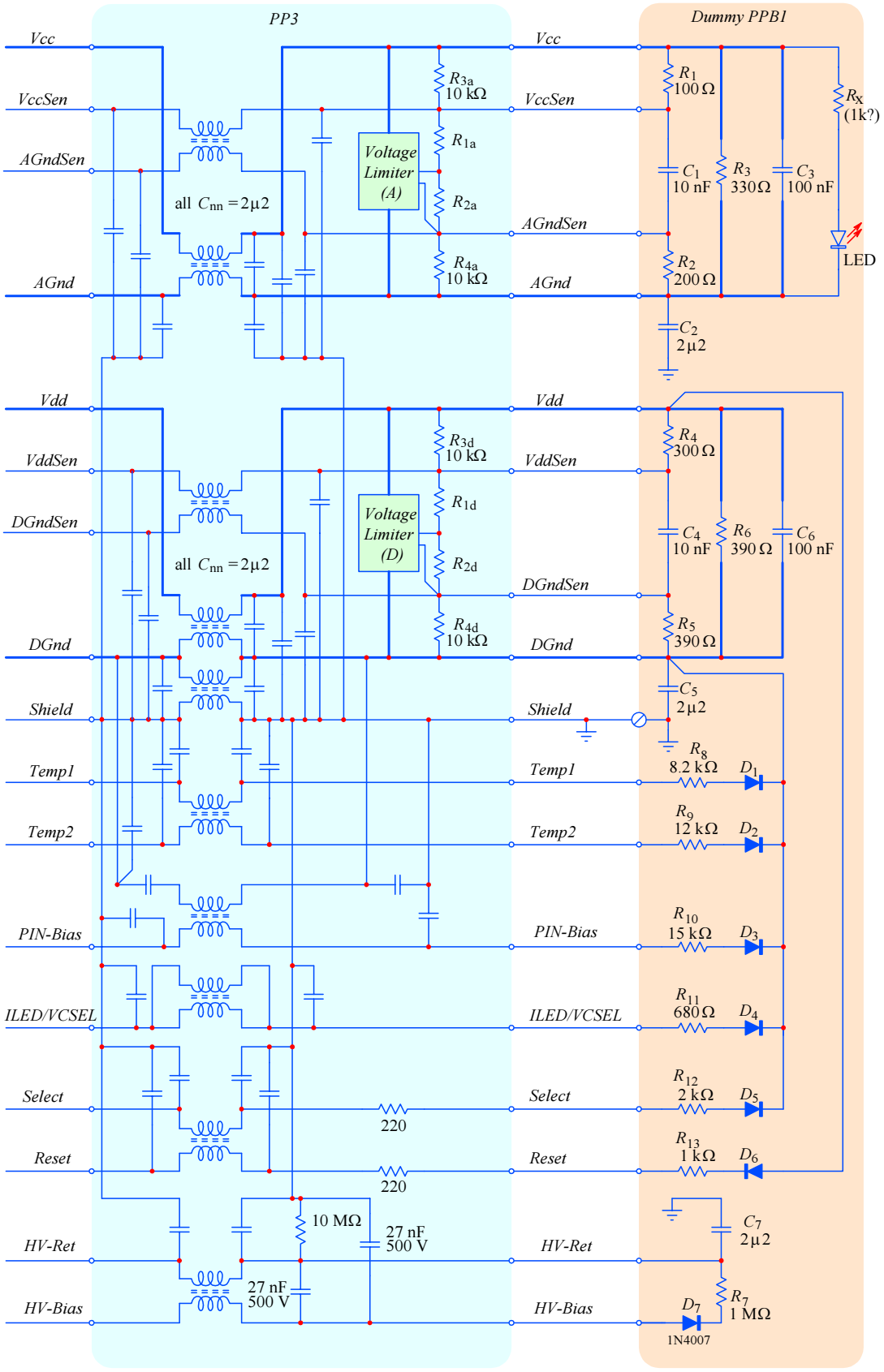

Fig.1 : Cables + PP3 + DPPB1 layout

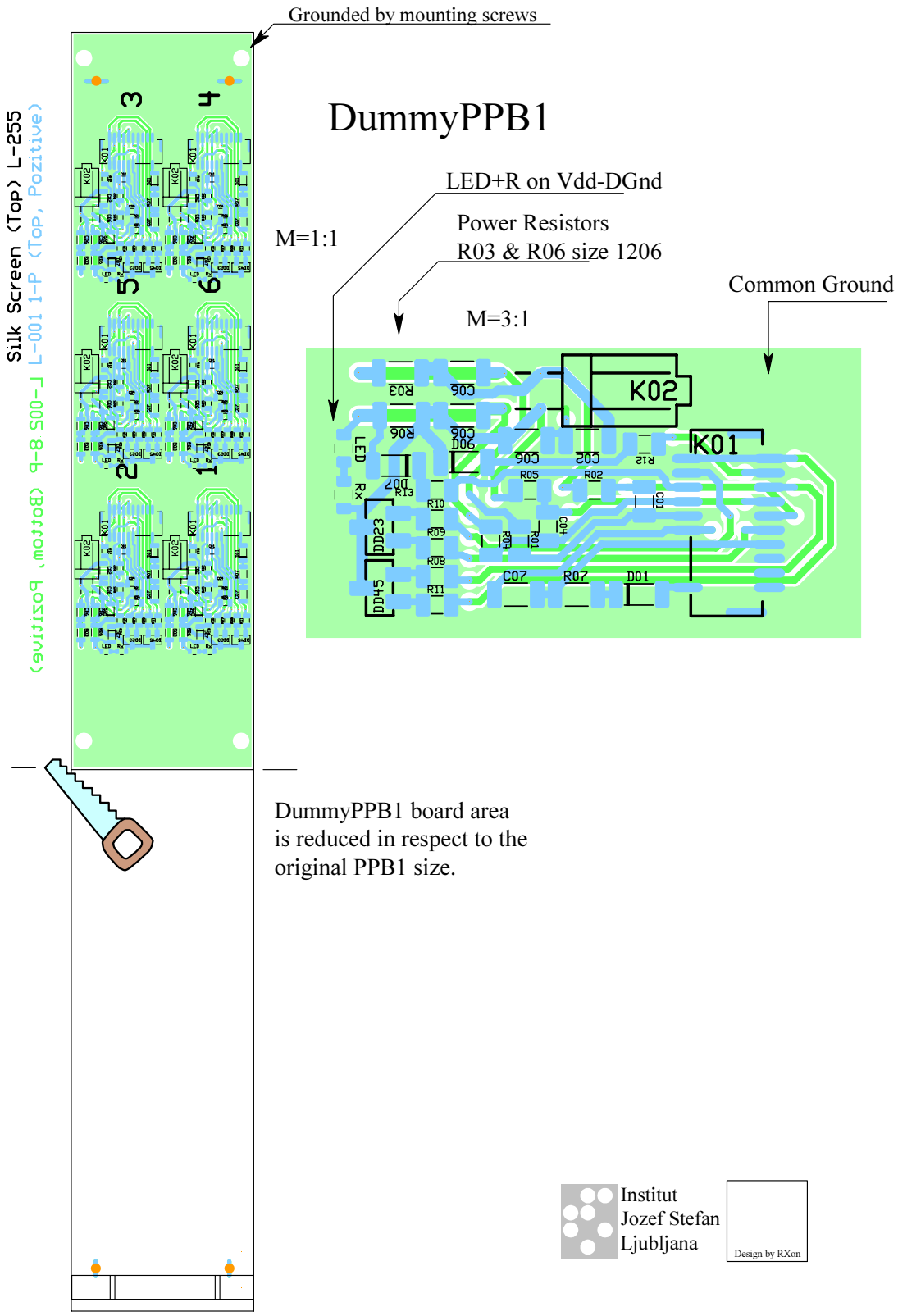

Fig.2 : DPPB1 pcb layout

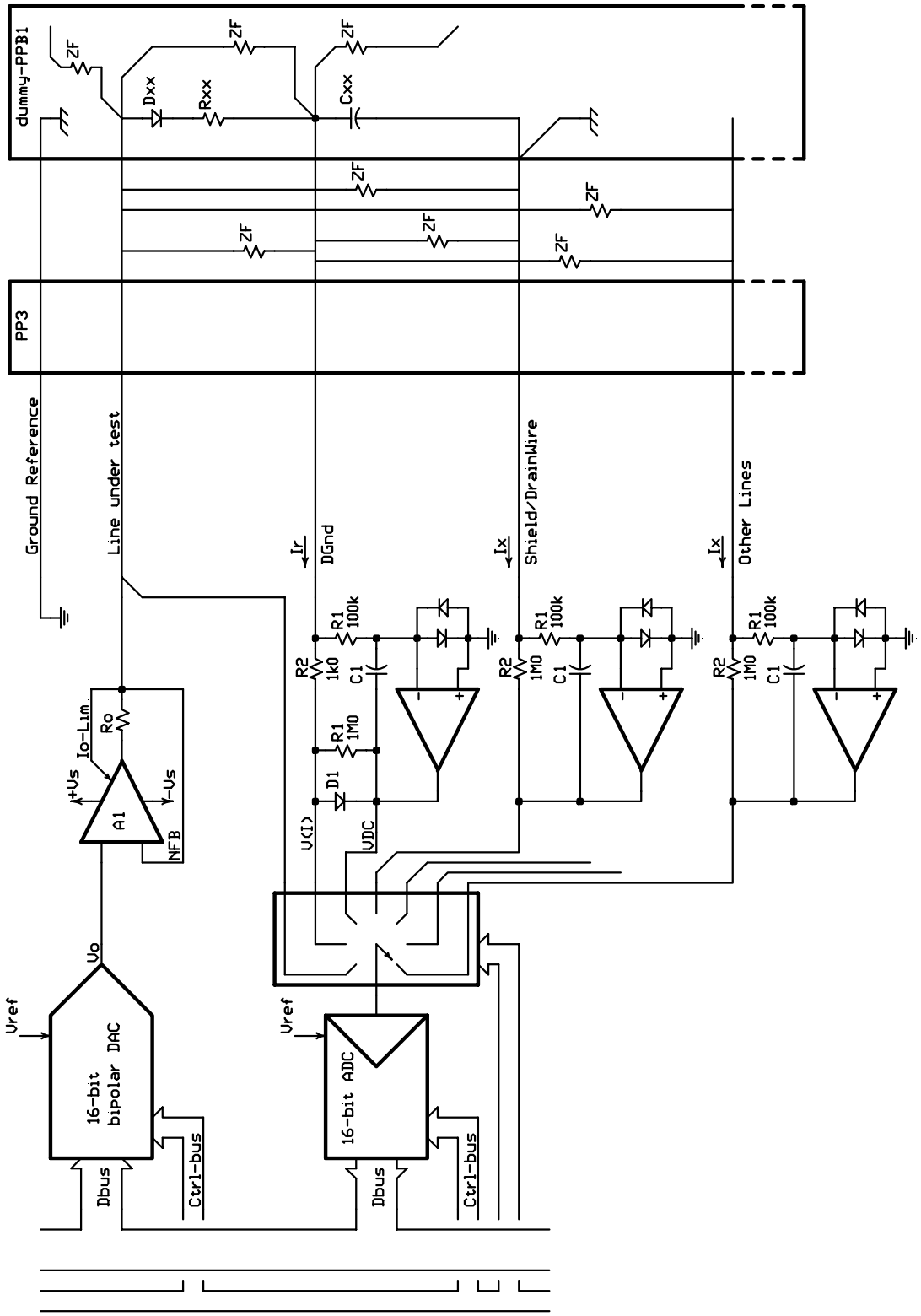

Fig.3 : Measurement principle illustration for connectivity identification

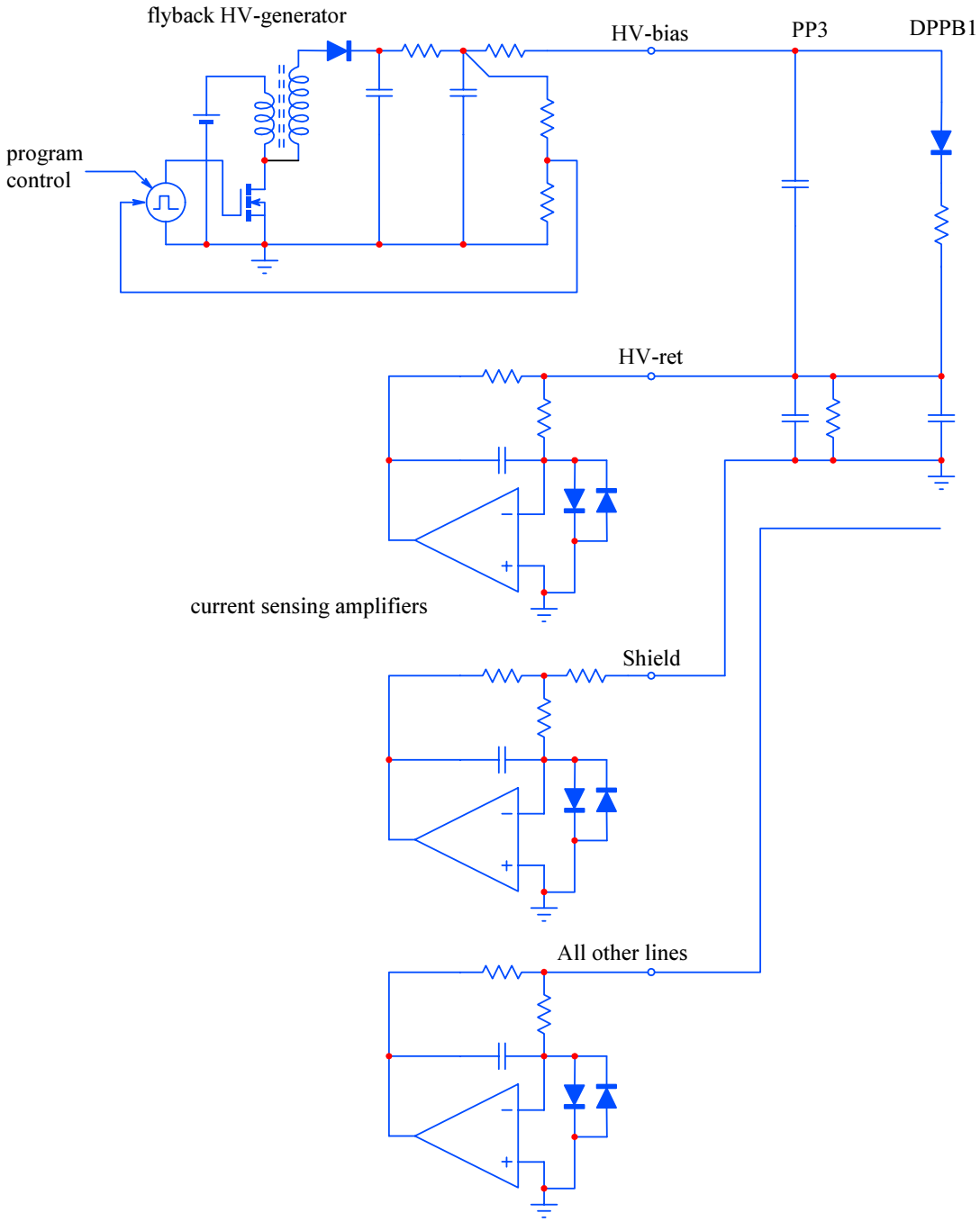

Fig. 4 : The High-Voltage measurement unit smplified circuit

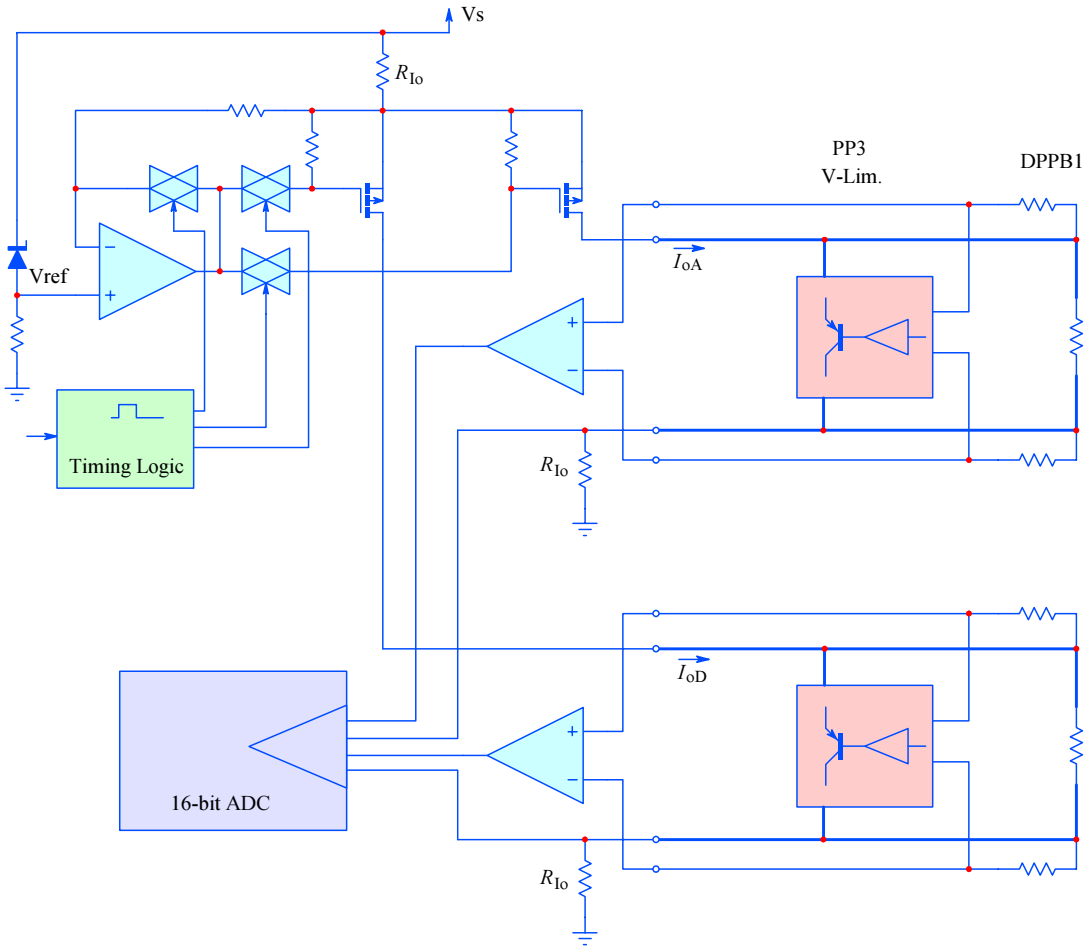

Fig. 5 : The Voltage Limiter test circuit simplified diagram