# Minutes of the SCT Power Supply and Distribution System Review

Held at CERN on 18-Oct-01

Attendees:

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|---|---|---|
| J. Bohm | M. Mikuz | M. Morrissey |
| J. Stastny | V. Cindro | M. Tyndel |
| I. Polak | E. Margan | V. O'Shea |
| P. Malecki | R. Brenner | A. Grillo |
| S. Koperny | H. Pernegger | E. Spencer |

These brief minutes will only outline the issues raised and some decisions made during the 10+ hour review which attempted to cover all the components of the SCT Power Supply and Distribution System including the power supply crates and cards, the cables and patch panels to PP1.

Interlocks:

The interlock card inside the power supply crate will be a 3U card located in the same slot as the crate controller (also a 3U card).

Cable from Interlock Matrix Box (probably one in USA15 and another in US15 but physically separated from the power supply crate) to interlock card will connect via DB15 connector on back of backplane.

Input signals to interlock card will be single ended TTL. 12 cooling interlocks and one VCSEL interlock. VCSEL interlock also routed through matrix box.

What is max distance from Interlock Matrix Box to power supply crate?
Is single-ended TTL possible over that distance?
What is max distance of signals to Interlock Matrix Box from cooling interlock box and from ROD crates (VCSEL interlocks)?
What will be signal type for such long runs?

Input signals to interlock card will be opto-isolated immediately at input.
No need to further isolate signals onto backplane.

Need schematic for interlock card.

Manual switch to override VCSEL interlock will be located on BOC or ROD crate.

General problem for interlock system is that SCT needs a naming convention for all 4088 modules and needs to initiate process to map modules into RODs,

power supplies, interlocks and associated cables. Do we need task force? R. Brenner to initiate.

Power Supply Crate Backplane:

Schematic and layout for backplane not yet complete or final.

Schematics need improved labeling in nameplate to include consistent name of schematic and correct "Sheet n or nn" designation.

Backplane will be 8-layer board.

Need to decide on electrical connection from Power Pack to Backplane, in particular the connection for the (+5, +12, Gnd, Communication) lines and also for the 48V AC power. These connections, especially the 48V AC, must be done in such a way to minimize any power radiation or common mode imbalance.

Need a consistent design for location of Power Pack in rack with respect to the crate.

HV traces and pins must meet 2.5mm spacing wherever they are exposed to air.

Power Pack:

Estimated size of power pack is 90 mm x 200 mm x (300 mm to 400 mm). Exact form factor not established, depends upon final choice of location relative to crate.

Need final plan for location of Power Pack with respect to crate. This must be worked out with overall rack layout to be acceptable with rack cooling design. It must also provide for good power transmission to Backplane to minimize power radiation and common mode imbalance. Prague group must work this out with ATLAS rack people and the Krakow group designing the Backplane.

A schematic exists for the Power Pack but it is not viewed to be final. Will have to be optimized after prototype is built and tested. See schedule at end.

Current plan is to provide a single phase AC input to Power Pack from a long duration UPS to power crate controller and a three phase AC input for bulk power. Given that SCT now plans to provide limited duration UPS to entire power supply system, this plan for separate single phase input from long duration UPS should be reviewed. It may still be a good idea but should be discussed and reviewed.

DCS - PS Interface:

Choice of ELMB for power supply crate controller simplifies this issue. Much of the software being developed by DCS can be used in the PS crate controller.

DCS still does not have final solution for PCI card to drive CANbus to ELMB. For initial testing of power supplies, we can use other interfaces available in ELMB (i.e. not CANbus).

Still need to define actual commands for communication between crate controller and HV and LV cards in crate as well as protocol between crate controller and DCS.

Need schedule for having real DCS interface and control of power supplies.

Length of CANbus to power supply crates in both USA15 and US15 is not believed to cause problem with communication response time. However, need to include specification of what response time is required and expected.

HV Card:

A few components will change from the VME version of this card. They are mostly the micro-controller and associated components. This reduces part count and is approximately cost neutral.

From the secondary transformer winding to the output, all circuitry is the same as the VME card. Therefore, expect same performance (if no new problems are introduced by the moving to the large bulk AC Power Pack).

Suggestion was made to add a common mode choke to each output. This would make the HV outputs symmetric with the LV outputs, which already have such a choke.

Need to fix sheet names on the schematics.

LV Card:

Suggestion to add common mode choke at input to each transformer to improve isolation from bulk Power Pack.

A few components will change from the VME version of this card. They are mostly the micro-controller and associated components. This reduces part count and is approximately cost neutral.

Design will return to using opto isolators rather than transformers to isolate control signals from floating outputs. This may marginalize rad-tolerance of card, however, HV card uses the same opto isolators. This is done to simplify design and save costs. New cost estimate for LV card is reduced by 8%, much of which is due to this change. Would be possible to substitute more rat-tolerant opto isolators.

Common mode test was performed on SCTLV3 by placing 10k resistor from AGND, DGND, PIN or VCSEL outputs to chassis ground. Measured ~1.2 mA (peak-to-peak) through resistor. However, SCTLV3 has an AC tie between AGND and chassis ground, which shunts much of this common mode signal. This test must be re-run with the AC tie removed before we fix the common mode noise spec.

The drain wire on the output cable will be AC tied to DNGD. This should probably be done at the backplane connector for the power cable and not inside the LV card?

Concern was raised about the amount of current drawn by the sense wires in the present design. This makes the sensing susceptible to unexpected loading. One reason for the current (~3 mA?) is that there is evidence that it provides cleaning of pins along the cable run. There are many pin connections so this could be important. Is there a reference for this current cleansing effect?

Voltage Limiter:

The voltage limiter circuit was re-optimized to account for the load on the sense wire by the detector module circuitry including the temperature sensing. It appears now to meet requirements based upon simulations and bench testing.

The limiter circuit now will dump 50 μA into the DGNDsense line during active limiting (a few msec) and 5 μA during nominal (inactive) operation. This is believed to be acceptable.

Next step is to provide the circuit for Prague group to test with SCTLV3 and for System Test to test with module and SCTLV3 setup.

It was pointed out that now with the voltage limiter using the sense wires to sense over voltage condition, it may be possible to move the voltage limiter from PP2 to PP3. There are issues to consider including the resulting impedance between the power supply and the limiter and the reaction time with the longer cable run to the module. The Ljubljana group will study the feasibility of this move.

System Test Experience:

Martin Morrissey gave a report on system test use of SCTLV3 and SCTHV cards:

HV channels occasionally trip off during startup. (2 or 3 out of 12) Upon resetting those that tripped all will come up fine. Sometimes a third try is needed for one channel.

Idd draw by module will typically come on to ~3x nominal when ramped up to 4.0V immediately. This over current often trips supplies, as it should. Without a trip, the current will decay to nominal in about 1 sec. This effect is seen with no clock going to the module since the LVDS drivers on the support cards are 5V parts and run off the same Vdd. With a different setup such that the clock turns on with the module, no trips are observed indicating that the current draw with clock may be more well behaved. Setting the supply to 2.8 volts first and then to 4.0V after a 1 sec delay seems to avoid these problems. Unless the cause of this strange large current draw can be solved, the

standard turn-on will have to include this two stage turn-on (2.8 V first, then 4.0 V).

Ivo Polak showed data regarding the reaction of the SCTLV3 to large changes in load. The recovery time is measured to be ~3 msec.

It was noted that the spikes on SCTLV3 outputs upon turn-on of the VME crate have been confirmed. The cause is understood and will be fixed in final LV cards.

Power Distribution:

Both versions of the proposed cable for PP2 to PP1 (1-in-1 and 2-in-1 varieties) have been received. It turns out that the 1-in-1 variety has a slightly larger than expected diameter (7.5 mm vs. 7.1 mm expected) and the 1-in-1 cable has significantly smaller than expected diameter (5.3 mm vs. 6.0 mm expected). The result is that the 1-in-1 cable will actually take up less total space than the 2-in-1 cable. Based upon this we will focus on tests of only the 1-in-1 cable and try to determine if that can fit in the available services area.

Decision is to keep the 50 mm thick Al tapes for forward from PP0 to PP1. There has been some thought to increasing this to 75 mm to lower the voltage drop, however, there is still some risk to such an increase (manufacturing issues) and the voltage drop to PP2 is no longer has critical now that the voltage limiter uses the sense lines to test for overvoltage.

Considerable discussion was given to the type of material for the crate holding PP2. Ideally this crate would be made of non-metallic material. If it is made of metal, then safety regulations will no doubt require that it be referenced to local ground. This may cause noise pick-up at PP2. Making the crate non-metallic may be expensive. Final decision is to allow PP2 crate to be metal as long as guides are plastic isolate crate from PP2 cards. PP2 cards will be increased to 9U and will accommodate cables for 6 detector modules. This will ensure the 6x grouping. Each channel (patch panel for one detector module's cable) will have shield layer on backside of PCB and metal cover shield on component side. Each such shield will be isolated from similar shields for the other 5 detector modules.

Question was raised about possibly moving the voltage limiter from PP2 to PP3. This may be possible since the voltage limiter uses the sense lines. However, the necessary finite resistance from the power supplies to the voltage limiter must be evaluated as well as the reaction time. Eric Margan will investigate.

We need to decide upon the shells for the cable connectors. Should they be plastic, metal plated plastic or metal. Heinz to determine availability and cost of each. Need to understand safety issues. Heinz and Ned will come to final decision.

No discussion of PP1 was conducted as time was running out. However, completed schematics for PP1 and PP2 were distributed.

There was no presentation on PP3. So far, it appears that no work has been done on this yet.

Finalizing documentation:

Most documents still need some revision prior to FDR. All documents (specs, schematics, etc.) should be finalized as quickly as possible. Heinz has offered to put all documents into EDMS. Each person responsible for a document should send a copy to Heinz. PDF format is preferable but others are OK if necessary.

Schedule:

There appears to be a substantial slip in the schedule compared to what was agreed in Prague in June. This needs to be addressed as soon and as best as possible.

This is the schedule now agreed to:

By 31-Dec-01:

Make existing 300 W Prototype Power Pack ready for crate
Prototype backplane ready
1 HV and 1 LV card complete

Tests will be conducted of this prototype system.

By 15-Jan-02:

Complete first 1.6 W Power Pack

Test this Power Pack with dummy loads by 31-Jan-02
Optimize Final Power Pack design.

By 1-Apr-02:

Complete 1 "unit 0" 1.6 W Power Pack
Complete at least 1 "unit 0" crate with backplane, crate controller and interlock card
Complete at least 12 LV and 6 HV cards.

Test full crate by (1-May-02?)

Project monitoring:

It was agreed to have by-weekly phone meetings to monitor progress.

Meetings will be held on Tuesdays at 17:15 CERN time starting on 30-Oct-01. Heinz will set up conference call with CERN switchboard. We should try to convert to VRVS on the web as soon as possible.

At the first meeting (30-Oct-01) each group should present a list of accomplishments to be finished at each 2-week interval leading to the schedule completion points listed above. Also, each group should point out any resource issues (money and/or personnel) which may be hindering progress to schedule.