Examination Of The Possibility Of Moving The Supply Voltage Limiter To Patch-Panel-3

(Draft)

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The map is not the territory. But it can help you to find your way.
(Philip Darrington, Editor, Wireless World)

Abstract :

The currently proposed location of the supply voltage limiter at PP2 is inconvenient for a number of reasons. As has been suggested at the Design Review (DR) meeting on Oct.18, 2001 in CERN, there is a possibility of moving it to the PP3 position. The complete power supply line of the system has been modeled to allow a quick comparison between the two options at the circuit simulation level. The results obtained are encouraging. But until the measurements are made on the actual system, the discussion remains open.

Motivation :

The long power supply lines cause a considerable voltage drop which must be compensated for by rising the voltage, according to the remote sensing line information. Since the regulation should be tight, the power supply reaction to a change in current demand is relatively slow. The function of the supply voltage limiter is to provide the protection from overvoltage on the detector module in case of sudden current switch-off for a time long enough (~2ms) for the power supply to react and correct the output voltage to the new operating conditions.

The function of accurate voltage sensing is impaired by the request for filtering all the connections with capacitors of large values (4.7μF on power lines and 1μF on sensing lines). The Al low-mass tape at the end of the supply line is long (between 0.8 and 3.1m), adding nearly 1Ω of total resistance on the power lines and up to 5Ω for each sense line, which, when included in the limiter feedback loop can lead to instability (see the Appendix for the study of the resonant frequency compensation).

The original idea was to keep the voltage limiter as close to the Detector Module as possible and the PP2 location was considered just adequate. But the latest limiter

circuitry, using the sense lines for the activation threshold detection and unconditionally stable frequency compensation with increased dV/dt sensitivity, opened the possibility to consider alternative options. For a number of reasons, the PP3 location would offer many advantages, easy serviceability among others. Since it has been argued that moving the voltage limiter to PP3 would introduce even more delay within its own feedback loop and, on the other hand, bring it to close to the power supply unit, where it could eventually condition its stability, it was necessary to investigate the system as a whole as accurately as possible.

Analysis Of The Voltage Limiter Action

The simulation of the limiter operation and the actual measurements, which have been presented at the DR, have both been done with a power supply of a fixed voltage value, whereas the real power supply unit is able to readjust itself to the changed load current demand (within some 2 ms). Therefore, the model of the power supply was made and adjusted to behave like the actual unit, with a transient response similar to the graph presented at the DR by the Praha Group. The model is shown in **Fig. 1** and its simulation with the power line model (but without the voltage limiter) is shown in **Fig. 2**. It is clear that the regulation loop represents a close-enough match to the 2 ms settling time of the actual PS unit. In **Fig. 3** the complete circuit model of the supply-line is shown, including the voltage limiter.

First, the original circuit simulation with the limiter at PP2 has been repeated with the new power supply model. The long-term action (10 ms) is shown in **Fig. 4** and the short-term (first 100 μs) is shown in **Fig. 5**. It can be noted that the long-term conditions with the new power supply model are favourable : the current peaks to nearly 1.5 A and then decays to zero (end of limiting) when the power supply regains its loop control, less than 2 ms after the load current was switched off. As the power supply reaction time is slower than the limiter, there is little change in the simulation result for the first 100 μs, compared to the simulation with a fixed power supply : the voltage overshoot at the Detector Module is practically identical (5.25V peak).

Next, the possibility of moving the voltage limiter to PP3 has been examined. For this, the resistors R_9, R_{10}, R_{11} and R_{12} of **Fig. 3** have been changed to 0.001 Ω and the resistors R_5, R_6, R_7 and R_8 have been changed to the sum of their original value with the respective original values of $R_{9\text{-}12}$. The results are shown in **Fig. 6** and **Fig. 7**.

The notable difference between **Fig. 4** and **Fig. 6** is the increased peak current (3.8A), due to the much lower power-line resistance between the PS and the limiter (0.3 Ω). The current is drawn from both sides : from the two 270 μF capacitors in the PS unit, helping the PS to discharge them, and from the capacitors on PP1 and the Detector Module (4.7 μF and 2.4 μF) . Because the later are much smaller, they are discharged to the limiting threshold value within 20-30 μs. Form then on, the current is drawn form the PS capacitors.

As can be seen in the schematic diagram of the actual PS (page 4, [c,3]), the 0.05 Ω current-sensing resistor R_{178} is in the ground line behind the two 270 μF capacitors, so the current which discharges the capacitors will not cause any additional

voltage drop. If the current sensing is combined with the voltage sensing (as it seems to have been done), the overvoltage information could be made to override any overcurrnet information, preventing the PS unit to switch off. But even if this is not the case, there should be no harm done, since the Detector Module can not be used anyway, until its operating conditions are properly reestablished.

From **Fig. 7** it can be seen that the voltage overshoot at the Detector Module is well controlled by the limiter : compared to **Fig. 5**, its increase is relatively low, peaking to 5.35 V.

We should be aware, however, that we are examining the worst-case condition, since the actual Detector Module will not switch the current off so abruptly. Instead, the actual switch-off current slope lasts for some 60-70 μs and in this case the overshoot is only 4.8 V , as can be seen in **Fig. 9**. To play it completely safe, even in the fast current switch-off case, if a reduced value of the sense-line filtering capacitor of, say, 100 nF can be acceptable, the sense-line delay could be reduced considerably, reducing in turn the overshoot from 5.35 V to 5.15 V, as can be seen in **Fig. 8**.

Finally, the case of increased operating voltage (from 3.5 V to 4.0 V) has been examined in **Fig. 10** and **Fig. 11**. As expected, the voltage overshoot was higher, peaking to about 5.56 V, just above the 5.5 V absolute maximum rating of the Detector Module chips. But again, this could be reduced by reducing the sense-line capacitors. And if the slow current switch-off slope is considered, the actual overshoot would be only 4.85 V.

The discussion above is based on the operating conditions for the analog supply. The digital supply is nominally 4V and the current drawn is about 350 mA, nearly 1/3 of the analog supply current. Also, with no Clock signal, the digital supply current falls to about 1/2 of its normal value, therefore the overshoot will be much lower than on the analog supply. The chip absolute maximum rating for the digital supply is also higher than the analog one, thus, considering the results for the analog supply, the limiting on the digital supply should not be a problem.

Instead Of Conclusion :

The simulation results look promising. Of course, before the final decision is made, the actual system should be thoroughly evaluated and tested for possible misbehaviour. To be honest, I have caught Edsel Murphy asleep on a few occasions, but he always amply compensated for it later!

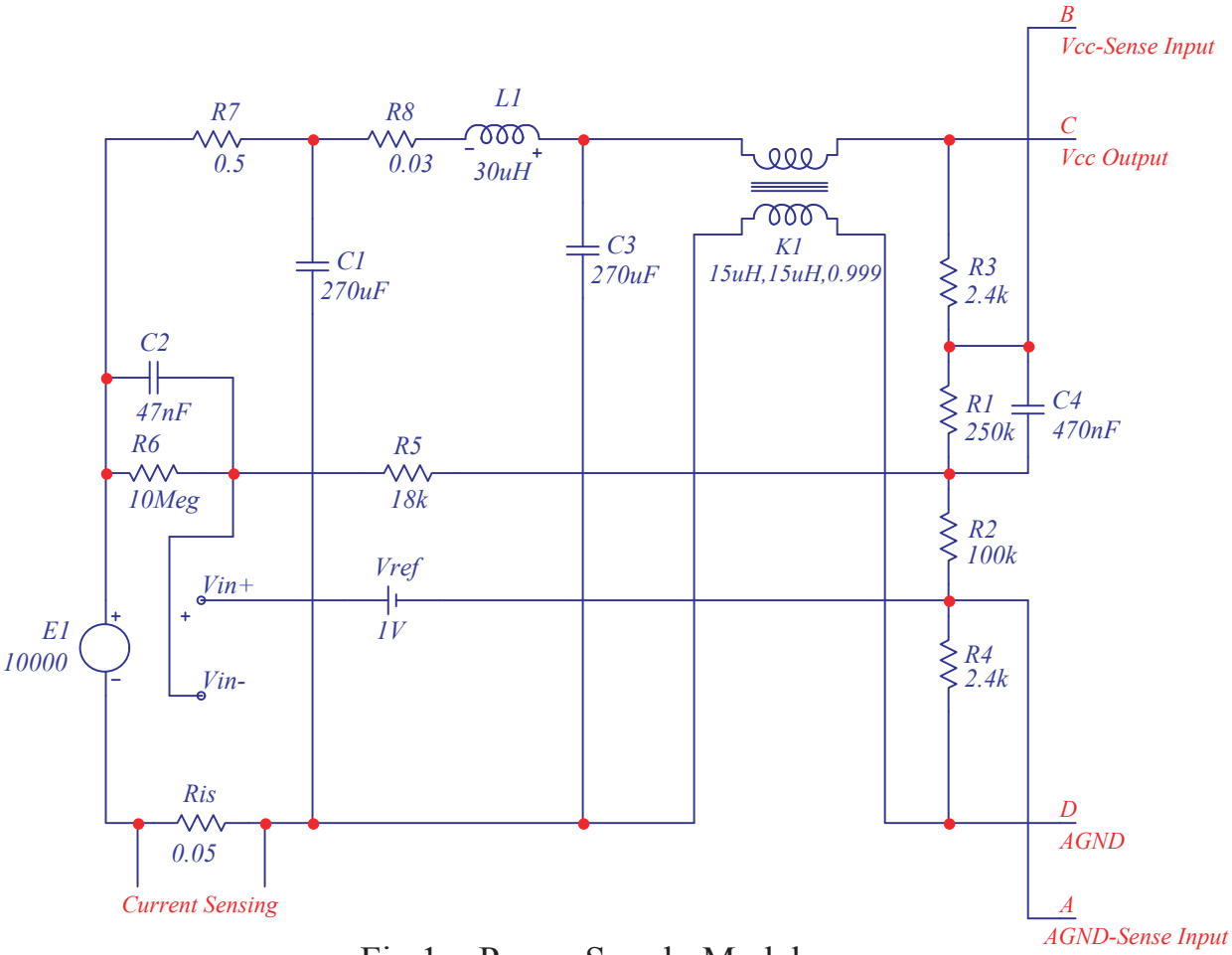

Fig.1 : Power Supply Model

(for simulation purpose only!)

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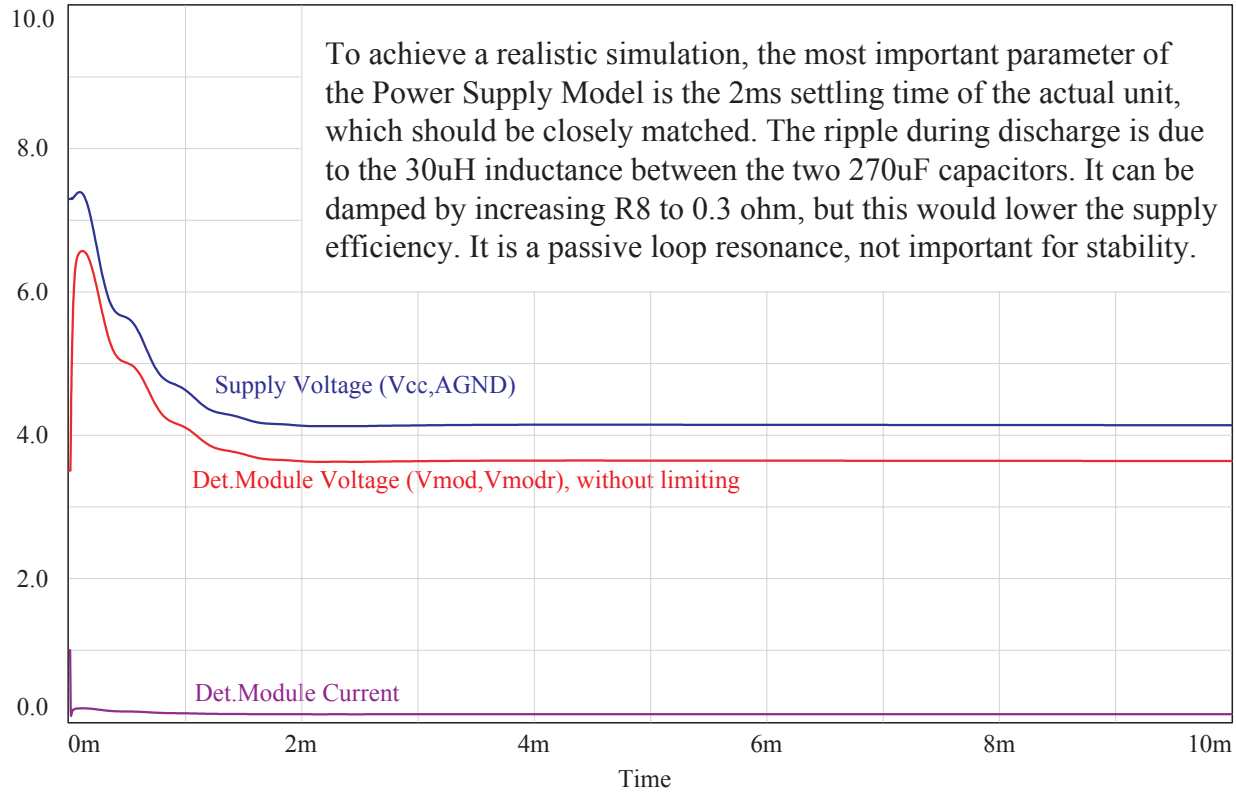
Fig. 2 : Power Supply Response To Load Current Switch-Off (No Limiting)



To achieve a realistic simulation, the most important parameter of the Power Supply Model is the 2ms settling time of the actual unit, which should be closely matched. The ripple during discharge is due to the 30uH inductance between the two 270uF capacitors. It can be damped by increasing R8 to 0.3 ohm, but this would lower the supply efficiency. It is a passive loop resonance, not important for stability.

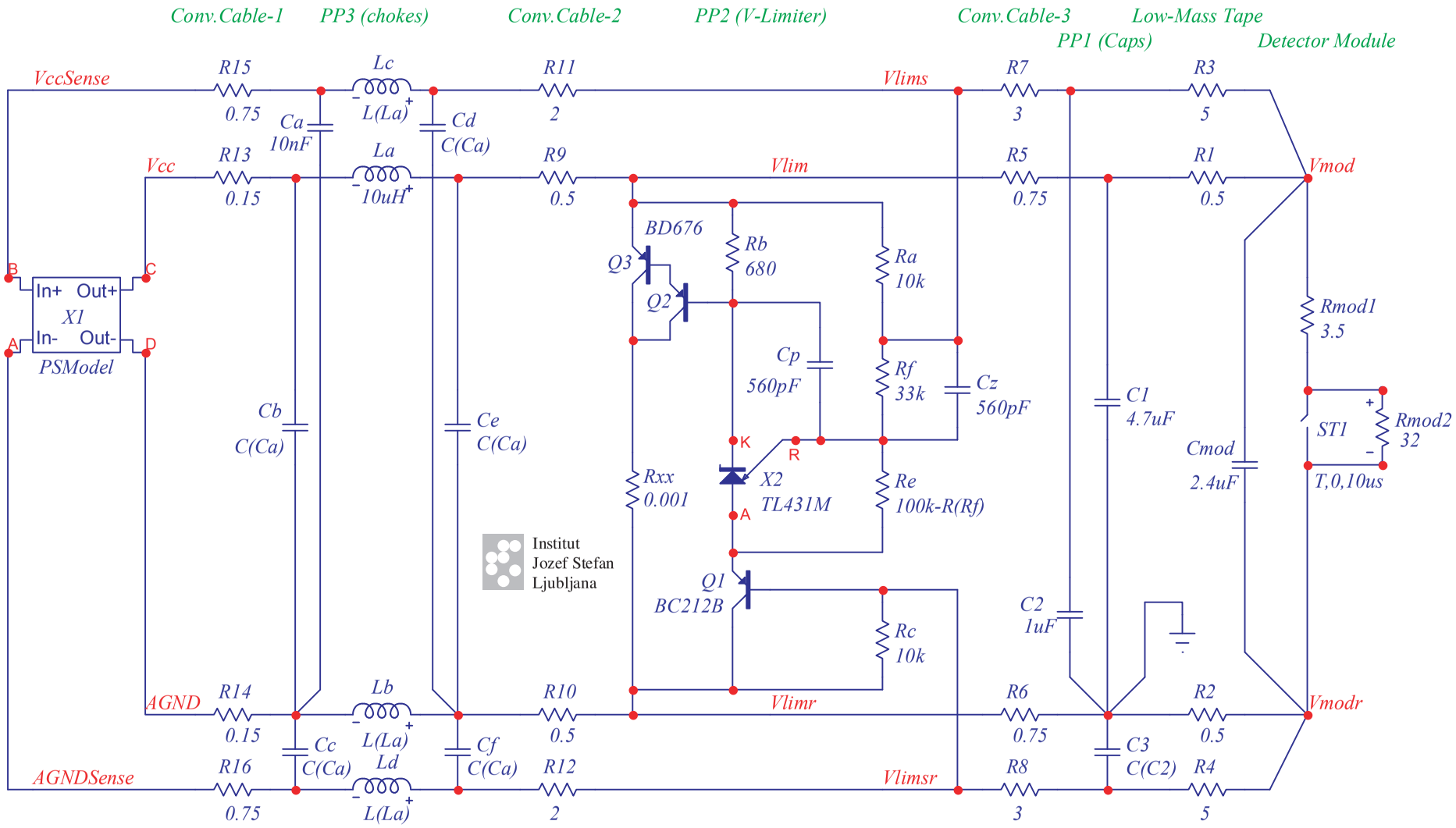


Fig. 3 : Simulation Setup With The Voltage Limiter At PP2

Fig. 4 : Voltage Limiter At PP2

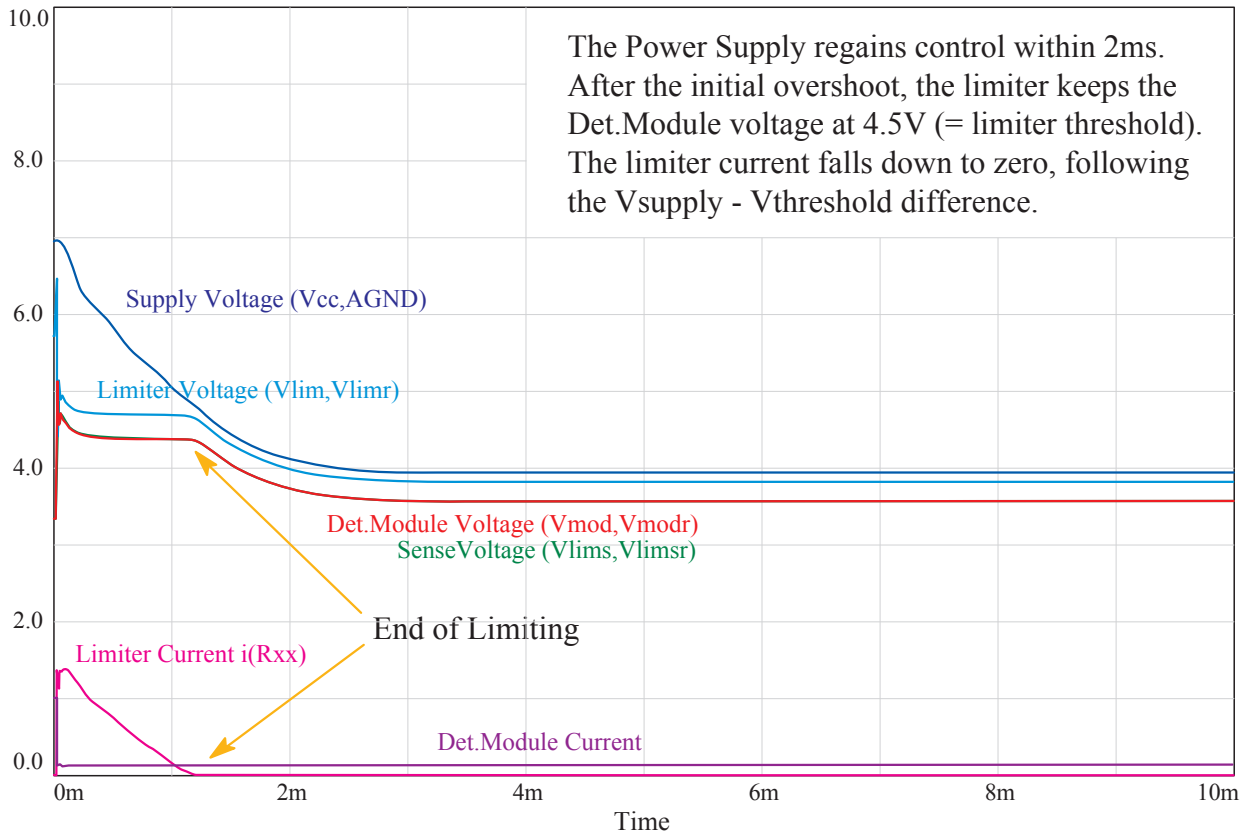


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Fig. 5 : First 100us of Fig.4

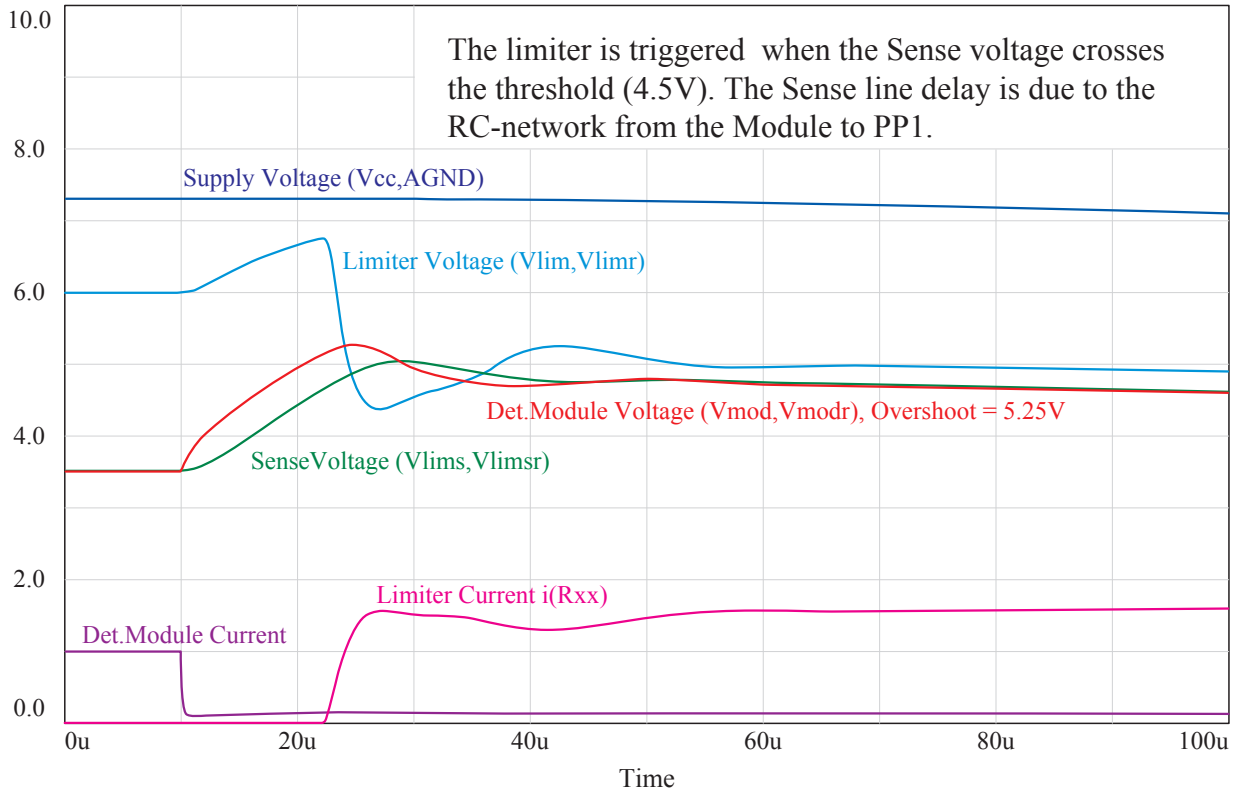

Fig. 6 : Voltage Limiter At PP3

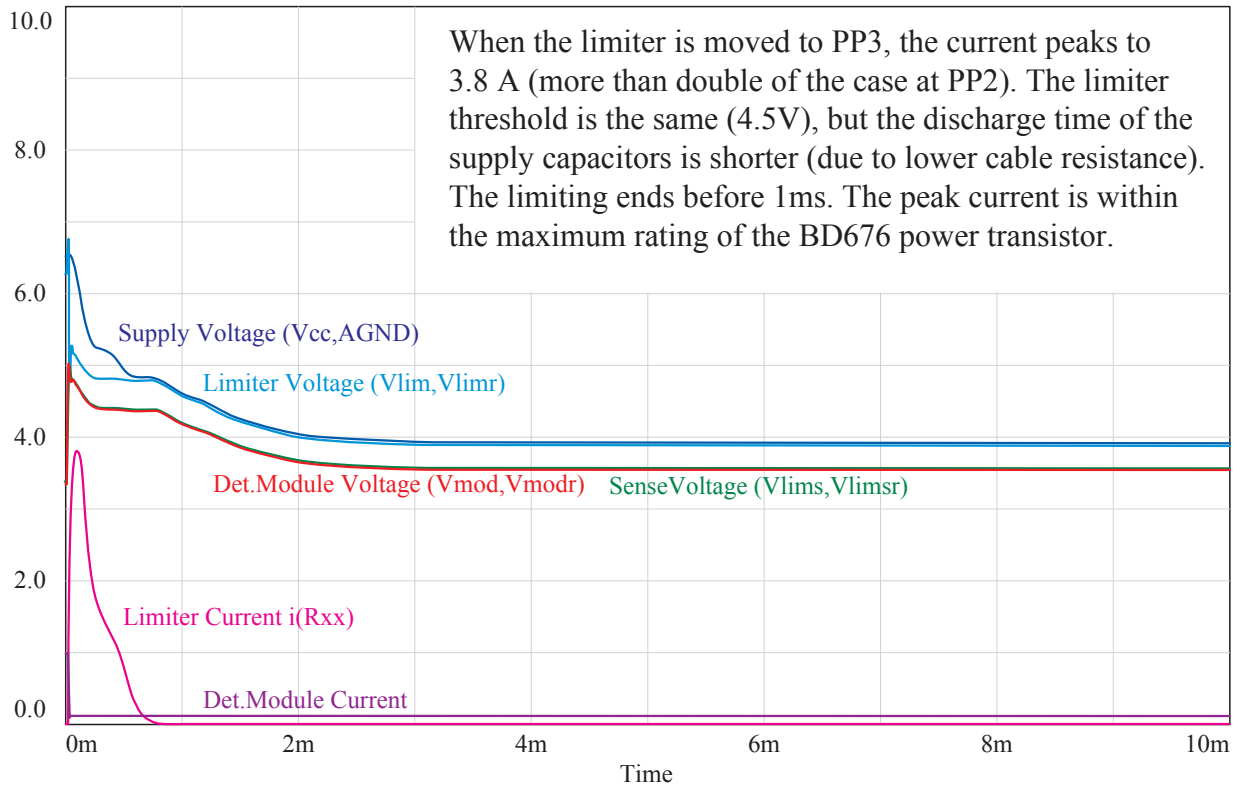

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Fig. 7 : First 100us of Fig.6

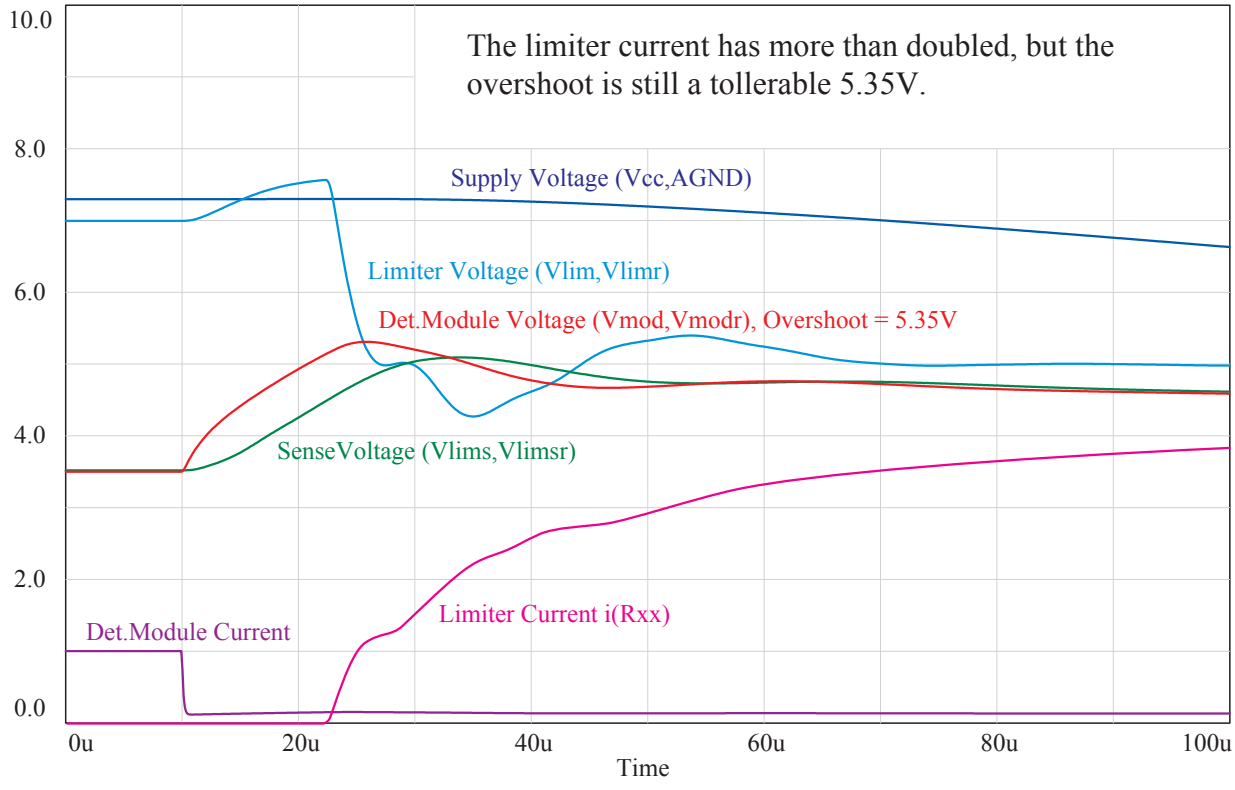

Fig. 8 : Limiter At PP3, Sense Line Capacitance Decreased From 1uF to 0.1uF

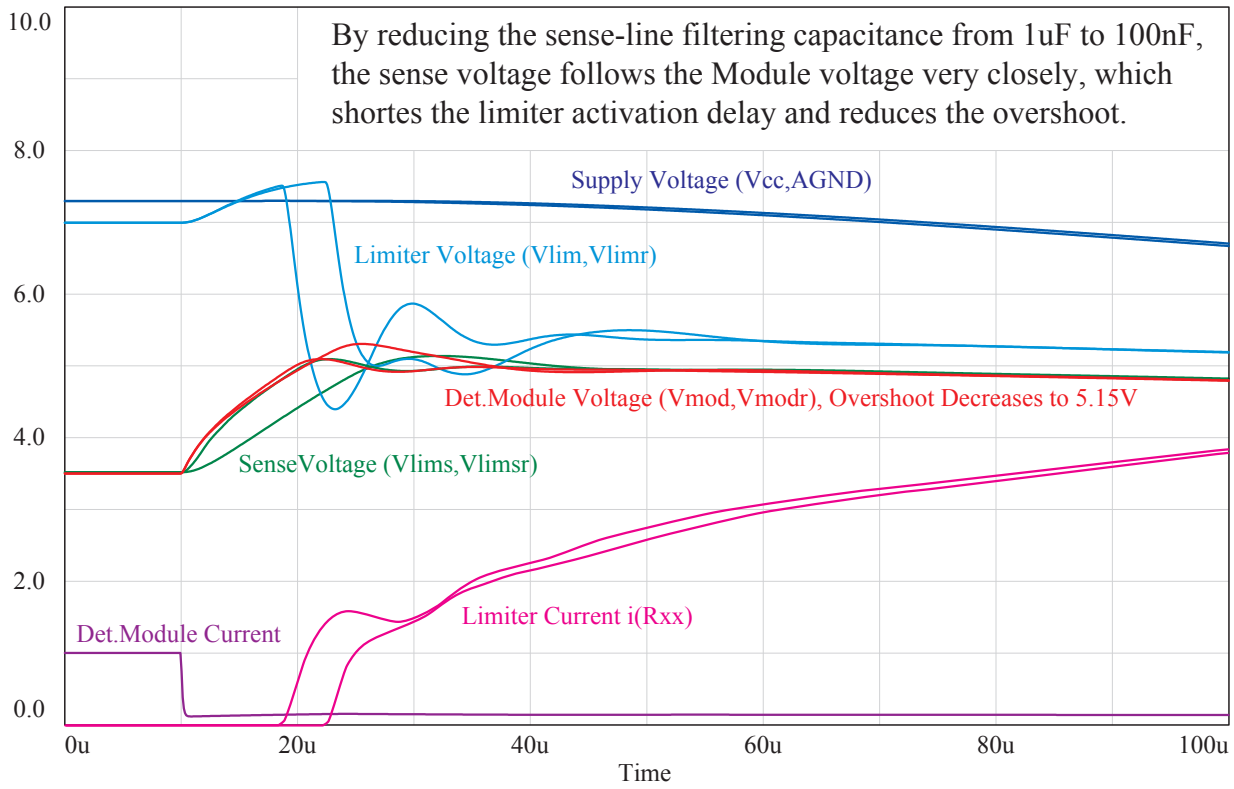

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Fig. 9 : Limiter At PP3, With Load Current Cutoff Slope Extended to 70us

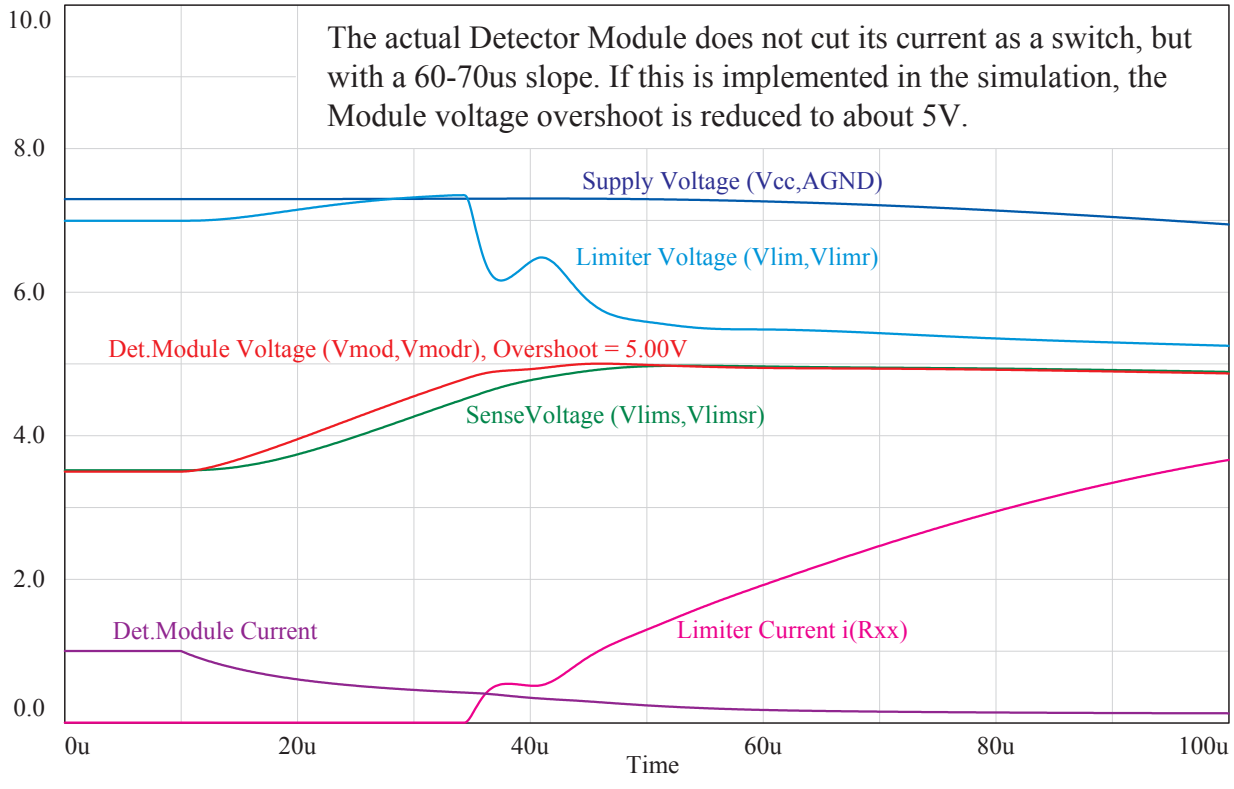

Fig.10 : Limiter At PP3, With The Operating Voltage Increased From 3.5 to 4.0V

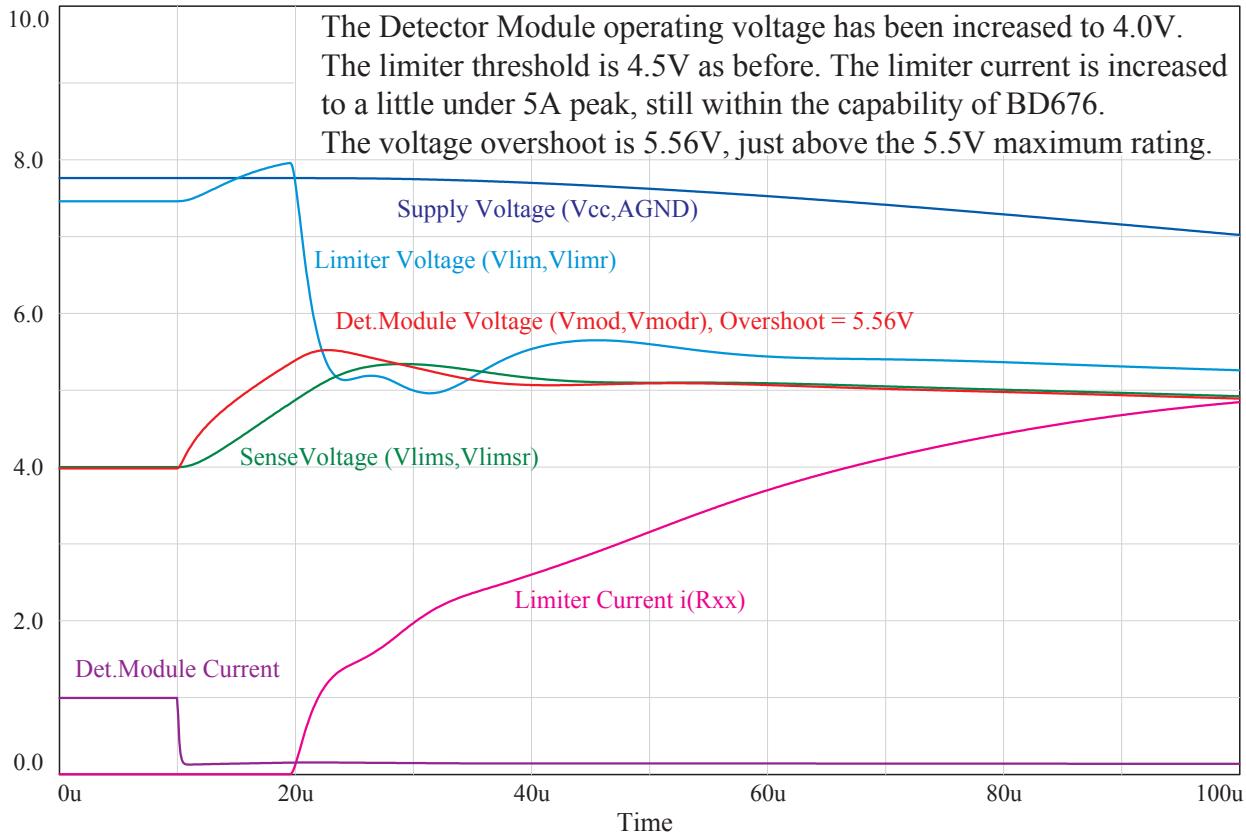

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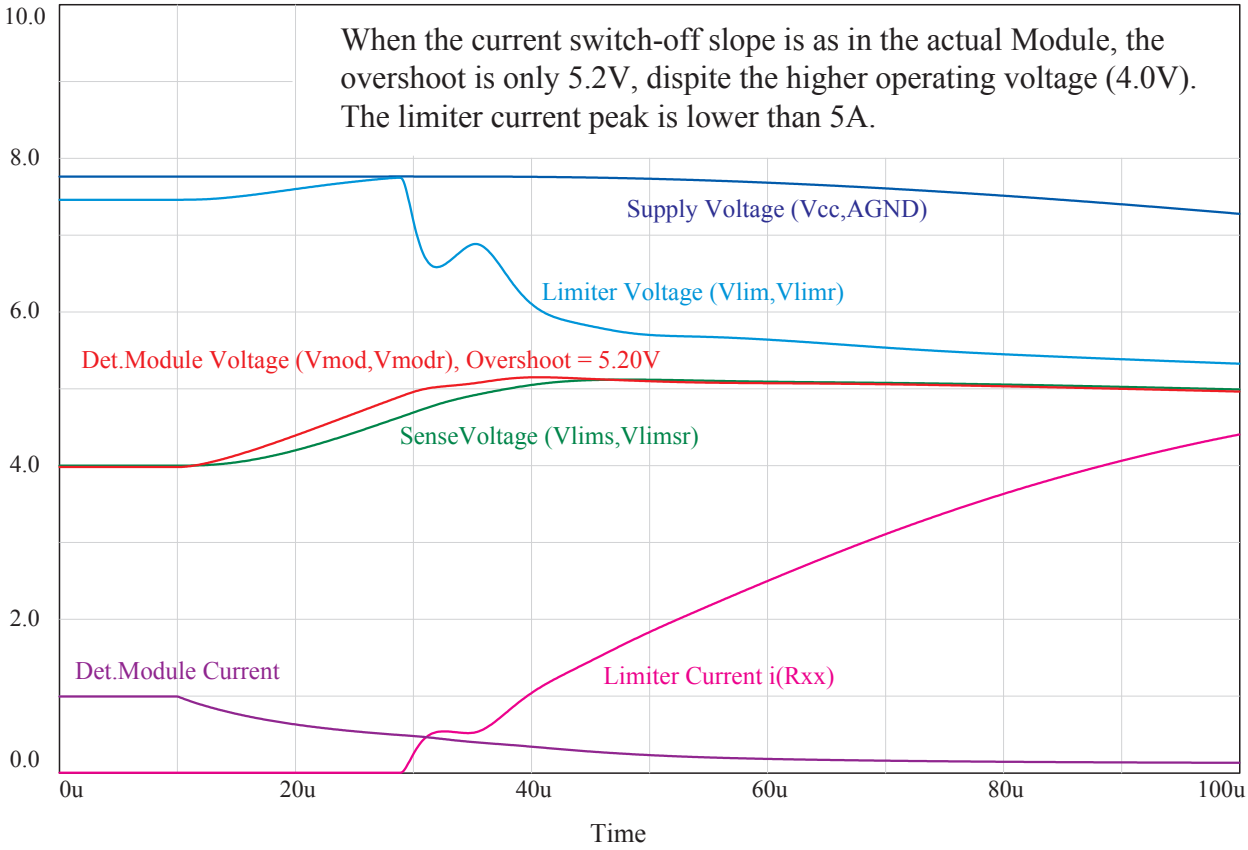
Fig. 11 : Limiter At PP3, Operating Voltage 4.0V, Switch-off Current Slope Decreased



Appendix : Limiter Feedback Loop Frequency Compensation

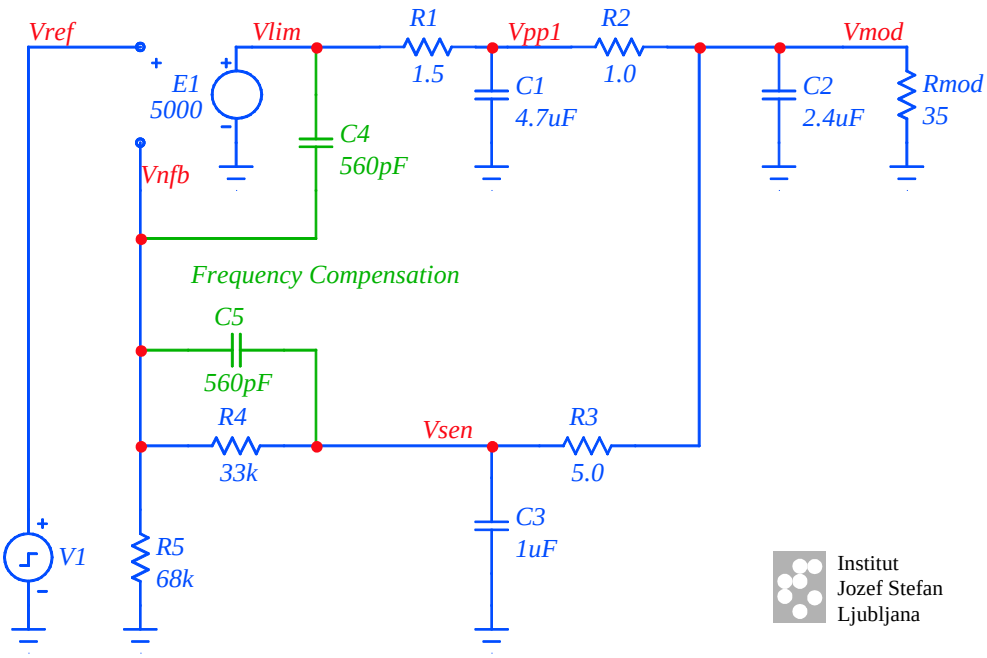


Fig. A1 : Limiter feedback loop model used for the study of frequency compensation

The limiter feedback loop model is shown in **Fig. A1**. The minimum gain of the TI shunt regulator TL431, driving the PNP darlington transistor BD676 and loaded with the low-resistance cable to the PS unit, was estimated to about :

$$A = 5000 \tag{1}$$

The circuit equations for various nodes, from which the system transfer function is derived, neglecting for a while the frequency compensation capacitors C_4 and C_5 , are :

$$V_{\text{lim}} = A\,(V_{\text{ref}} - V_{\text{nfb}}) \tag{2}$$

$$V_{\text{nfb}} = \beta\, V_{\text{sen}} \qquad \text{where} \qquad \beta = \frac{R_5}{R_4 + R_5} \tag{3}$$

$$V_{\text{sen}} = V_{\text{mod}} \frac{1}{1 + sC_3R_3} \tag{4}$$

The loading of V_{sen} by $R_4 + R_5$ can be neglected here. The V_{mod} node can be analyzed from the current summing :

$$\frac{V_{\text{PP1}} - V_{\text{mod}}}{R_2} = V_{\text{mod}}\, sC_2 + \frac{V_{\text{mod}}}{R_{\text{mod}}} + \frac{V_{\text{mod}} - V_{\text{sen}}}{R_3}$$

but when the Detector Module current is cutoff and the limiter threshold is exceeded, R_{mod} can be assumed to be high (infinite in worst-case, regarding the loop delay) :

$$V_{\text{PP1}} = V_{\text{mod}}\left(sC_2R_2 + 1 + \frac{R_2}{R_3}\right) - \frac{R_2}{R_3}V_{\text{sen}} \tag{5}$$

$$V_{\text{lim}} = V_{\text{PP1}}\left(sC_1R_1 + 1 + \frac{R_1}{R_2}\right) - \frac{R_1}{R_2}V_{\text{mod}} \tag{6}$$

We "close the loop" and derive the system transfer function form V_{ref} to V_{mod} :

$$\frac{V_{\text{mod}}}{V_{\text{ref}}} = \frac{A}{1+A\beta} \cdot \frac{C_3R_3\left(s + \dfrac{1}{C_3R_3}\right)\dfrac{1+A\beta}{C_1C_2C_3R_1R_2R_3}}{s^3 + s^2K_1 + sK_2 + \dfrac{1+A\beta}{C_1C_2C_3R_1R_2R_3}} \tag{7}$$

where :

$$K_1 = \left[\frac{1}{C_3R_3} + \frac{1+\dfrac{R_1}{R_2}}{C_1R_1} + \frac{1+\dfrac{R_2}{R_3}}{C_2R_2}\right] \tag{8}$$

and :

$$K_2 = \left[\frac{1}{C_2C_3R_2R_3} + \frac{1+\dfrac{R_1}{R_2}}{C_1C_3R_1R_3} + \frac{1+\dfrac{R_1}{R_3}+\dfrac{R_2}{R_3}}{C_1C_2R_1R_2}\right] \tag{9}$$

Obviously from (7), the system gain is :

$$G = \frac{A}{1+A\beta} \approx \frac{1}{\beta} \tag{10}$$

and the system has a real zero at :

$$s_{\text{z}} = -\frac{1}{C_3R_3} \tag{11}$$

The remaining part of the equation can be compared to the normalized general third-order system :

$$F(s) = \frac{\omega_{\text{o}}^3}{s^3 + as^2 + bs + \omega_{\text{o}}^3} \tag{12}$$

and from this it is evident that the system has a characteristic resonant frequency at :

$$\omega_{\text{o}} = \sqrt[3]{\frac{1+A\beta}{C_1C_2C_3R_1R_2R_3}} \tag{13}$$

By comparing the characteristic polynomial of (12) with its pole-product expression, we can derive the system poles :

$$s^3 + as^2 + bs + \omega_{\text{o}}^3 = (s-s_1)(s-s_2)(s-s_3) \tag{14}$$

Now we can examine the influence of the frequency compensation capacitors, C_4 and C_5 . C_4 provides local negative feedback to the gain block at high frequencies, so we can assume the gain A to vary with frequency as :

$$A(s) = A_{\text{dc}} \frac{\frac{1}{C_4 R_R}}{s + \frac{1}{C_4 R_R}} \tag{15}$$

where R_R is the real part of the loop impedance at the negative feedback input. Similarly, the high branch of the feedback divider is bypassed by C_5, so we can write :

$$\frac{V_{\text{nfb}}}{V_{\text{sen}}} = \frac{R_5(1 + sC_5R_4)}{R_4 + R_5(1 + sC_5R_4)} = \beta(s) \tag{16}$$

By inserting $A(s)$ and $\beta(s)$ in place of A and β in (7) we get the compensated system transfer function. The influence of the compensation on the frequency response can be seen in **Fig. A2**.

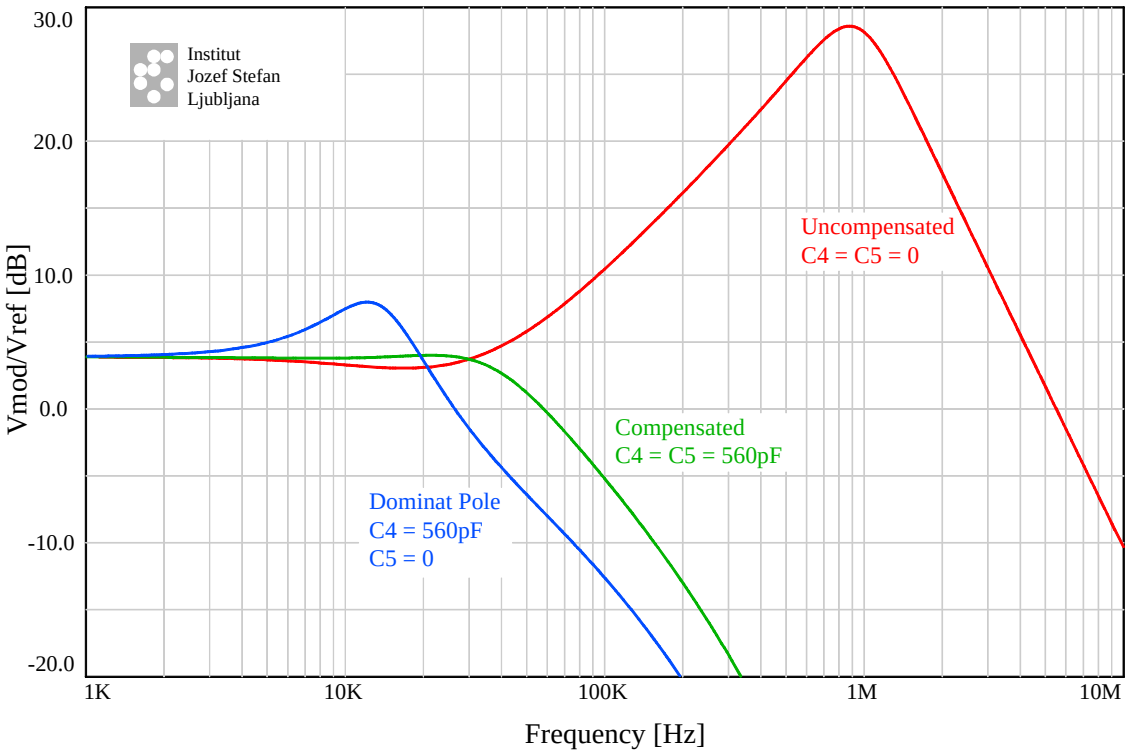


Fig. A2 : Feedback loop frequency-response peaking compensation. The uncompensated circuit has a high resonance peak which can lead to instability and oscillations. If only the dominant-pole compensation scheme is used, the circuit bandwidth is too low and there is still a peak in the frequency-response. The correct compensation with both dominant pole and a phase-leading zero gives a maximally flat response and improves the bandwidth.