Project Specification
Project Name: CAFE-P
Version: 4.01

Revision History

Revision	Change Description, Pages Revised	Engineer in Charge	Date Approved
0.00	Initial draft version.		
0.01	Additions; cleanup for prelim review.		21-Jul-96
1.00	First approved version; Detector parameters finalized; Description of cal circuit complete. pp. 2, 3, 5, 6, 7, 8, 9.	I. Kipnis, N. Spencer	8-Sep-96
2.02	Cleanup for pre-fab design review; Block diagrams added. pp. 7, 8, 9, 14, 15, 16, 17, 18, 19-22.	I. Kipnis, N. Spencer	4-Feb-97
3.00	Pad layout fixed after fab submission; Power Supply Rejection Ratio added; Gain sensitivity to Vcc added. pp. 7, 18, 19-21, 23.	I. Kipnis, N. Spencer	19-Sep-97
3.01	Correct CALSP, CALSN values. p. 6.	N. Spencer	23-Oct-97
4.00	Changed to p-strip detector (new IC name: CAFE-P); adjust min. output signal size; improvements for post-rad matching. pp. 2, 4, 5, 6, 7, 8, 9, 12, 18, 19, 23.	N. Spencer	2-Sep-98
4.01	Changes at second submission: Improve description of VISET; New voltage spec for VISET; New spec for Output Signal amplitude; Add Output Signal Bias Requirement; Corrections to Figure 1; Modify Figure 4 for new ABC DAC; Add test pads to Table 1; New pad layout and chip size in Figure 5 and Table 2; pp. 3, 7-8, 9, 13, 16, 17, 18, 19-21.	N. Spencer	13-Jan-99

1. Scope:

Establish the requirements and the target design specifications for the Front-end Bipolar Amplifier/Discriminator Integrated Circuit to be used as part of the Binary Readout of the ATLAS Semi-Conductor Tracker (SCT). This design is based upon previous work, in particular TekZ IC used in the DESY ZEUS experiment, the FABRIC IC used in the CERN NA50 experiment and the LBIC and CAFE prototype ICs. The CAFE-M was designed for fabrication by Maxim to this specification. The design is now modified to accomodate p-strip detectors (old version for n-strip) and to enhance performance, especially the post-irradiation channel-to-channel matching. New chip is called CAFE-P.

2. Reference Documents:

1) Specification for the Atlas Binary Chip (ABC), 1996.
2) I. Kipnis, "CAFE: A complementary Bipolar Analog Front End Integrated Circuit for the ATLAS SCT", 1995.
3) E. Spencer, et al., "A Fast Shaping Low Power Amplifier-Comparator Integrated for Silicon Strip Detectors", IEEE Nuclear Science Symposium, 1994, (SCIPP 94/32)
4) W. Dabrowski, et al., "Fast Bipolar Front-end for Binary Readout of Silicon Strip Detectors", Nuclear Instruments and Methods A 350 (1994), 548
5) I. Kipnis, et al., "An Analog Front-end Bipolar-transistor Integrated Circuit for the SDC Silicon Tracker," IEEE Transactions on Nuclear Science, vol. 41, no. 4, (1994), 1095-1103.
6) E. Barberis, et al., "A Fast Shaping Amplifier-Comparator Integrated Circuit for Silicon Strip Detectors", IEEE Nuclear Science Symposium, 1992, (SCIPP 92/40)
7) "Silicon Tracker Conceptual Design Report", SCIPP 92/04.
8) H. Spieler, "Electronics Baseline Specification - Recap and Postscript", Minutes of SDC Silicon Tracker Meeting at LBL, 16-Dec-92.
9) J. Leslie, A. Seiden, Y. Unno, "Signal Simulations for Double-sided Silicon Strip Detectors", SCIPP 92/20.
10) H. Spieler, "Rate of Noise Hits in Threshold Discriminator Systems", unpublished note.
11) H. Spieler, "Some Comments on Specifications for Front-End Electronics in the SDC Silicon Tracker", unpublished note.

3. Technical Aspects:

3.1 Requirements

3.1.1 An Integrated Circuit (IC) to process signals from 128 p-type strips of a Silicon Micro-strip Detector. An outline schematic of the IC is shown in Figure 1.

3.1.2 Signal Processing (See block diagram in Figure 2):

The IC must contain the following functions:

Charge integration
Pulse shaping
Threshold/timing discrimination

The result of the discrimination function, indicating a "hit" or "no hit" for each strip, is output from this IC to another circuit for further digital processing. This IC will have one independent channel to process signals from each silicon strip of the detector. Signals from each detector strip will be received at single-ended Sensor Input pads IN0..INn and results appear at single-ended Output pads OUT0..OUTn. Two reference current outputs OUTRH and OUTRL are provided as well as a ground return DRET for the output current.

A control input (VISET) is provided to set the operating current of the input transistor. A current must be supplied at this input with care for appropriate noise filtering. The current is now mirrored internally to allow a reasonable positive compliance at the pad. The nominal current range specified in 3.2.3.3 should be adjusted to optimize noise under pre- and post-radiation conditions.

The threshold value is provided either as a differential voltage from an external source (VTHP, VTHN) or as a programmable current from the adjoining digital processing IC (ITH) as selected by the pad VTSEL. See 3.2.3.7 for more details.

3.1.3 Compatibility:

The design of this IC and that of the digital processing IC, ABC, must be compatible so that they can work together as a chip set. This compatibility of design includes the interface circuits (128 data signals with references, the calibration and threshold controls and the DAC reference) and the corresponding bonding pad locations.

3.1.4 Calibration Circuitry (See block diagram in Figure 3):

Each channel will have an internal Calibration Capacitor connected to its input for purposes of simulating a "hit" strip. The Calibration Capacitors will be charged by a chopper circuit which is triggered by an independent differential input Calibration Strobe (CALSP, CALSN). Every fourth channel can be tested simultaneously with group selection determined by two binary coded Calibration Address inputs (CALD0, CALD1). These strobe and selection signals are expected to originate in the accompanying digital processing IC which is acting on commands from the experiments control system. The voltage applied to the Calibration Capacitors by the chopper is determined by a single differential DC Calibration Level input voltage (CALVP, CALVN) or as a single programmable current from the adjoining digital processing IC (CALI). See 3.2.3.9 for more details. The four calibration bus lines, each of which connects the calibration capacitors of every fourth channel, are also brought out to pads on each side of the IC (CBUS0, CBUS1, CBUS2, CBUS3) which can be directly driven with an AC coupled voltage step. This is intended for use during IC testing.

3.1.5 DAC Reference Circuit (See block diagram in Figure 4):

The adjoining digital processing IC will contain digital-to-analogue converters (DACs) to supply programming currents for the Comparator Threshold and the Calibration Level. It is assumed that these DACs will scale down a reference current supplied by this bipolar IC according to values programmed via commands from off-detector. One reference current will be generated via a band-gap reference circuit. The derived reference current and the voltages derived from the returned currents programmed by the DACs will depend upon resistors on this bipolar chip in order to maintain process independent scaling.

3.2. Specification of Deliverables:

3.2.1 Physical Requirements:

Number of amp/comparator channels per IC: 128

Physical Layout: See Figure 5.

Pad Layout:

Sensor Inputs on front edge.
Comparator Outputs on back edge
Service (power, ground, references) on side edge (reflected on both sides)
Threshold Inputs on back edge (current mode, including reference current)
and also on side edge (differential voltage mode, reflected on both sides)
Calibration Strobe & Address Inputs on back edge near corners
Calibration Amplitude Inputs on back edge (current mode)
and also on side edge (differential voltage mode, reflected on both sides)
Output logic high and low reference current on back edge

Sensor Input Pad Pitch: = 48 μm, 2 rows @ 96 μm pitch each offset at 48 μm to each other

Output Pad Pitch: = 40 μm, 3 rows @ 120 μm pitch each offset at 40 μm.

Pad Size (nominal):

Sensor Inputs:	140 x 60 μm
Outputs:	140 x 60 μm
Service: (Vcc, GND)	190 x 92 μm
(Other Service on side edge)	92 x 92 μm
Service on front and back edge:	140 x 60 μm

Total Chip Width: $\geq$ 6.4 mm, $\leq$ 6.6 mm after sawing and including all bond pads.

Total Chip Length: $\geq$ 3.5 mm, $\leq$ 4.5 after sawing and including all bond pads. (Minimize total area to improve cost.)

Channels must be laid out in parallel to meet electrical requirements.

Services like power, ground and voltage references must be bussed across chip with pads on both sides to allow bonding on either side. The SSGND pads must be bonded on both sides of the IC to equalize voltage drop across the IC. It would ease the IC layout if the services were required to be bonded on both sides rather than on either side. This should be studied further with the hybrid designers.

Critical service pads (e.g. Vcc, GND) are made double width to allow double wire bond for improved reliability.

3.2.2 Assumed Detector Electrical Characteristics at Input to this IC from p-type 12 cm long strips:

	Unirradiated	Irradiated
Coupling type to amplifier	AC	AC
Coupling capacitance to amp Total for 12 cm strips	20 pF/cm 240 pF	20 pF/cm 240 pF
Capacitance of strip to all neighbor strips	0.92 pF/cm	0.92 pF/cm
Capacitance of strip to backplane	0.28 pF/cm	0.28 pF/cm
Metal strip resistance	15 Ω/cm	15 Ω/cm
Bias Resistor	0.75 MΩ	0.75 MΩ
Max leakage current per strip for shot noise	2.0 nA	2.0 μA

AC characteristics for a detector signal are shown in Figure 6 and Table 3 for an irradiated n-strip detector. An inverted version of the same signal shape will be used for simulation now that the we have switched to p-strip detectors. We don't really know what a p-strip signal looks like before and after irradiation at the extreme bias values planned to be used. The assumption is that sufficient detector bias bill be applied to achieve necessary charge collection time.

3.2.3 Electrical Requirements:

Note that notation convention for currents used in the entire specification is "+" for current going into (sunk by) the chip and "-" for current going out of (sourced from) the chip.

3.2.3.1 Sensor Input Characteristics:

Input Signal Polarity: Positive signals from p strips.

Crosstalk: < 5% (with detector)

Input Protection: Must sustain voltage step of 300 V of either polarity with a cumulative charge of 5 nC in 15 ns.

Open Inputs: Any signal input can be open without affecting performance of other channels.

Max Parasitic Leakage Current: 100 nA DC per channel with < 10 % change in gain at 1 fC input charge.

3.2.3.2 Calibration Input Characteristics:

The digital signal processing IC, ABC, must provide the following inputs for the Calibration Circuit. See 3.2.3.9 for functional specifications of the Calibration Circuit.

Two single ended logic inputs CALD1, CALD0 to select one of four groups of channels to test.

	Min	Nominal	Max
"1" State Level	2.9 V	4 V	4.2 V
"0" State Level	0 V	0 V	0.5 V
Current			100 µA
Rise Time			10 ns
Duration		DC	

One pair of Calibration Strobe inputs CALSP, CALSN which form one signal to activate the Calibration circuitry. The CALSP input is normally in the "Off" state and the CALSN input is normally in the "On" state when the Calibration Strobe is idle. During an active Calibration Strobe, CALSP goes to the "On" state and CALSN goes to the "Off" state. It is expected that these inputs are driven by a complementary driver:

	Min	Nominal	Max
"On" State Current at 0.7 V Nom (each input)	- 180 µA	- 240 µA	- 300 µA
"Off" State Current	- 15 µA		- 30 µA
Voltage Range (either state)	Vcc-0.9V		Vcc-0.6V
Rise Time			4 ns
Duration	125 ns		
Delay after transition of CALD1,CALD0	250 ns		
Off interval between consecutive pulses	250 ns		

Calibration Level: See DC Supply and Control Characteristics

3.2.3.3 DC Supply and Control Characteristics:

The following DC inputs are required for 128 channels with voltage specifications listed on this page and current specifications on the following page. Differential pairs are grouped together.

		Operational Values			Absolute
	Pad Name	Min	Nominal	Max	Max
Circuit Supply	Vcc	3.325 V	3.5 V	3.675 V	0 to 6 V
Preamp Current Control *	VISET	0 V (off)	1 to 1.3 V	1.6 V	Vcc
Small Signal Ground	SSGND		0 V		
Circuit Ground	GND		0 V		
Digital Ground Return	DRET	-100 mV	0 V	100 mV	-500 mV
Comparator (voltage) Threshold (Vthp - Vthn)	VTHP	3.1 V	Vcc	Vcc+.3V	Vcc+.5V
	VTHN		VTHP-.2V		Vcc+.5V
			0.2 V	0.9 V	0 to 2 V
Comparator (current) Threshold *	ITH	Vcc - 1.2 V			Vcc
Threshold Select (for voltage mode)	VTSEL	Vcc - 0.5 V		Vcc	Vcc
Calibration (voltage) Level (diff. pair) (CALVP - CALVN) (Equiv. Sensor Input Charge)	CALVP	1.2 V		2.8 V	Vcc
	CALVN	1.2 V		2.8 V	Vcc
		50 mV (.5 fC)		1 V (10 fC)	2.0 V
Calibration (current) Level *	CALI	1.0 V		2.4 V	Vcc
DAC Reference Current (Output source; not input)	IDAR	1.8 V			Vcc

* These are current, not voltage, sourced inputs.

Special Requirements (Not design targets but simulation results):

Gain Sensitivity to Vcc for 1 fC signal (As measured at input to comparator) — See Figure 7

Power Supply Rejection Ratio at:	10 Hz - 100 Hz	50 dB
	10 kHz - 100 kHz	20 dB
	1 MHz - 100 MHz	-14 dB

The current draw at each DC input is as follows. Maximums assume -14 % resistor production skew and Max Vcc. The notation convention for currents is "+" for current going into (sunk by) the chip and "-" for current going out of (sourced from) the chip.

		Min	Nominal	Max
Circuit Supply	Vcc			
For I(VISET)=200 µA	(post rad)			67 mA
For I(VISET)=300 µA	(pre rad)		74 mA	81 mA
Preamp Current Control	VISET		.15 to .3 mA	.5 mA
Small Signal Ground	SSGND			
For I(Vi1)=150 µA			23 mA	23 mA
For I(Vi1)=300 µA			45 mA	45 mA
Circuit Ground	GND		22 mA	27 mA
Digital Ground Return	DRET		1 mA	
Comparator (voltage) Threshold	VTHP		12 µA	15 µA
	VTHN		12 µA	15 µA
Current Balance	|I of VTHP - I of VTHN|			
Comparator (current) Threshold	ITH	- 3 µA		- IDAR
Threshold Select	VTSEL		50 µA	60 µA
Calibration (voltage) Level	CALVP			1 µA
	CALVN			1 µA
Current Balance	|I of CALVP - I of CALVN|			10 %
Calibration (current) Level	CALI	+ 15 µA		IDAR
(Equiv. Sensor Input Charge)		(.5 fC)		(10 fC)
DAC Reference Current (Output source; not input)	IDAR		+ 324 µA	+ 363 µA

3.2.3.4 Signal Output Characteristics:

Assumed type of logic of receiving stage: edge triggered

Output configuration: open collector output of npn transistor as a current source.

	Min	Nominal	Max
"Off" State Current	0 µA		10 µA
"On" State Current	120 µA	160 µA	180 µA
Output Bias Requirement ("On" or "Off" State)	0.7 V		4.0 V
Bias variation between outputs (including OUTRH & OUTRL)			0.5 V
Pulse Duration			
for 1.25 fC	8 ns		
for 3.50 fC			44 ns

Open Outputs: Any signal output can be open without affecting performance of other channels.

Output Reference pad named OUTRH: DC current equal to that of "On" state of normal outputs.

Output Reference pad named OUTRL: DC current equal to that of "Off" state of normal outputs.

3.2.3.5 Power Dissipation:

Power use will be minimized for this design.

Total Average Power simulated for 3 cases:

Nominal: (nom fab skew, nom Vcc, VISET=300µA, Cal at 4 fC)	260 mW
Worst Case: (low resisitor fab, Max Vcc, VISET=300µA, Cal at 10 fC)	300 mW
Post Rad Worst Case: (low resistor fab, Max Vcc, VISET=200µA, Cal at 10 fC)	250 mW

3.2.3.6 Noise:

Maximum rms. noise for nominal components including contributions from:
a) All detector parameters listed in 3.2.2
b) Two neighboring channels (one on each side): 3 channel simulation
will be: <= 1400 electrons for unirradiated module
<= 1500 electrons for irradiated module

Noise analysis predicated on worst case p-strip signal assuming the front-end ICs are wire bonded at the center of the 12 cm detector strips. For the time being, an inverted n-strip signal as shown from simulation of depleted detector signal in Figure 6 and Table 3 will be used until the expected p-strip signal is understood.

3.2.3.7 Comparator Stage:

A threshold is applied as a voltage offset to the comparator stage.

Threshold setting range: 0.5 fC to 5 fC, nominal 1 fC

This threshold voltage is applied externally either as a differential voltage or as a current. The unused inputs must be left floating. A pad VTSEL on the side of the chip must be bonded to Vcc to use the voltage mode or left floating to use the current mode.

For voltage mode, typical externally applied differential threshold voltage to establish nominal threshold of 1 fC: ~ 190 mV (150 mV/fC + offset)

For current mode, a reference current (IDAR) is sunk as output expecting a programmable scaled current supplied as a threshold input (ITH). It is expected that the reference current will be scaled into 256 programmable linear steps to provide the necessary precision. Resulting step size near 1 fC threshold should correspond to ~0.025 fC of input charge. Typical externally supplied current to establish nominal threshold of 1 fC: ~ 60 μA.

Threshold variation at 1 fC:
4% (1 sigma) channel to channel matching within one chip
20% (1 sigma) including all process variations

3.2.3.8 Timing Requirements:

Timewalk: <= 16 ns. This specification depends on the precision of the digital acquisition latch edge. Good alignment, 1 or 2 ns over a common clocked array of channels implies a longer timewalk assignment to the rising edge of the shaped signal.

Timewalk defined: The maximum time variation in the crossing of the time stamp threshold over a signal range of 1.25 to 10 fC, with the comparator threshold set to 1 fC according to 3.2.3.7.

Double Pulse Resolution: <= 50 ns for a 3.5 fC signal followed by a 3.5 fC signal, including a 6 ns off state of Output between pulses.

Max recovery time for a 3.5 fC signal following a 80 fC signal: 1 μs

3.2.3.9 Calibration Circuit Characteristics:

Calibration Capacitors: 100 fF +- 20% (3 sigma) over full production skew
+- 2% (3 sigma) within one chip

Absolute accuracy of voltage step applied to capacitors: 5% (full process skew)

Relative accuracy of voltage step: < 2 %
(for known values of calibration capacitors, amplitude range 0.8 to 4 fC, across one chip, including non-linearity of differential receiver, switching pickup, etc.)

Relative accuracy of voltage step: < 10 %
(for known values of calibration capacitors, amplitude range 0.8 to 8 fC, across one chip, including non-linearity of differential receiver, switching pickup, etc.)

Calibration circuit must be laid out such that Calibration Strobe signal pickup at comparator will be less than 0.3 fC equivalent sensor input.

The calibration amplitude is established externally either as a differential voltage or as a current. The unused inputs can be left floating or grounded

For voltage mode, typical externally applied differential voltage will correspond linearly to roughly 100 mV/fC of equivalent input charge up to 1 V

For current mode, the same reference current (IDAR) used for threshold control will be available expecting a programmable scaled current supplied as a calibration level input (CALI). It is expected that the reference current will be scaled into 256 programmable linear steps to provide the necessary precision. Typical externally supplied current will correspond linearly to roughly 30 μA/fC of equivalent input charge up to 300 μA. Linearity will be < 1 % in the range 0.5 fC to 2 fC and < 4 % in the range 2 fC to 10 fC.

For test purposes, a voltage step can be applied directly to any one of the four groups of calibration capacitor via the input pads (CBUS0, CBUS1, CBUS2, CBUS3). Such an external voltage step must be AC coupled. When not used, these four pads must be left floating.

4. Quality Assurance:

4.1 Specification Review:

This specification and all revisions will be approved by the selected Review Committee for appropriateness to meet the goals of the detector and integratability with the rest of the subsystem.

4.2 Circuit Simulations:

The design will be simulated to test fulfillment of these requirements before submission to fabrication.

Transient analyses will be performed in which all DC supplies are cycled in random order to verify that no latch up occurs in the circuit.

Behavior will be simulated for variations in supply voltages 25 mV beyond that specified in section 3.2.3.3. Simulations will be done at temperatures of -10 and 25 degrees centigrade.

DC and AC analysis will be performed for 25% of the channels activated using actual metal busses and expected on-chip and off-chip bus impedances.

Sensitivity analysis will be done for all relative process parameters over 3 standard deviations of the expected fabrication distributions to the satisfaction of the review committee listed in 4.3. Circuit parameters will also be varied to simulate circuit performance at initial commissioning and after irradiation of $10^{14}/cm^2$ neutrons and 10 MRad ionization including the respective sets of unirradiated and irradiated detector parameters given in section 3.2.2.

In the sensitivity analysis, < 1% of all channels may deviate from the specification.

4.3 Preliminary Design Review:

The design will be checked and simulations reviewed in detail by at least one engineer other than the circuit designer.

A Data Sheet specific to each prototype design must be submitted and include typical operating values, operating limits and absolute maximum values of supply voltages and currents.

The specific data sheet and simulation results will be reviewed by the Selected Review Committee of this specification before submission to fabrication.

4.4 Intermediate Design Review:

Results of prototype circuits including test data will be reviewed by the Review Committee to verify compliance with these requirements.

4.5 Final Design Review:

Before this circuit is submitted for Production Fabrication, a Final Design Review will be held by the Review Committee. The following data will be reviewed:

Electrical component tests

Electrical tests in assembled modules

Comparisons of tests vs. simulations

Expected yield and performance over process variations from each potential vendor

Reliability data

Irradiation effects

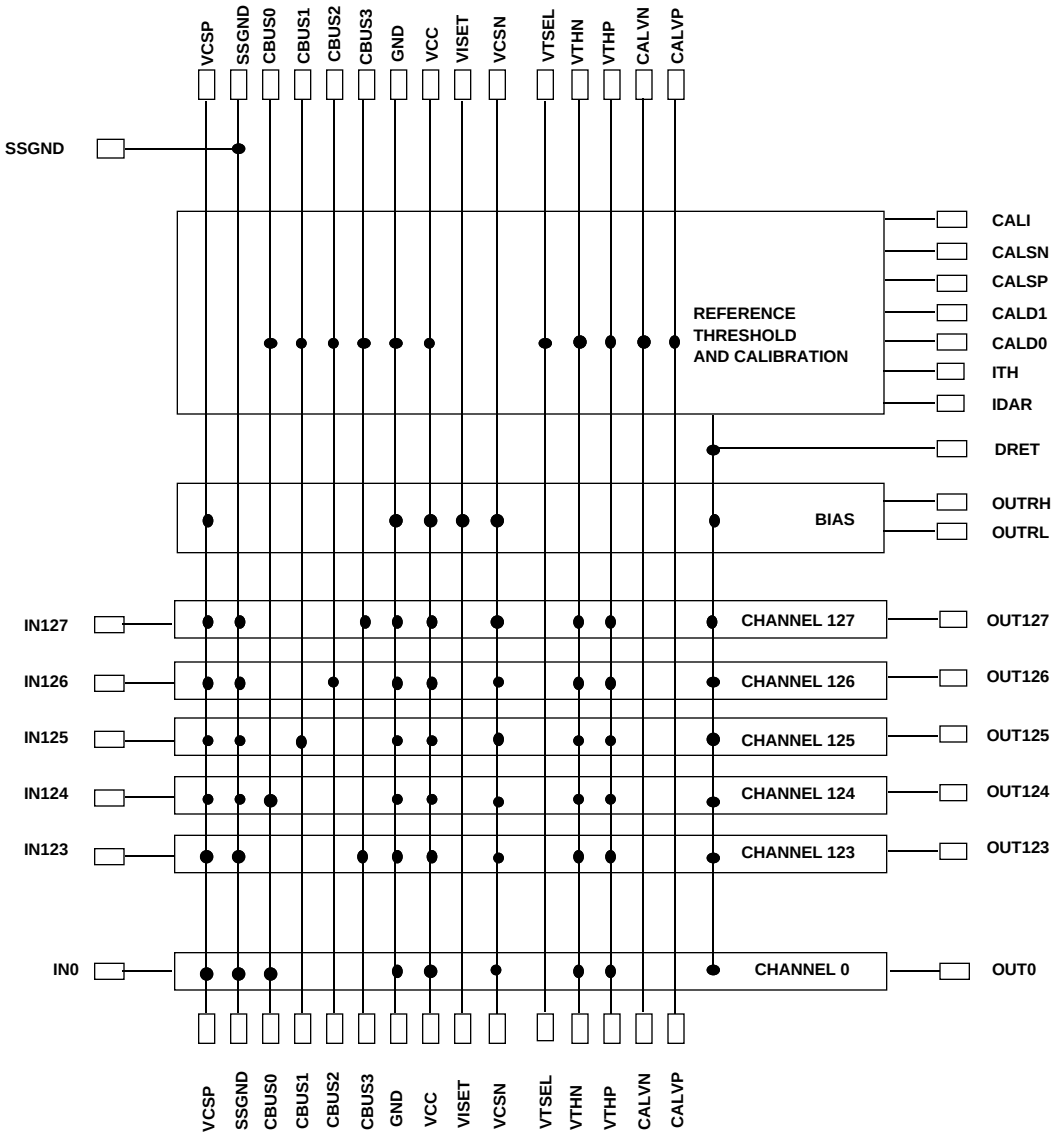

Figure 1: Chip Outline Schematic
Note: This figure shows relationships of input/output signals to circuit blocks and not relative pad positions of the chip layout.

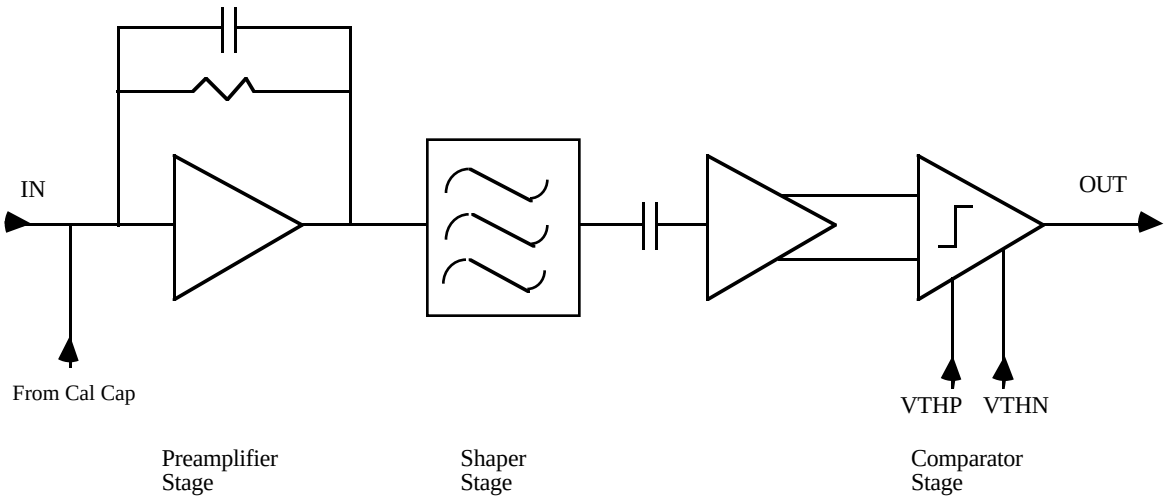

Figure 2: Block Diagram of One Signal Processing Channel

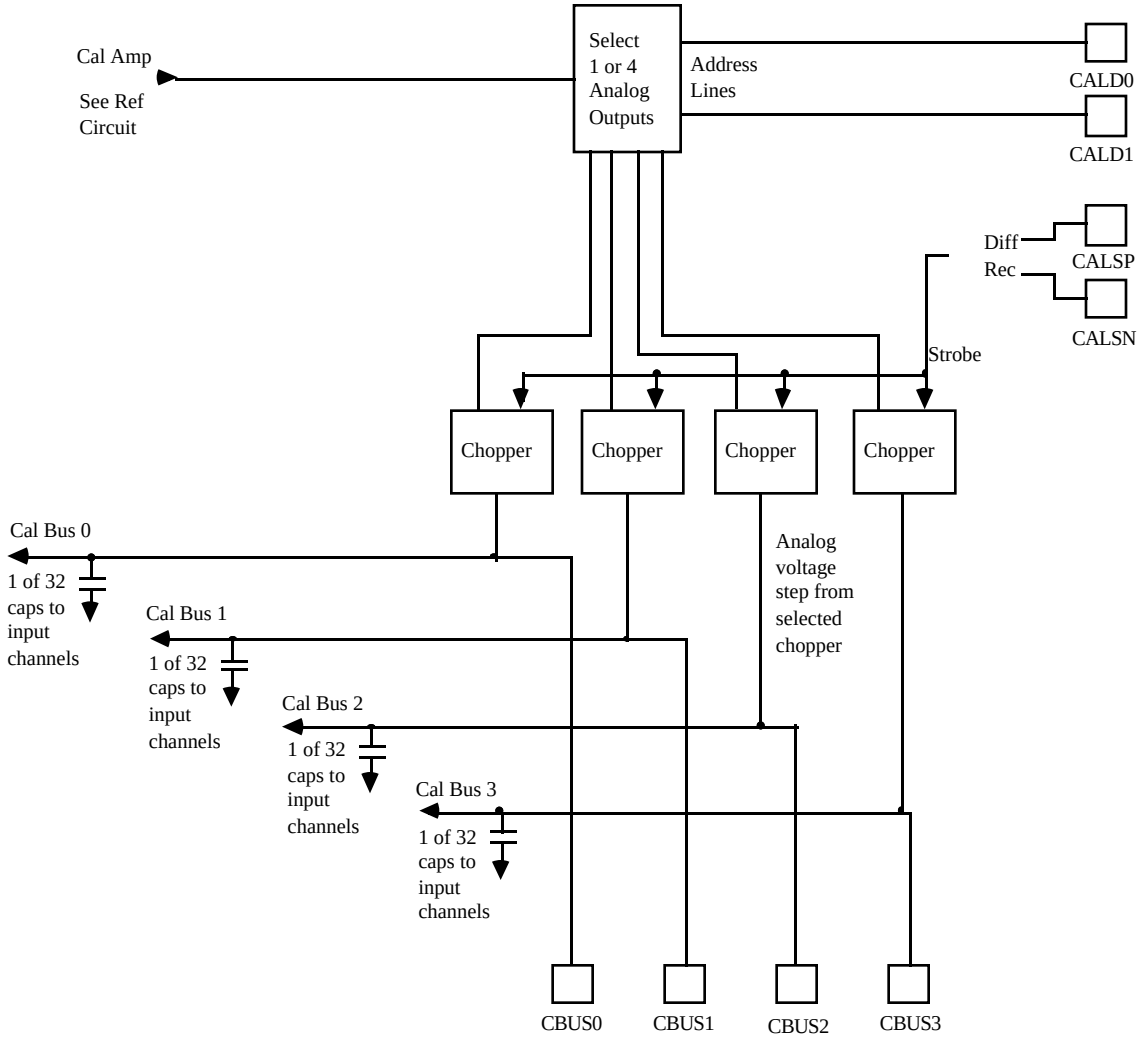

Figure 3: Block Diagram of Calibration Circuitry

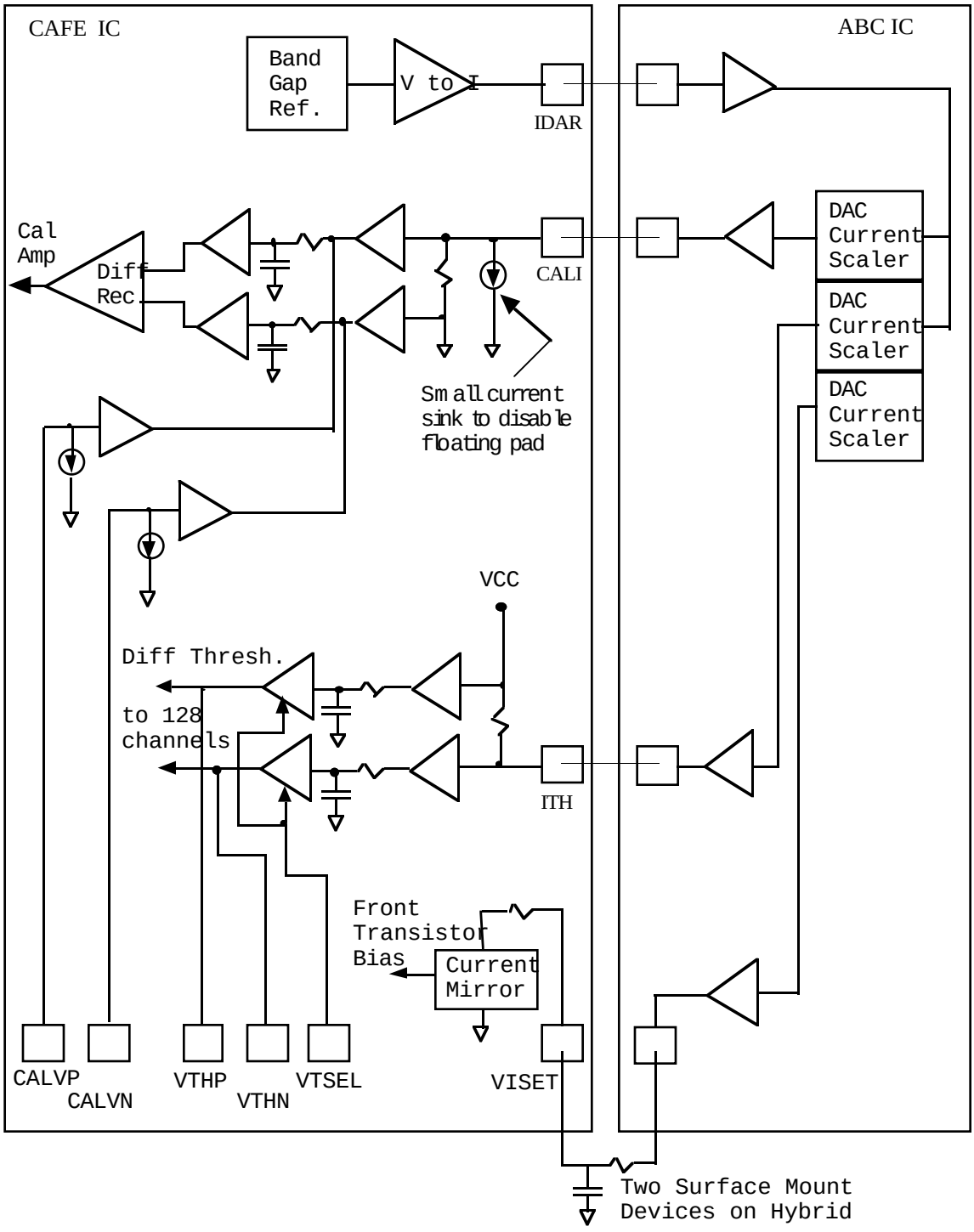

Figure 4: Block Diagram of DAC Reference Circuit

Table 1: Pad List

The following connections are associated with pads intended for conventional wire bonds to hybrid or digital processing IC

IN0 .. IN127	128 input data channels
SSGND	Ground of Strip Detector
OUT0 .. OUT127	128 output data channels
OUTRL	Low output reference current
OUTRH	High output reference current
DRET	Ground return to digital processing IC
Vcc	Chip power
GND	Chip ground
VISET	Bias for front-end transistor
IDAR	Reference current for DACs on digital processing IC
ITH	Current mode threshold control
VTHP	High side of differential voltage threshold control
VTHN	Low side of differential voltage threshold control
VTSEL	Threshold control mode selection
CALI	Current mode calibration amplitude control
CALVP	High side of differential voltage calibration amplitude control
CALVN	Low side of differential voltage calibration amplitude control
CALD0	Address 0 for calibration channels
CALD1	Address 1 for calibration channels
CALSP	High side of calibration strobe
CALSN	Low side of calibration strobe
CBUS0	Calibration Bus #0 for channels 0, 4, .. 124
CBUS1	Calibration Bus #1 for channels 1, 5, .. 125
CBUS2	Calibration Bus #2 for channels 2, 6, .. 126
CBUS3	Calibration Bus #3 for channels 3, 7, .. 127
VCSP, VCSN	Internal bias buses

The following connections are associated with test pads intended for diagnostic testing with pico-probes. Some are simple openings in the passivation layer with circuitry underneath the metal contact point. Conventional bonding to these pads may result in IC failure. Refer to schematics for their exact function.

VCSP2	Internal bias bus
VX, VQ4	Internal bias buses
BFIX	Internal bias bus
VBFIX	Adjusts value of BFIX via series resistor (R29). Load=1.85V
VICOM	Adjusts value of VCSP2 via series resistor (R12). Load=1.85V
BGAP_DIS	Disables band-gap when grounded
STROBE	Calibration strobe to Chopper sub-circuit
STROBEREF	Calibration reference to Chopper sub-circuit
SEL0,1,2,3	Decoded select lines for the four calibration busses
VHIGH, VLOW	Calibration signals to Chopper sub-circuit
P1n	Output of first stage on even channels (Q3 emitter)
P2n	Output of second stage on even channels (Q11 emitter)
P3n	Non-inverting half of signal to comparator on even channels (Q22)
P4n	Inverting half of signal to comparator on even channels (Q23)

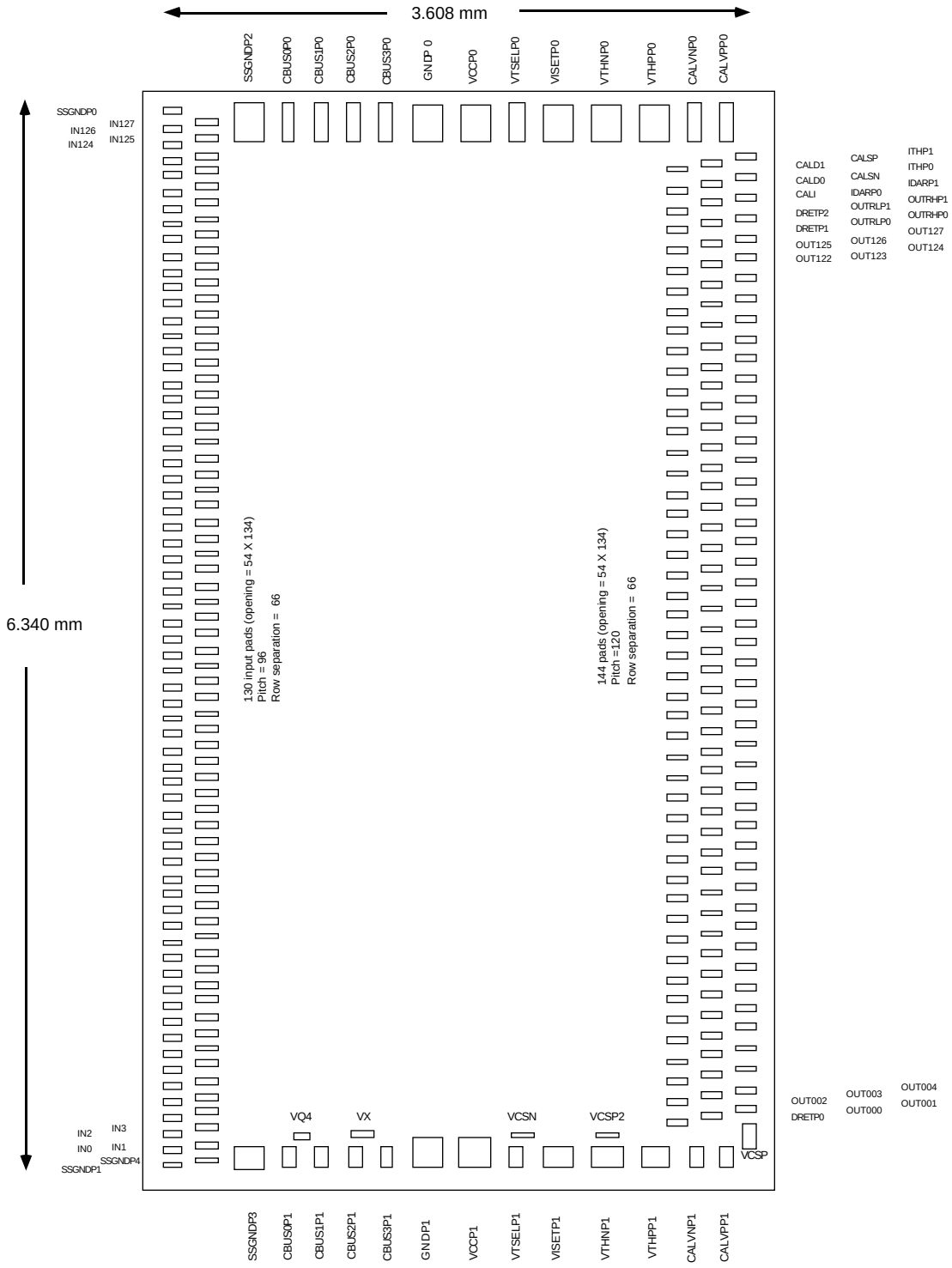

Figure 5: Pad Layout
Overall chip size is extent of digitized area (not including scribe area).
Openings for diagnostic probe points are not all shown.
Note that pad names ending with "Pn" with a numeral n
refer to multiple instances of the same pad connection.

Table 2: Pad Coordinates and Sizes

X, Y Coordinates refer to layout of Figure 5 with X measuring to the right and Y measuring up. The orgin is at lower left corner edge of digitized area.
Pad sizes are for openings in over glass.

Pad #	Name	X-Center	Y-Center	X-Size	Y-Size
1	SSGNDP1	72	32	134	54
2	SSGNDP4	272	76	134	54
3	IN0	72	128	134	54
4	IN1	272	172	134	54
5	IN2	72	224	134	54
6	IN3	272	268	134	54
7	IN4	72	320	134	54
8	IN5	272	364	134	54
9	IN6	72	416	134	54
10	IN7	272	460	134	54
11	IN8	72	512	134	54
12	IN9	272	556	134	54
13	IN10	72	608	134	54
14	IN11	272	652	134	54
15	IN12	72	704	134	54
16	IN13	272	748	134	54
17	IN14	72	800	134	54
18	IN15	272	844	134	54
19	IN16	72	896	134	54
20	IN17	272	940	134	54
21	IN18	72	992	134	54
22	IN19	272	1036	134	54
23	IN20	72	1088	134	54
24	IN21	272	1132	134	54
25	IN22	72	1184	134	54
26	IN23	272	1228	134	54
27	IN24	72	1280	134	54
28	IN25	272	1324	134	54
29	IN26	72	1376	134	54
30	IN27	272	1420	134	54
31	IN28	72	1472	134	54
32	IN29	272	1516	134	54
33	IN30	72	1568	134	54
34	IN31	272	1612	134	54
35	IN32	72	1664	134	54
36	IN33	272	1708	134	54
37	IN34	72	1760	134	54
38	IN35	272	1804	134	54
39	IN36	72	1856	134	54
40	IN37	272	1900	134	54
41	IN38	72	1952	134	54
42	IN39	272	1996	134	54
43	IN40	72	2048	134	54
44	IN41	272	2092	134	54
45	IN42	72	2144	134	54
46	IN43	272	2188	134	54
47	IN44	72	2240	134	54
48	IN45	272	2284	134	54
49	IN46	72	2336	134	54
50	IN47	272	2380	134	54
51	IN48	72	2432	134	54
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54	IN51	272	2572	134	54
55	IN52	72	2624	134	54
56	IN53	272	2668	134	54
57	IN54	72	2720	134	54
58	IN55	272	2764	134	54
59	IN56	72	2816	134	54
60	IN57	272	2860	134	54
61	IN58	72	2912	134	54
62	IN59	272	2956	134	54
63	IN60	72	3008	134	54
64	IN61	272	3052	134	54
65	IN62	72	3104	134	54
66	IN63	272	3148	134	54
67	IN64	72	3200	134	54
68	IN65	272	3244	134	54
69	IN66	72	3296	134	54
70	IN67	272	3340	134	54
71	IN68	72	3392	134	54
72	IN69	272	3436	134	54
73	IN70	72	3488	134	54
74	IN71	272	3532	134	54
75	IN72	72	3584	134	54
76	IN73	272	3628	134	54
77	IN74	72	3680	134	54
78	IN75	272	3724	134	54
79	IN76	72	3776	134	54
80	IN77	272	3820	134	54
81	IN78	72	3872	134	54
82	IN79	272	3916	134	54
83	IN80	72	3968	134	54
84	IN81	272	4012	134	54
85	IN82	72	4064	134	54
86	IN83	272	4108	134	54
87	IN84	72	4160	134	54
88	IN85	272	4204	134	54
89	IN86	72	4256	134	54
90	IN87	272	4300	134	54
91	IN88	72	4352	134	54

92	IN89	272	4396	134	54	146	CALSP	3336	5964	134	54
93	IN90	72	4448	134	54	147	CALD1	3136	5924	134	54
94	IN91	272	4492	134	54	148	ITHP0	3536	5884	134	54
95	IN92	72	4544	134	54	149	CALSN	3336	5844	134	54
96	IN93	272	4588	134	54	150	CALD0	3136	5804	134	54
97	IN94	72	4640	134	54	151	IDARP1	3536	5764	134	54
98	IN95	272	4684	134	54	152	IDARP0	3336	5724	134	54
99	IN96	72	4736	134	54	153	CALI	3136	5684	134	54
100	IN97	272	4780	134	54	154	OUTRHP1	3536	5644	134	54
101	IN98	72	4832	134	54	155	OUTRLP1	3336	5604	134	54
102	IN99	272	4876	134	54	156	DRETP2	3136	5564	134	54
103	IN100	72	4928	134	54	157	OUTRHP0	3536	5524	134	54
104	IN101	272	4972	134	54	158	OUTRLP0	3336	5484	134	54
105	IN102	72	5024	134	54	159	DRETP1	3136	5444	134	54
106	IN103	272	5068	134	54	160	OUT127	3536	5404	134	54
107	IN104	72	5120	134	54	161	OUT126	3336	5364	134	54
108	IN105	272	5164	134	54	162	OUT125	3136	5324	134	54
109	IN106	72	5216	134	54	163	OUT124	3536	5284	134	54
110	IN107	272	5260	134	54	164	OUT123	3336	5244	134	54
111	IN108	72	5312	134	54	165	OUT122	3136	5204	134	54
112	IN109	272	5356	134	54	166	OUT121	3536	5164	134	54
113	IN110	72	5408	134	54	167	OUT120	3336	5124	134	54
114	IN111	272	5452	134	54	168	OUT119	3136	5084	134	54
115	IN112	72	5504	134	54	169	OUT118	3536	5044	134	54
116	IN113	272	5548	134	54	170	OUT117	3336	5004	134	54
117	IN114	72	5600	134	54	171	OUT116	3136	4964	134	54
118	IN115	272	5644	134	54	172	OUT115	3536	4924	134	54
119	IN116	72	5696	134	54	173	OUT114	3336	4884	134	54
120	IN117	272	5740	134	54	174	OUT113	3136	4844	134	54
121	IN118	72	5792	134	54	175	OUT112	3536	4804	134	54
122	IN119	272	5836	134	54	176	OUT111	3336	4764	134	54
123	IN120	72	5888	134	54	177	OUT110	3136	4724	134	54
124	IN121	272	5932	134	54	178	OUT109	3536	4684	134	54
125	IN122	72	5984	134	54	179	OUT108	3336	4644	134	54
126	IN123	272	6028	134	54	180	OUT107	3136	4604	134	54
127	IN124	72	6080	134	54	181	OUT106	3536	4564	134	54
128	IN125	272	6124	134	54	182	OUT105	3336	4524	134	54
129	IN126	72	6176	134	54	183	OUT104	3136	4484	134	54
130	IN127	272	6220	134	54	184	OUT103	3536	4444	134	54
131	SSGNDP0	72	6272	134	54	185	OUT102	3336	4404	134	54
132	SSGNDP2	602	6218	186	234	186	OUT101	3136	4364	134	54
133	CBUS0P0	838	6216	98	238	187	OUT100	3536	4324	134	54
134	CBUS1P0	1030	6216	98	238	188	OUT099	3336	4284	134	54
135	CBUS2P0	1222	6216	98	238	189	OUT098	3136	4244	134	54
136	CBUS3P0	1414	6216	98	238	190	OUT097	3536	4204	134	54
137	GNDP0	1654	6218	186	234	191	OUT096	3336	4164	134	54
138	VCCP0	1934	6218	186	234	192	OUT095	3136	4124	134	54
139	VTSELP0	2174	6216	98	238	193	OUT094	3536	4084	134	54
140	VISETP0	2414	6218	186	234	194	OUT093	3336	4044	134	54
141	VTHNP0	2698	6218	186	234	195	OUT092	3136	4004	134	54
142	VTHPP0	2982	6218	186	234	196	OUT091	3536	3964	134	54
143	CALVNP0	3218	6216	98	238	197	OUT090	3336	3924	134	54
144	CALVPP0	3410	6216	98	238	198	OUT089	3136	3884	134	54
145	ITHP1	3536	6004	134	54	199	OUT088	3536	3844	134	54

200	OUT087	3336	3804	134	54
201	OUT086	3136	3764	134	54
202	OUT085	3536	3724	134	54
203	OUT084	3336	3684	134	54
204	OUT083	3136	3644	134	54
205	OUT082	3536	3604	134	54
206	OUT081	3336	3564	134	54
207	OUT080	3136	3524	134	54
208	OUT079	3536	3484	134	54
209	OUT078	3336	3444	134	54
210	OUT077	3136	3404	134	54
211	OUT076	3536	3364	134	54
212	OUT075	3336	3324	134	54
213	OUT074	3136	3284	134	54
214	OUT073	3536	3244	134	54
215	OUT072	3336	3204	134	54
216	OUT071	3136	3164	134	54
217	OUT070	3536	3124	134	54
218	OUT069	3336	3084	134	54
219	OUT068	3136	3044	134	54
220	OUT067	3536	3004	134	54
221	OUT066	3336	2964	134	54
222	OUT065	3136	2924	134	54
223	OUT064	3536	2884	134	54
224	OUT063	3336	2844	134	54
225	OUT062	3136	2804	134	54
226	OUT061	3536	2764	134	54
227	OUT060	3336	2724	134	54
228	OUT059	3136	2684	134	54
229	OUT058	3536	2644	134	54
230	OUT057	3336	2604	134	54
231	OUT056	3136	2564	134	54
232	OUT055	3536	2524	134	54
233	OUT054	3336	2484	134	54
234	OUT053	3136	2444	134	54
235	OUT052	3536	2404	134	54
236	OUT051	3336	2364	134	54
237	OUT050	3136	2324	134	54
238	OUT049	3536	2284	134	54
239	OUT048	3336	2244	134	54
240	OUT047	3136	2204	134	54
241	OUT046	3536	2164	134	54
242	OUT045	3336	2124	134	54
243	OUT044	3136	2084	134	54
244	OUT043	3536	2044	134	54
245	OUT042	3336	2004	134	54
246	OUT041	3136	1964	134	54
247	OUT040	3536	1924	134	54
248	OUT039	3336	1884	134	54
249	OUT038	3136	1844	134	54
250	OUT037	3536	1804	134	54
251	OUT036	3336	1764	134	54
252	OUT035	3136	1724	134	54
253	OUT034	3536	1684	134	54
254	OUT033	3336	1644	134	54
255	OUT032	3136	1604	134	54
256	OUT031	3536	1564	134	54
257	OUT030	3336	1524	134	54
258	OUT029	3136	1484	134	54
259	OUT028	3536	1444	134	54
260	OUT027	3336	1404	134	54
261	OUT026	3136	1364	134	54
262	OUT025	3536	1324	134	54
263	OUT024	3336	1284	134	54
264	OUT023	3136	1244	134	54
265	OUT022	3536	1204	134	54
266	OUT021	3336	1164	134	54
267	OUT020	3136	1124	134	54
268	OUT019	3536	1084	134	54
269	OUT018	3336	1044	134	54
270	OUT017	3136	1004	134	54
271	OUT016	3536	964	134	54
272	OUT015	3336	924	134	54
273	OUT014	3136	884	134	54
274	OUT013	3536	844	134	54
275	OUT012	3336	804	134	54
276	OUT011	3136	764	134	54
277	OUT010	3536	724	134	54
278	OUT009	3336	684	134	54
279	OUT008	3136	644	134	54
280	OUT007	3536	604	134	54
281	OUT006	3336	564	134	54
282	OUT005	3136	524	134	54
283	OUT004	3536	484	134	54
284	OUT003	3336	444	134	54
285	OUT002	3136	404	134	54
286	OUT001	3536	364	134	54
287	OUT000	3336	324	134	54
288	DRETP0	3136	284	134	54
289	CALVPP1	3418	82	98	154
290	CALVNP1	3226	82	98	154
291	VTHPP1	2990	82	186	154
292	VTHNP1	2706	82	186	154
293	VISETP1	2422	82	186	154
294	VTSELP1	2182	82	98	154
295	VCCP1	1942	109	186	208
296	GNDP1	1662	109	186	208
297	CBUS3P1	1422	82	98	154
298	CBUS2P1	1230	82	98	154
299	CBUS1P1	1038	82	98	154
300	CBUS0P1	846	82	98	154
301	SSGNDP3	610	82	186	154
302	VCSP	3555	171	92	156
303	VCSP2	2739	215	140	44
304	VCSN	2151	219	140	52
305	VX	1209	223	152	60
306	VQ4	845	221	120	48

Table 3: Tabulation of Simulated Detector Signal

Time [ns]	Current [μA]	8.5	0.4317	18.5	0.0068
-1.0	0.0000	9.0	0.3383	19.0	0.0064
-0.5	0.0000	9.5	0.1628	19.5	0.0060
0.0	0.0000	10.0	0.0253	20.0	0.0056
0.5	0.1850	10.5	0.0195	20.5	0.0052
1.0	0.3931	11.0	0.0183	21.0	0.0048
1.5	0.4027	11.5	0.0172	21.5	0.0044
2.0	0.4025	12.0	0.0161	22.0	0.0040
2.5	0.4055	12.5	0.0151	22.5	0.0037
3.0	0.4124	13.0	0.0142	23.0	0.0033
3.5	0.4242	13.5	0.0133	23.5	0.0030
4.0	0.4373	14.0	0.0125	24.0	0.0027
4.5	0.4489	14.5	0.0117	24.5	0.0024
5.0	0.4615	15.0	0.0110	25.0	0.0021
5.5	0.4675	15.5	0.0103	25.5	0.0017
6.0	0.4709	16.0	0.0096	26.0	0.0013
6.5	0.4718	16.5	0.0090	26.5	0.0008
7.0	0.4725	17.0	0.0084	27.0	0.0002
7.5	0.4665	17.5	0.0078	27.5	0.0000
8.0	0.4588	18.0	0.0073		

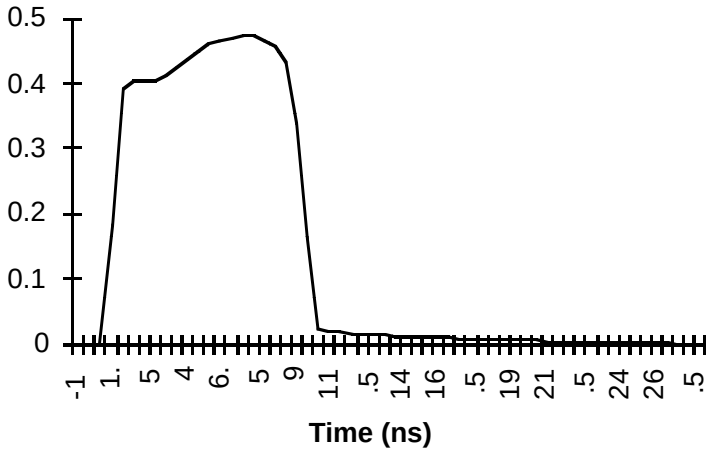

Figure 6: Simulated Depleted Detector n-Strip Signal
Signal is for an irradiated n-strip detector. For an unirradiated detector, the time scale should be scaled shorter by the ratio 0.60.
[See reference (9) J. Leslie, et al.]

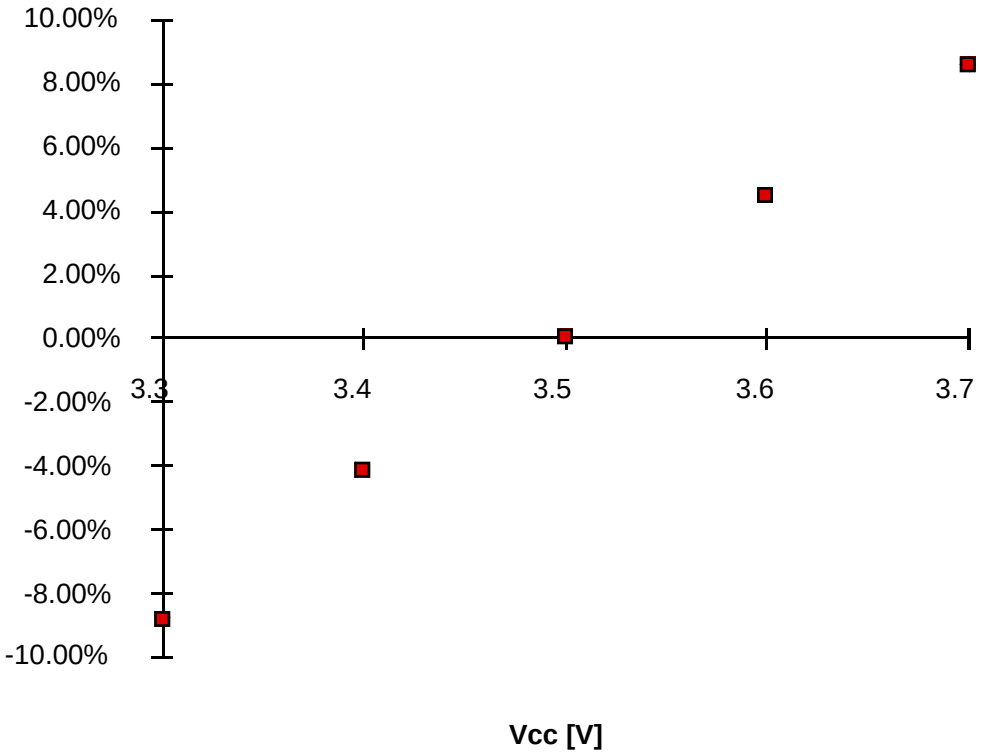

Figure 7: Simulated Gain Sensitiviy to Vcc for 1 fC signal
(As measured at input to comparator)