RADIATION HARD ELECTRONICS

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- Radiation Effects
- RadHard Technologies, Design Examples
- SEU
- Design sensitivity to radiation

Radiation Effect in Si/SiO2

TOTAL DOSE EFFECTS

Silicon : displacement damage

Silicon oxide : (positive) trapped charges

Si/SiO2 interface : charges sign depends on bias

TRANSIENT EFFECTS

Single Event Upset

Single Event Latchup

“Today” Rad-Hard Technologies

AIM : RADIATION RESISTANCE BEYOND 1Mrads

A FEW COMPANIES ARE ACTIVE IN THE WORLD : ATMEL (Temic), HONEYWELL, LAUREL, MARCONI, TRW

TWO COMPANIES EXPRESS INTEREST IN HEP APPLICATIONS : ATMEL (Temic), HONEYWELL

"Today" Rad-Hard Technologies

BACKGROUND :		Production	Application
MILITARY APPLICATIONS ↘ SPATIAL APPLICATIONS ↗		Low Volumes High Cost	Radsoft clone versions (uP) Small analogue
HIGH ENERGY PHYSICS EXPERIMENTS :	(?)	"Large" Volumes (*) Low Cost	Proprietary designs Analogue

(*) compare to other radiation environment applications. Small compare to standard process

"Today" Rad-Hard Technologies

BACKGROUND :

Radiation Environment

MILITARY APPLICATIONS ↘

SPATIAL APPLICATIONS ↗

"Burst"

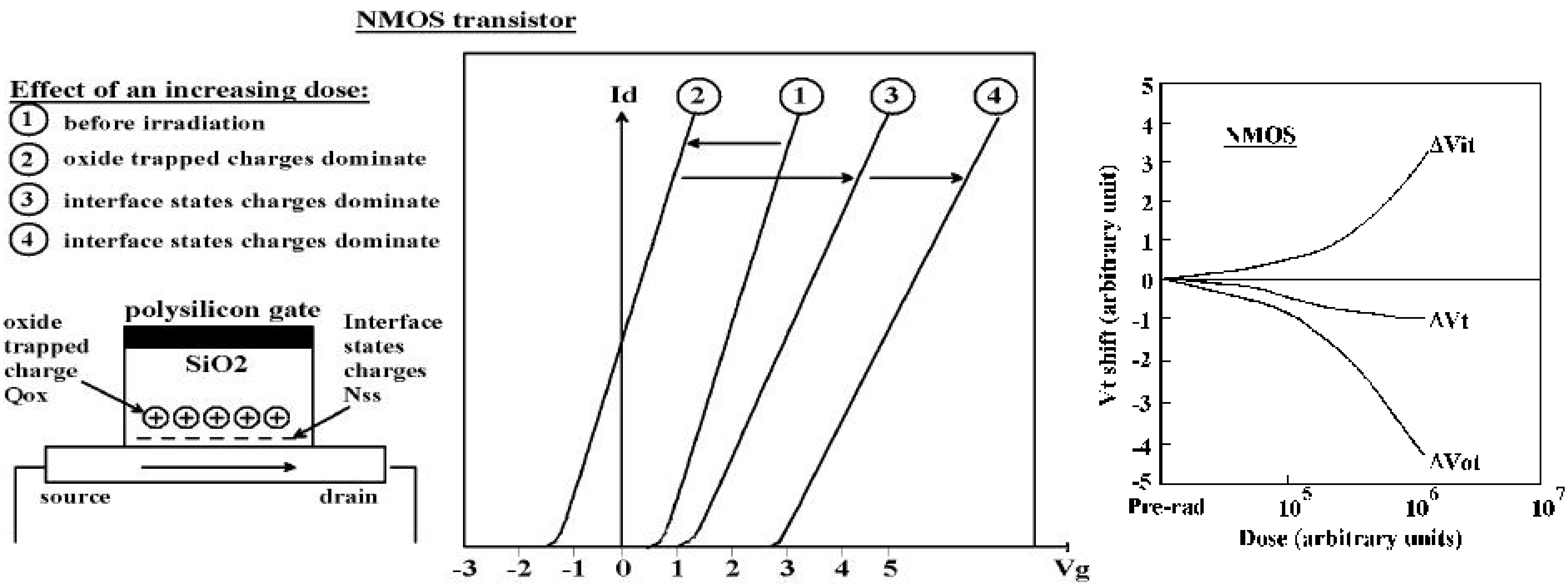
Low Total Dose, Low neutron fluence

HIGH ENERGY PHYSICS EXPERIMENTS : (?)

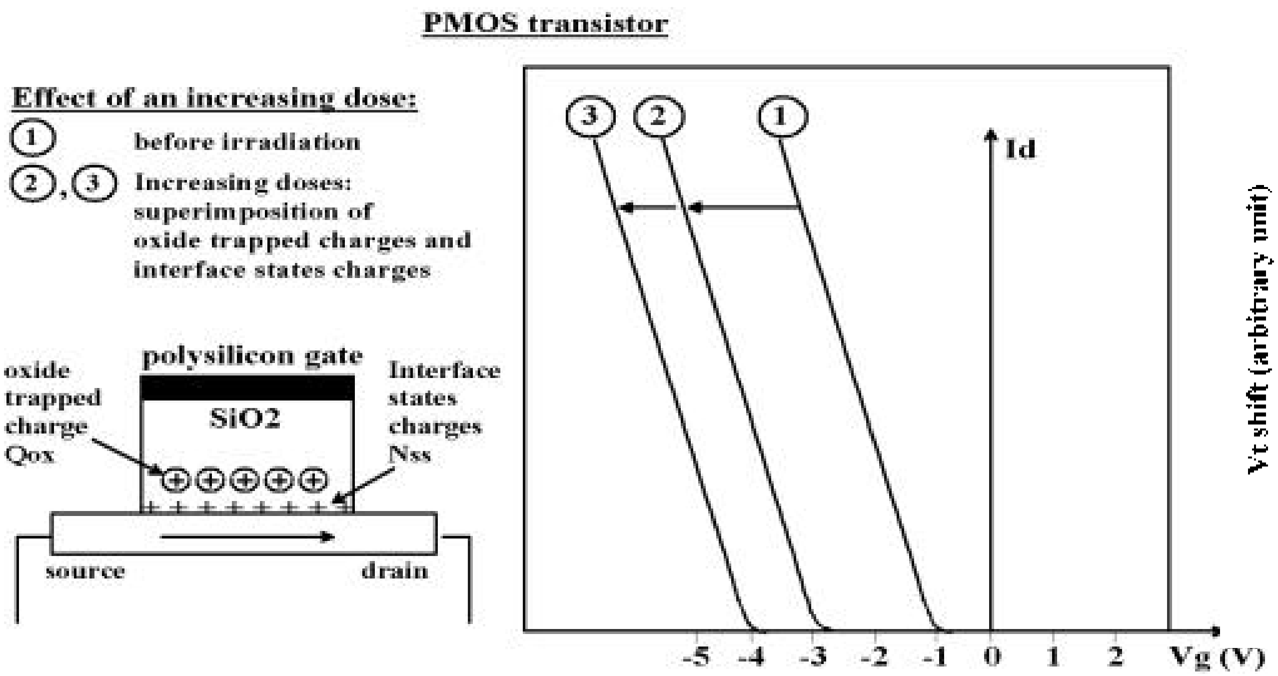
Low dose rate

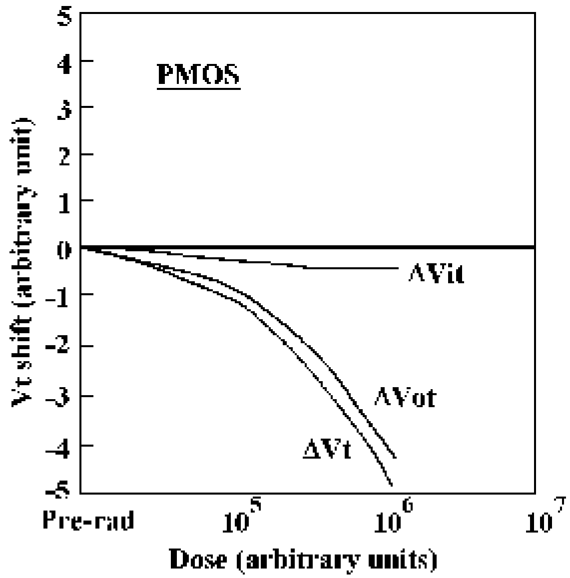
Large neutron fluence

Radiation Effects in N-MOS

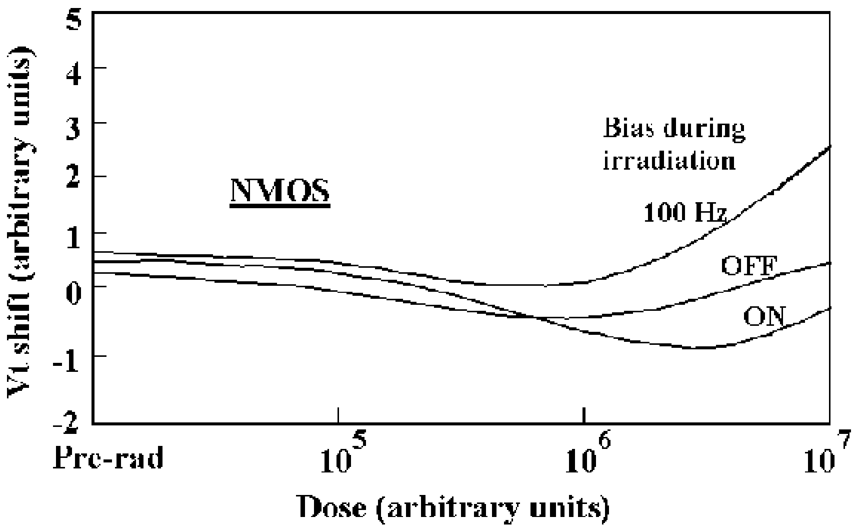


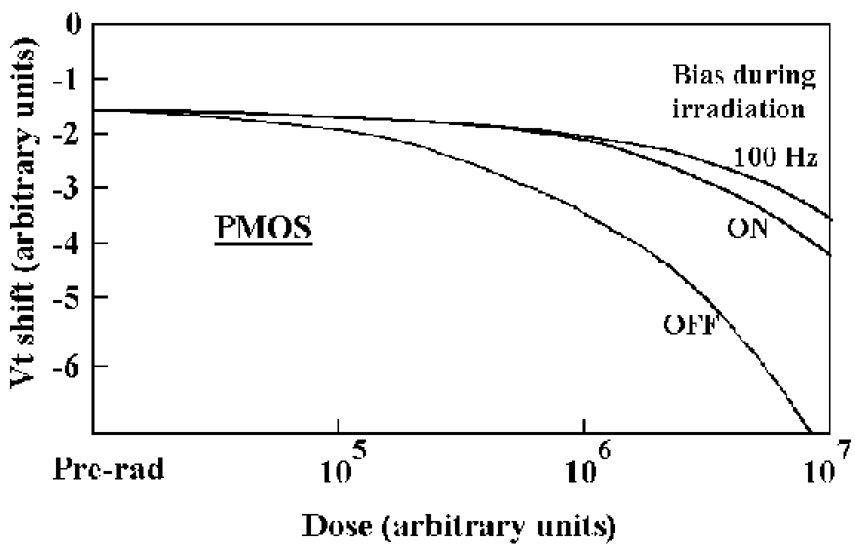
Radiation Effect in P-MOS



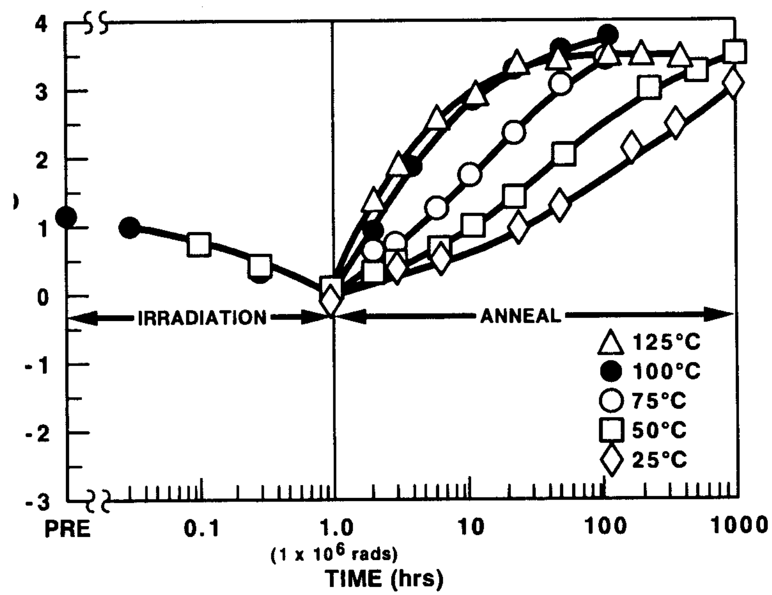


BIAS EFFECTS



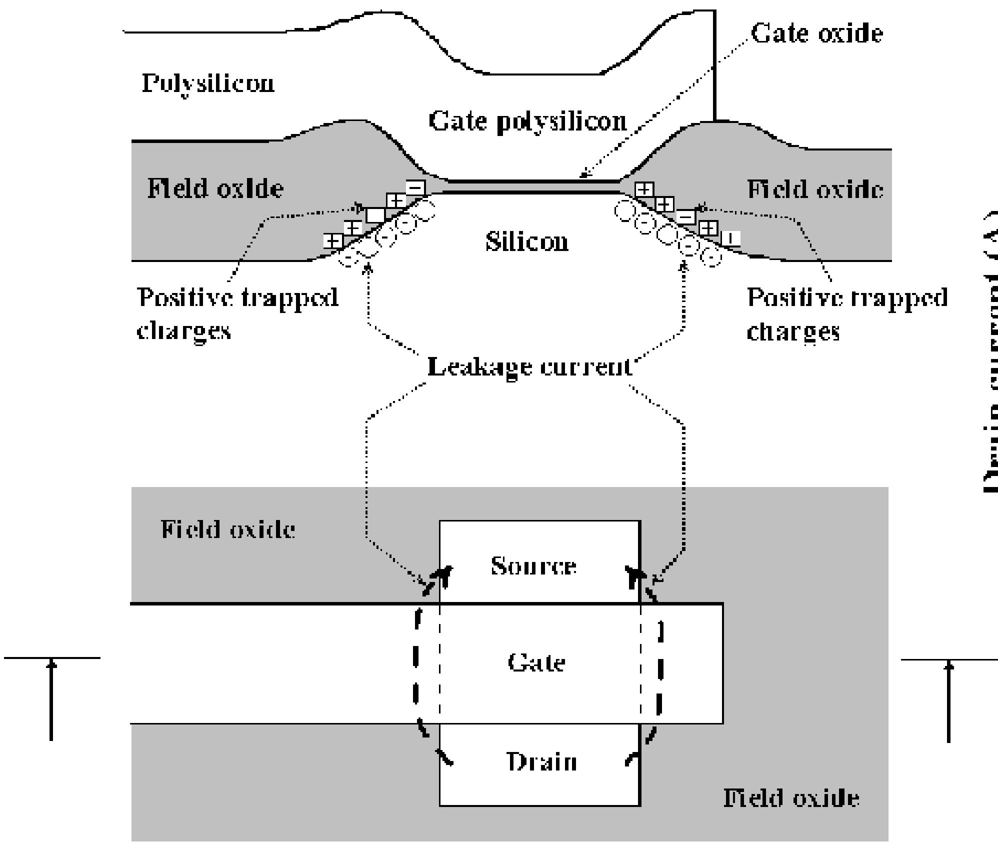


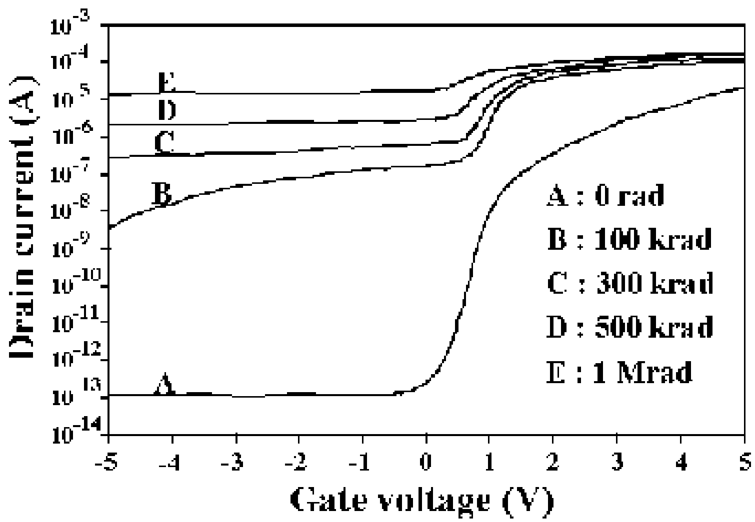
ANNEALING



- Slow release of trapped charges
- Activated by Temp.
- Relative recovery of Oxide/Interface traps may lead to “rebound” (N-channel)

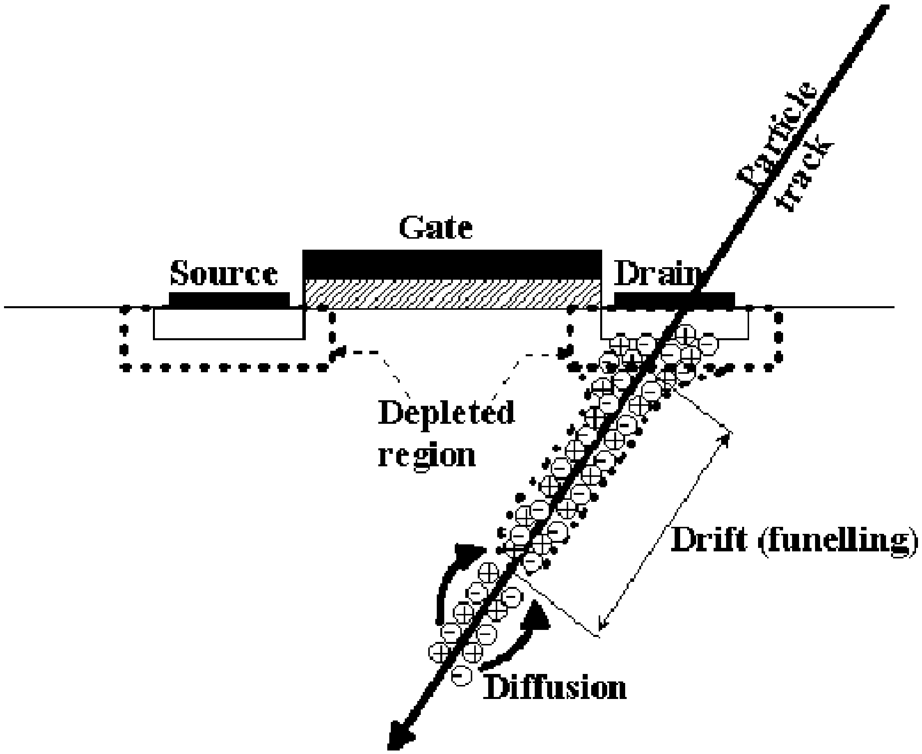
LEAKAGE CURRENT EFFECT



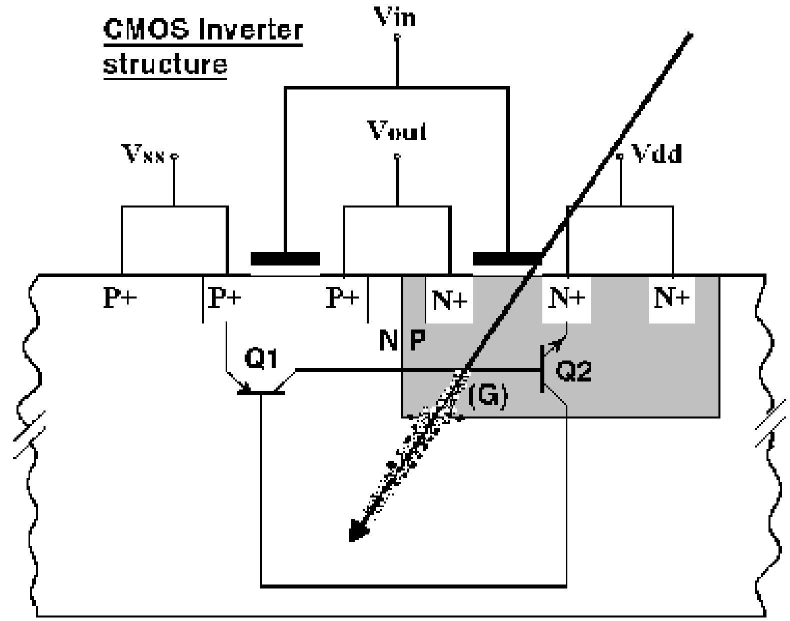


"Thick" Field Oxides accumulate more + charges ==> ↑ Vot contr.
↓ Vth for NMOS

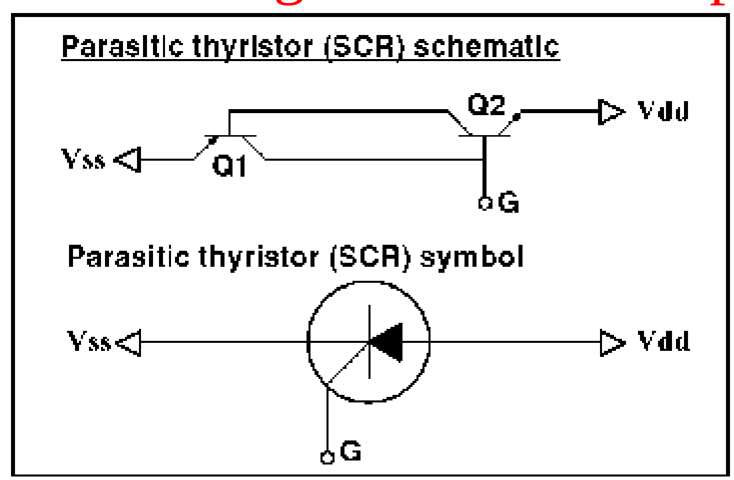
SINGLE EVENTS



SEU : Single Event Upset
(corruption of logic state)

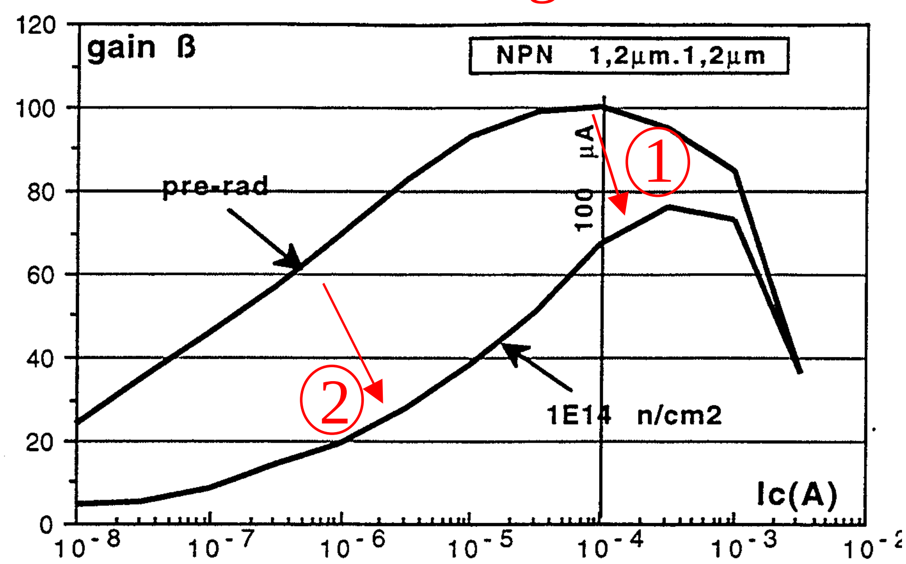


SEL : Single Event Latchup



BIPOLAR TRANSISTOR

Neutron Degradation

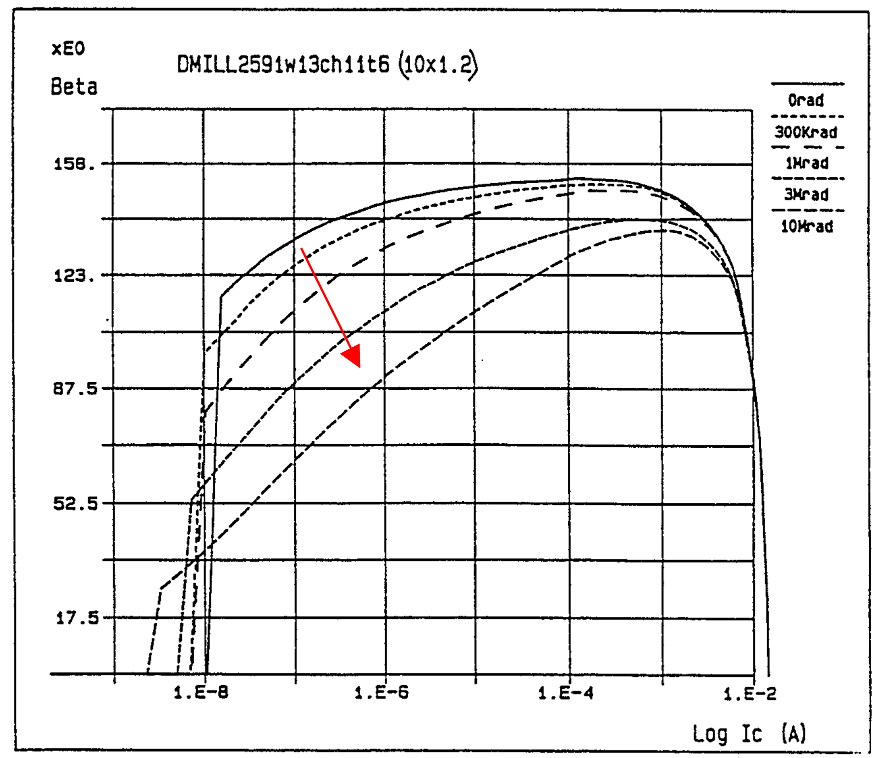


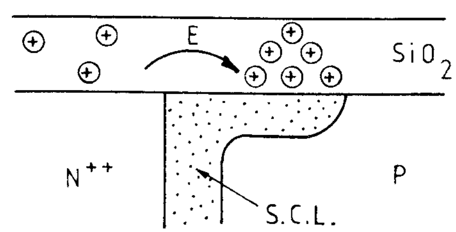
Silicon crystalline structure defects with neutrons :

① Shorter Minority Carriers Lifetime

② Surface Current Increase

Gamma Degradation





b)

β = Ic/IbT

IbT = Ir + Id + Ist

Ist ↗ with trapped charges in oxide

RAD-HARD by technology

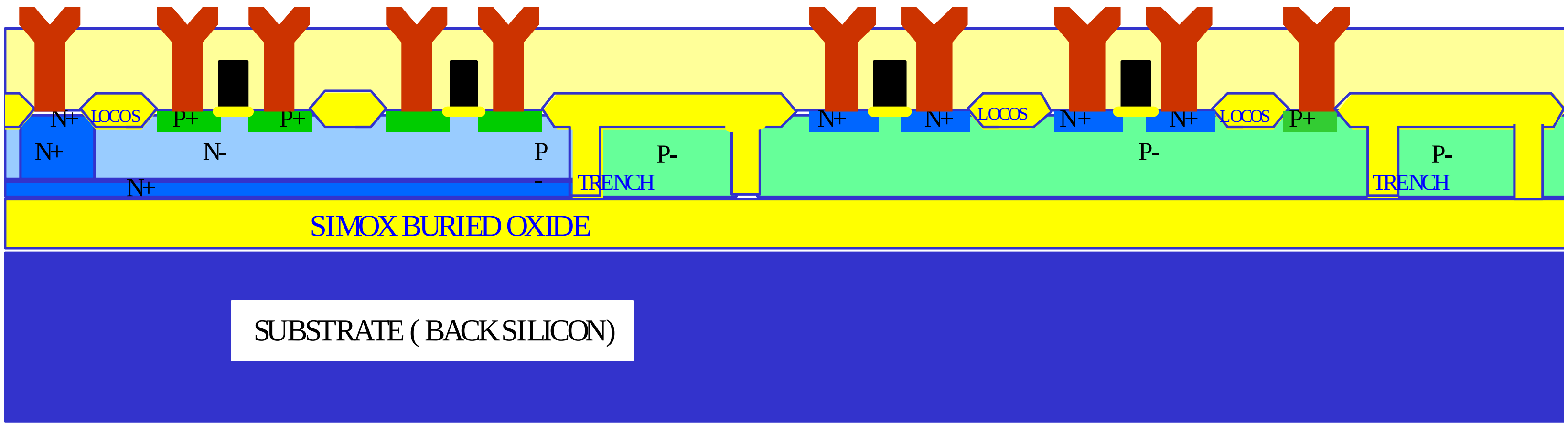
Specific Oxide and Si/SiO2 treatments

- **Low Temp Oxidation**
- **Low Temp Oxide Annealing**
- **Trap sites filling at Si/SiO2 interface**

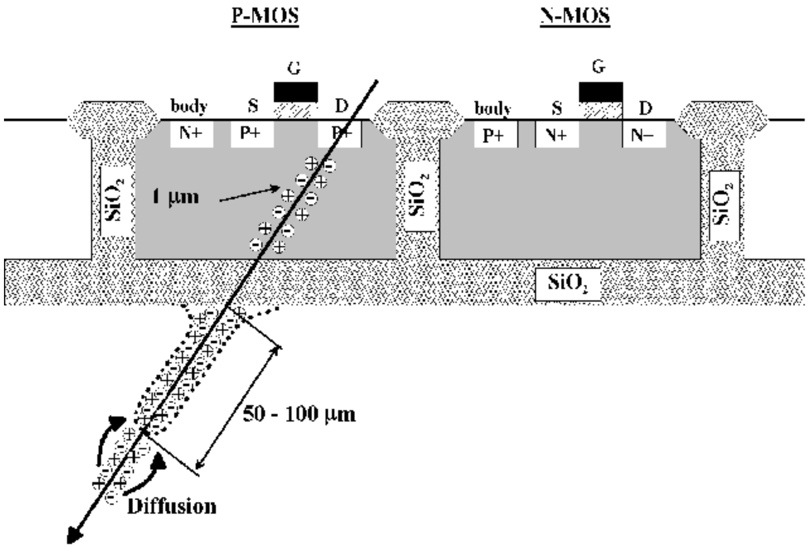
Latch-up protection

- **Low resistance epitaxial layer**
- **SOI structure**

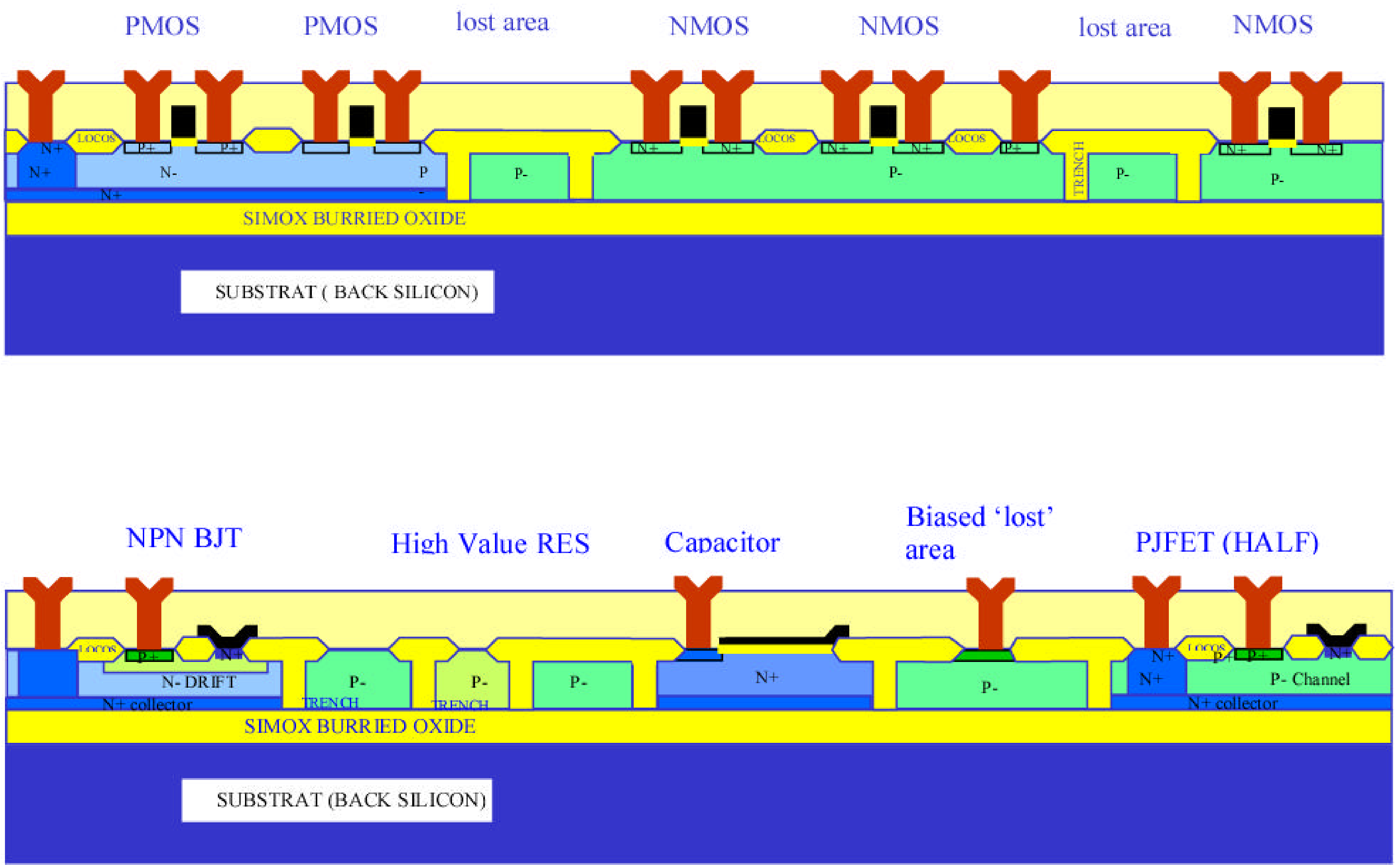
DMILL-SOI STRUCTURE



- **SOI STRUCTURE PREVENTS LATCH-UP, LIMITS SEU**
- **RADIATION HARDENED OXIDES**



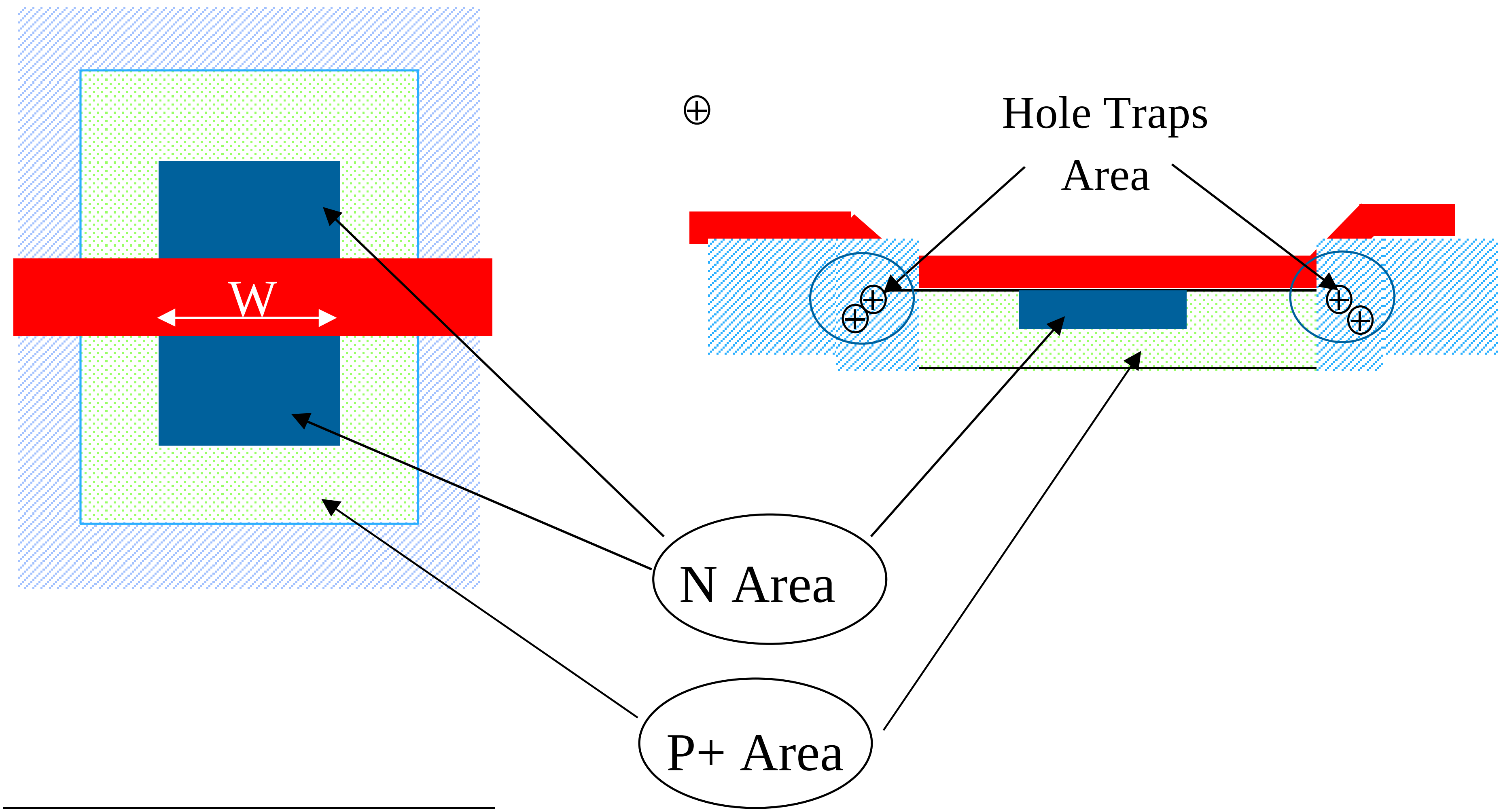
Dmill : Isolated Trench Structure



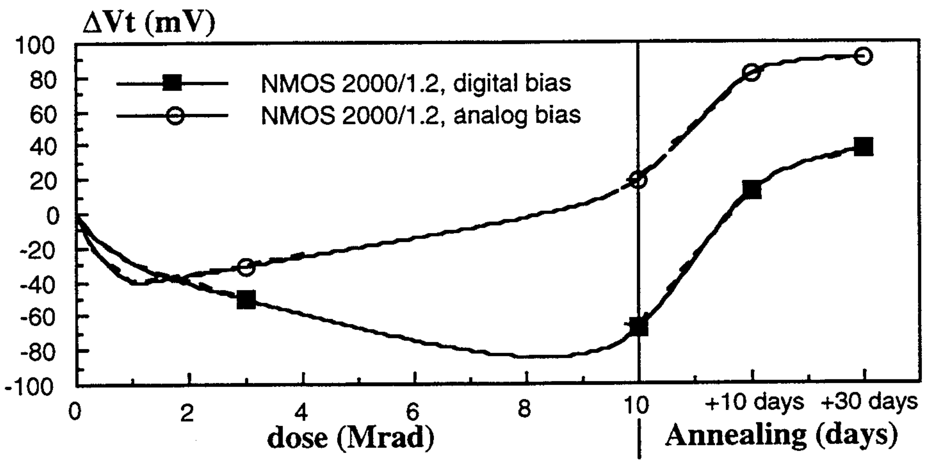
Dmill : Mixed Digital-Analog Technology

Parameter	Typ value	Unit	Description
MOS transistors			
Leff N	0.72	µm	Electrical length of a 0.8µm N channel transistor
Leff P	0.70	µm	Electrical length of a 0.8µm N channel transistor
VTN	0.93	V	Threshold voltage of a 0.8µm N channel transistor
VTP	-0.80	V	Threshold voltage of a 0.8µm P channel transistor
IDSN (0.8µm)	8.30	mA	Drain current for a 25/0.8µm N transistor with VGS=VDS=5.0V
IDSP (0.8µm)	4.60	mA	Drain current for a 25/0.8µm P transistor with VGS=VDS=-5.0V
BVDSS (1µA)	>8.00	V	Drain / Source breakdown voltage at ID = 1.0µA
VTN Field	>10.0	V	
VTP Field	>10.0	V	
NPN Bipolar			
Beta (1.2x1.2)	250	NU	NPN 1.2x1.2 ideal forward beta
V_{EARLY}	96	V	NPN Forward early voltage
BVCE0	5.70	V	Breakdown of collector/emitter with base open
BVCB0	17.0	V	Breakdown of collector/base with emitter open
P-JFET			
VPPJ (1.2µm)	1.20	V	Pinch-off voltage of a 100/1.2 P-JFET
GDPJ (1.2µm)	1.135	µS/µm	Drain transconducatnce of a 100/1.2 PJFET (VGS=0V; VDS=-3V)
OXIDES			
E_{ox}	17.5	nm	Gate oxide thickness
E_{Field}	470	nm	Gate oxide thickness
E_{capa}	42.0	nm	Gate oxide thickness
RESISTORS			
R_{P+}	118	/square	P+ resistivity
R_{P-}	3550	/square	P- resistivity
$R_{extrins}$	1650	/square	Extrinsic base resistivity
R_{POL}	2.35	/square	Poly gate resistivity
R_{M1}	0.050	/square	Metal 1 resistivity
R_{M2}	0.040	/square	Metal2 resistivity

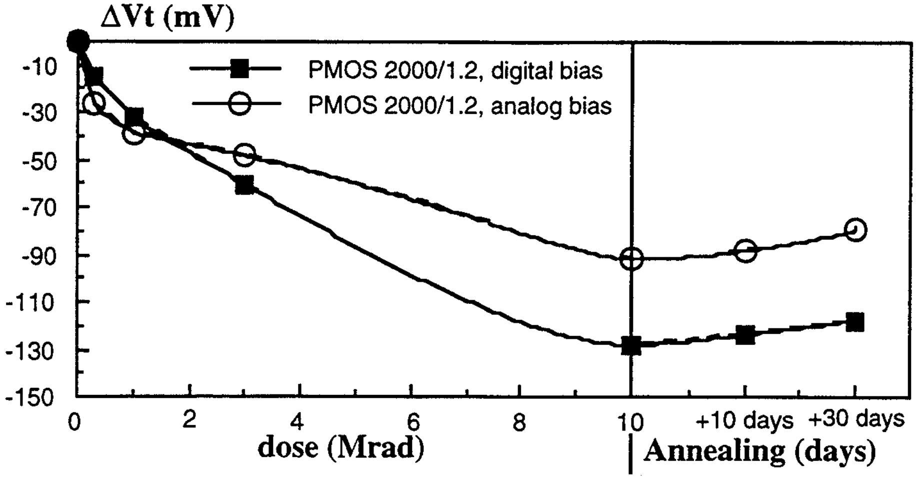
N-MOS Leakage Prevention in DMILL



Typical DMILL VT Shifts

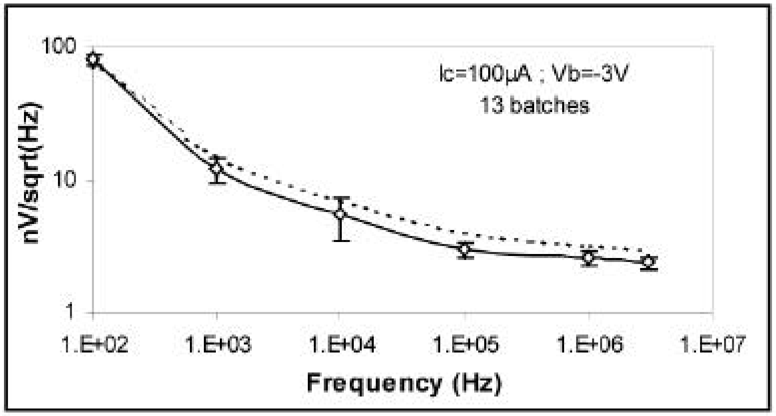


VTN shows the typical "rebound" effect for N-MOS transistors, which continues during annealing

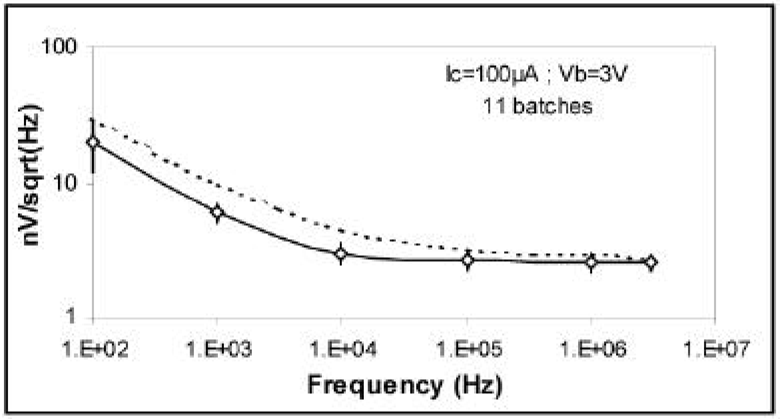


VTP shows larger shifts because of additional ΔVot ΔVit drifts. -200mV is the max. drift at 10Mrads

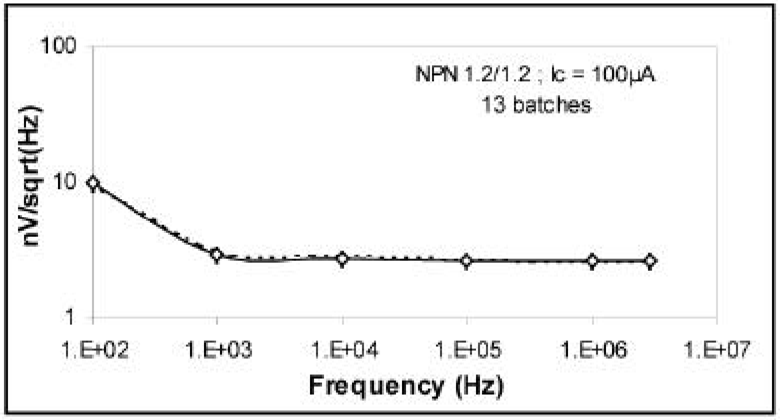
Dmill : Analog Characterics (noise)



Nmos



Pmos



BJT

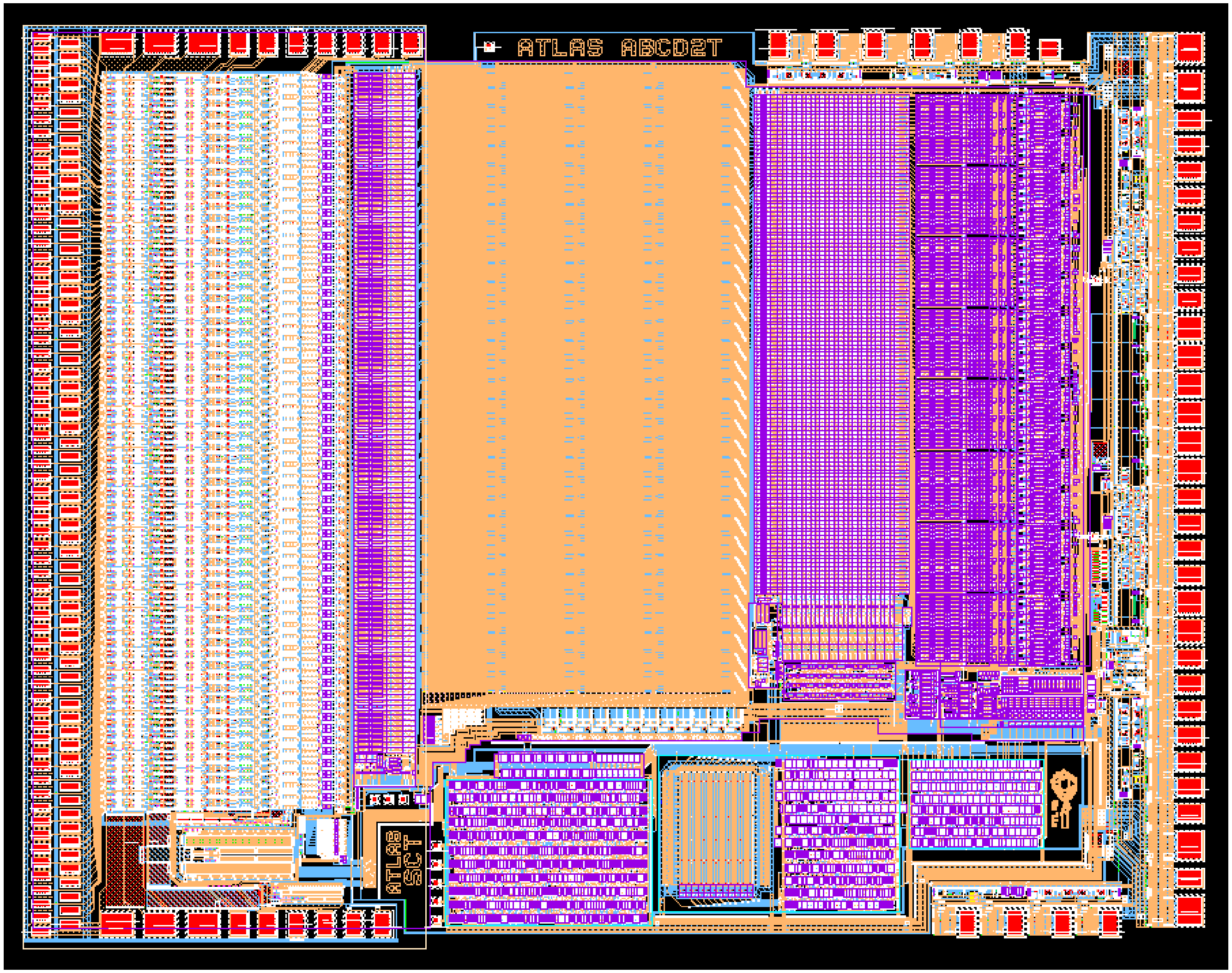
Noise figures for NMOS, PMOS, BJT devices (before & after irradiation to 10Mrads)

Dmill : SEU resistance

Storing element	SEU threshold (MeV/(mg/cm²))	Reduction factor (*)
Memory Cell	15	200
DFF cell	70	130
Combinatorial	70	40

* Compared to equivalent in standard bulk process with same device features

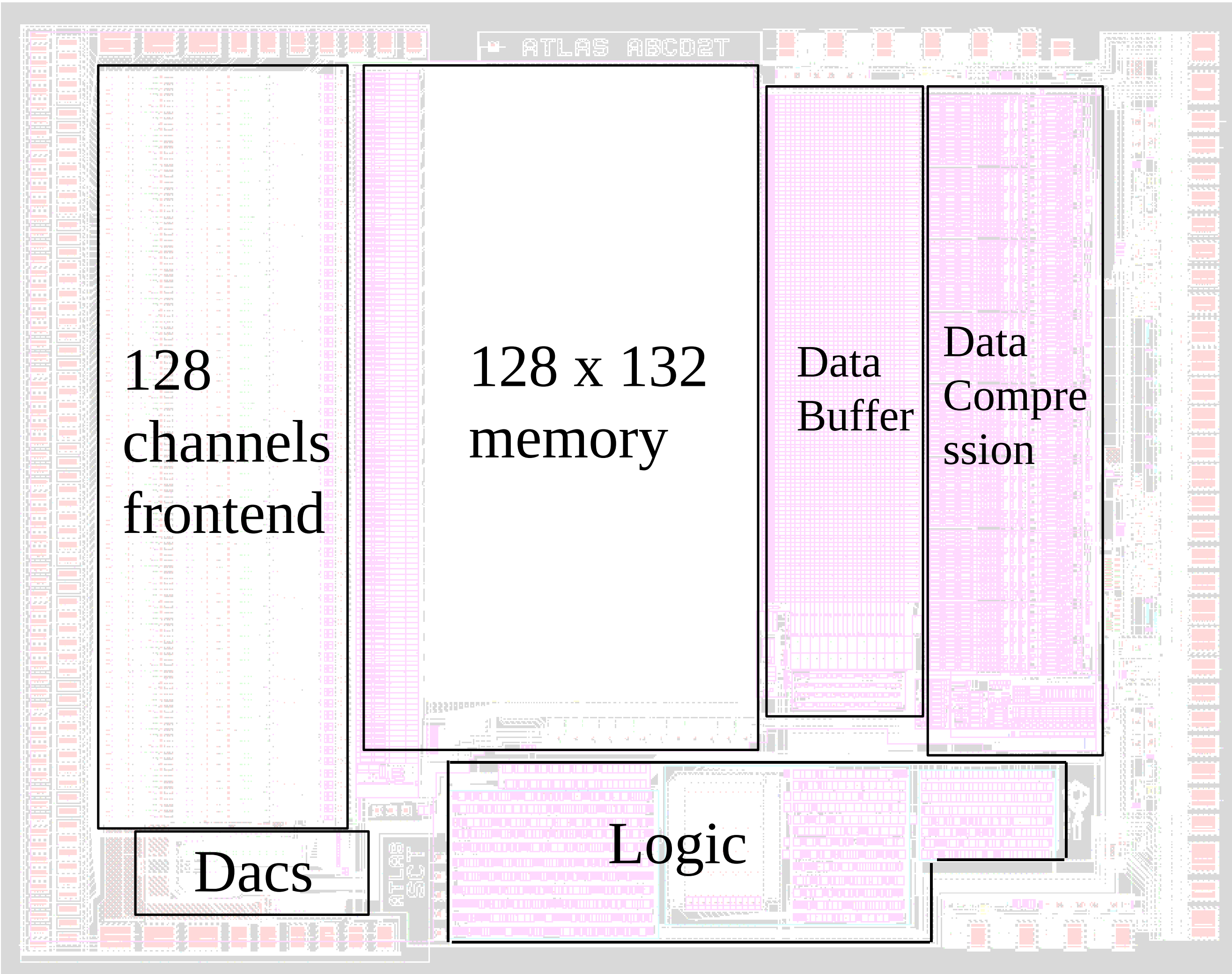
Example of Chip Design in DMILL



• Mixed mode SCT Front-end chip (ABCD, 250K Trans.)

• 10Mrads, 3x1014 neutrons/cm^2 guaranteed**

ABCD Chip Blocks



Bipolar

Fast Frontend
(25ns peaking Time)
Low Noise
(1500 el @ 20pF CL)

CMOS

40 MHz clock
3.2 uS data retention
Data compression
Logic

51 mm2
P < 0.5w

Performance Degradation (gain)

24 GeV protons
3×10^{14} p/cm^2

Neutrons
2×10^{14} n/cm^2

10 keV X-ray
10 Mrad

Title:
C:\Lars\GainvsPreamp.eps
Creator:
ROOT Version 2.21/08
Preview:
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with a preview included in it.
Comment:
This EPS picture will print to a
PostScript printer, but not to
other types of printers.

Title:
GainSh24NoErr.eps
Creator:
ROOT Version 2.21/08
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other types of printers.

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ROOT Version 2.21/08
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with a preview included in it.
Comment:
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PostScript printer, but not to
other types of printers.

Performance Degradation (noise)

24 GeV protons
3 x 10^{14} p/cm^2

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C:\Lars\transparencies\NoisevsPreamp.eps
Creator:
ROOT Version 2.21/08
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with a preview included in it.
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PostScript printer, but not to
other types of printers.

Neutrons
2 x 10^{14} n/cm^2

Title:
NoiseSh24NoErr.eps
Creator:
ROOT Version 2.21/08
Preview:
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with a preview included in it.
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PostScript printer, but not to
other types of printers.

10 keV X-ray
10 Mrad

Title:
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Creator:
ROOT Version 2.21/08
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with a preview included in it.
Comment:
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PostScript printer, but not to
other types of printers.

Bipolar Beta degradation

24 GeV protons

1.1×10^{14} p/cm^2

24 GeV protons

3.3×10^{14} p/cm^2

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(Stmmn_yes.xls)
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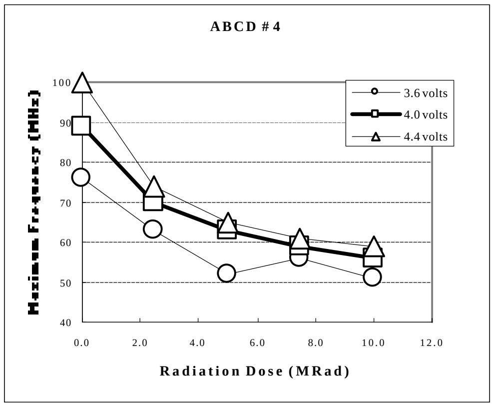
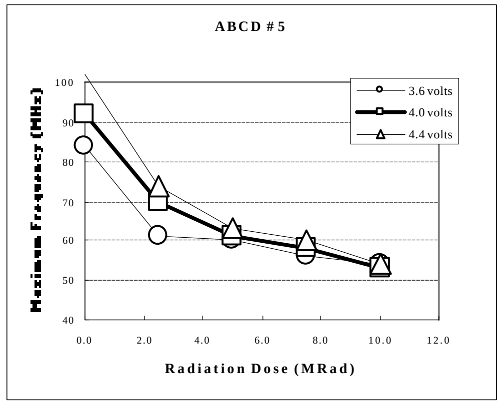
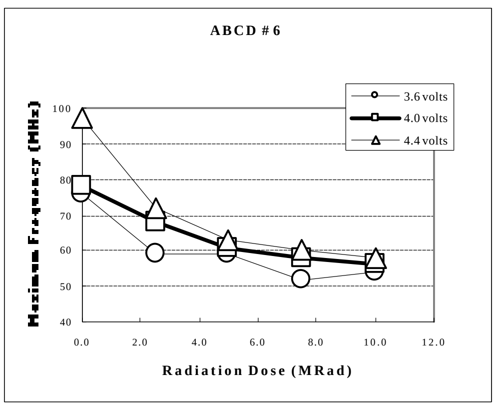
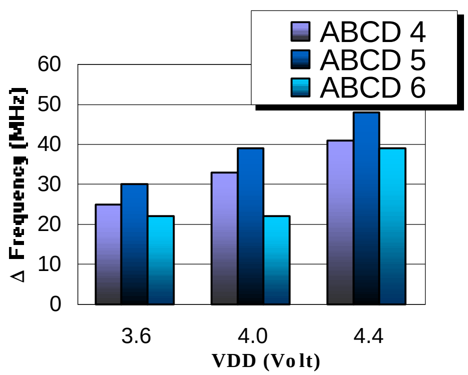
ABCD - Digital Tests









Expected Frequency loss after irradiation # 15-20 MHz

Higher Frequency loss after irradiation is due to design issue

ABCD - Digital Tests

Test vectors were extracted directly from the Verilog models and applied to the ATS tester.
100 000 test vectors run to validate the logical functionality

Maximum working frequency for individual blocks and for the whole chip were evaluated.

Margins for timing and I/O signal levels were evaluated.

Maximum working frequency (in MHz):

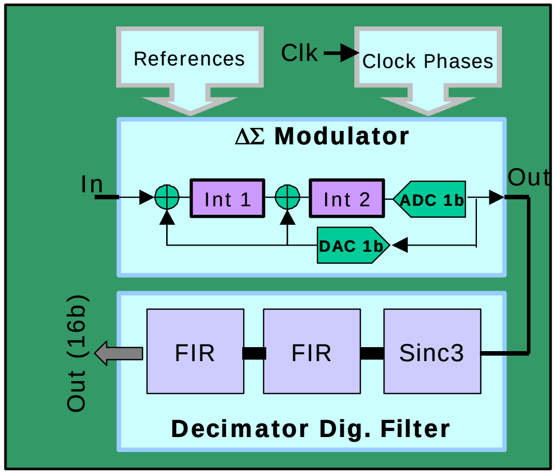
Test #	Chip #2		Chip #4		Test Description
	A	B	A	B	
1	62.5	47.6	66.7	50.0	Send Id mode, address decodin
2	x	47.6	x	52.6	BC reset tests
3	58.8	45.4	62.5	50.0	DTM mode, no hit readout
4	50.0	47.6	58.8	50.0	DTM, single hit readout
5	58.8	47.6	58.8	47.6	DTM, multiple hit readout
6	58.8	47.6	52.6	50.0	Accumulator tests
7	34.5	34.5	45.4	45.4	Data Compression Logic test

x - test was not run
A - L1 and BC counters were excluded from data comparison
B - full data comparison

Dmill : Example of chips

Main Features:

- 16 bit / 25KHz Sigma-Delta A / D converter
- Max sample rate: 50 KHz
- Resolution: 16 bit
- SNR > 96
- Input range: 2 V
- Clock frequency: 12.8 MHz
- Operating temperature range: 0-125 °C
- Supply voltage: 5 V



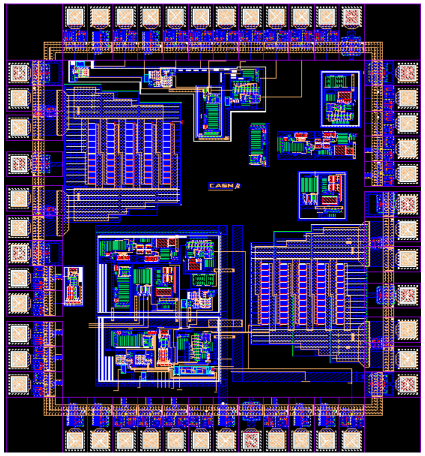
Dmill : Example of chips

Functionality

•Designed to protect CMOS commercial devices (DUPs) against SEL: it contains a power switch to disconnect power supply to the DUP and a control logic to program the critical threshold current and the allowed over-threshold time

Main Features:

•Max threshold current: 100 mA
•Over-threshold time interval: 0.1/10 ms
•Power consumption: <1 mW at 3.3 V
•Operating temperature range: 0-125 °C
•Supply voltage: 3.3 V - 5 V
•Area: 10 mm^2



Dmill : Example of chips

DMILL experience

Centre of competence of TEMIC Semiconductors for DMILL technology (SOI BiCMOS 0.8µm - qualified up to 10 Mrad total dose) since the end of 1998

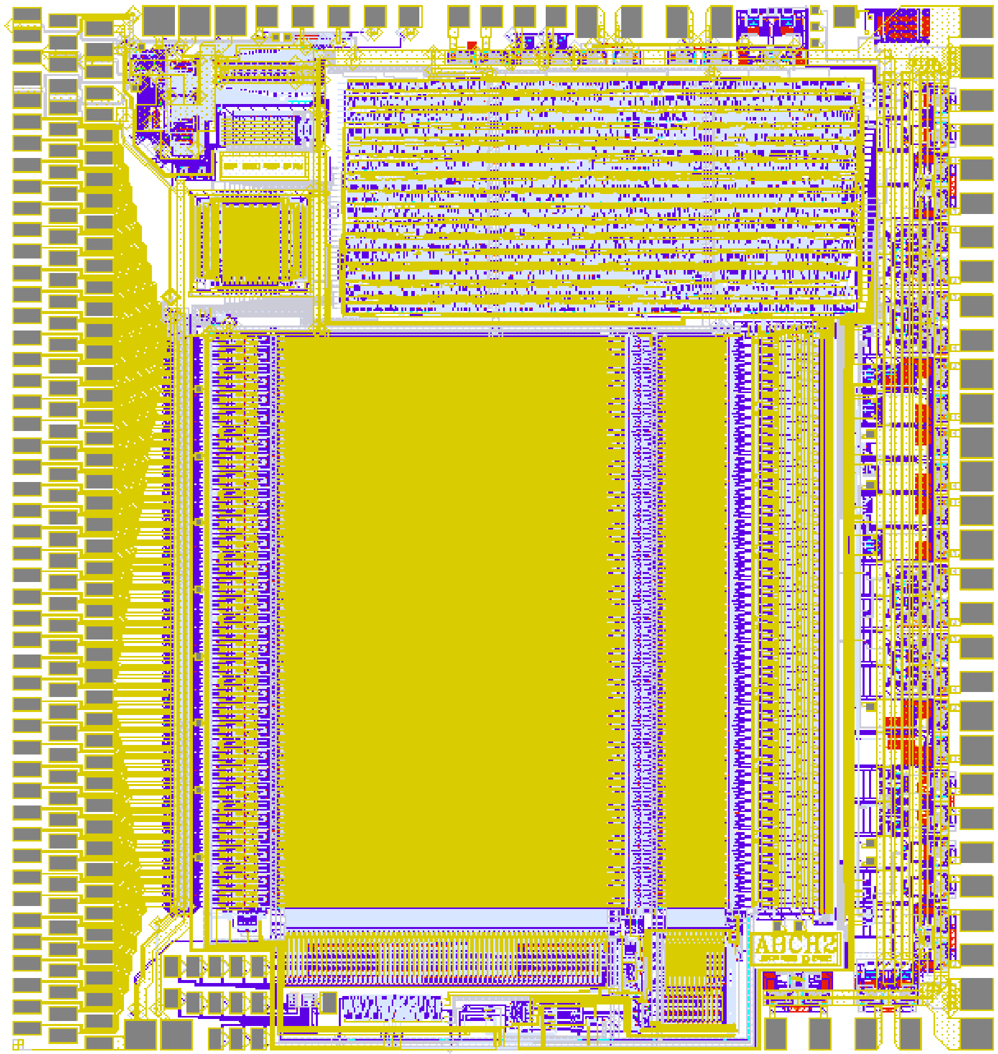
Design activity:

- Analogue
  - TRACK: Testing Rad-hard Analog Cells & design Kit
  - SELP: Single Event Latch-up Protector
- Mixed
  - SDADC16: 16 bit Sigma Delta Analog to Digital Converter
  - RAD-ADC: 12bit/3MHz A/D Converter
- Digital
  - CASA: CAN 2.0B protocol interface macro-cell
  - I2C: I2C protocol slave interface macro-cell
  - 80C51: 80C51 CPU macro-cell

Analogue library

Digital library and Design Kit improvement

Honeywell 0.8um



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Adobe Illustrator(TM) 7.0
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with a preview included in it.
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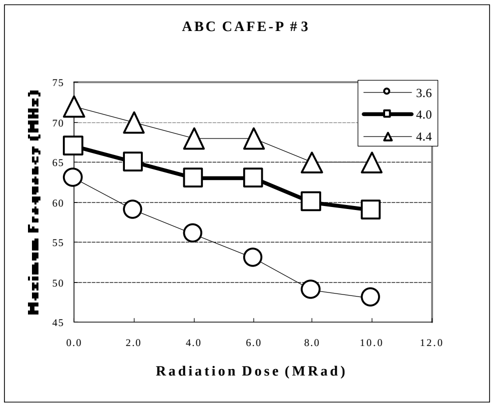
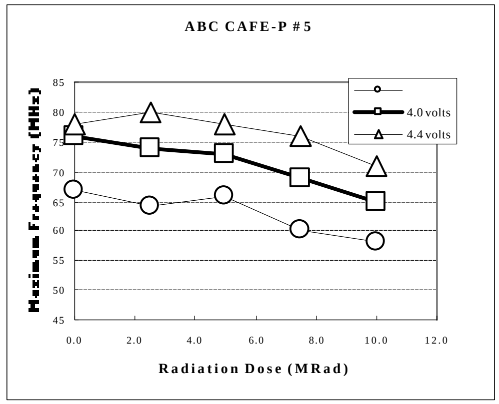
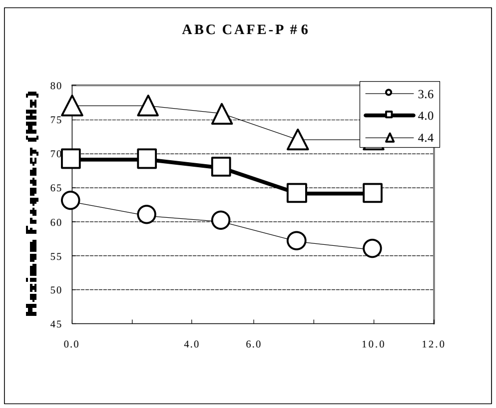
other types of printers.

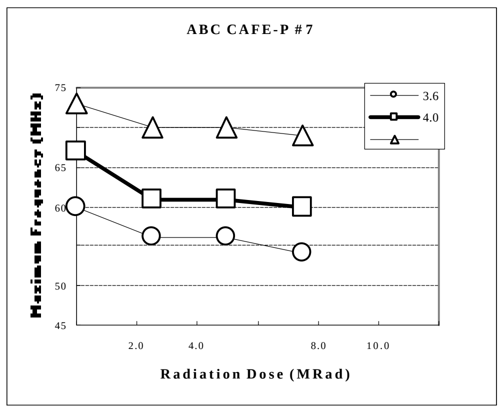
SCT readout in ATLAS

ABC Radiation Results









- 55 ^{13} p/cm^2 corresponds to a dose of 10 MRad. Fluence rate was $5 \cdot 10^{10}$ p/cm^2/s.
- Samples cooled down to 0-3º C during irradiation and stored in freezer afterwards.
- Curves show maximum frequency at which the slowest TV passed as a function of the dose.
- Upper curves: VDD=4.4 V, middle curves: VDD=4.0 V, lower curves: VDD=3.6V

Honeywell 0.8um Bulk

0.8 um CMOS bulk rad-hard technology available

Layout is fully compatible with Rad-Soft, equivalent size features technologies (HP, …)

Guaranteed 1Mrads by manufacturer

Honeywell 0.8um SOI

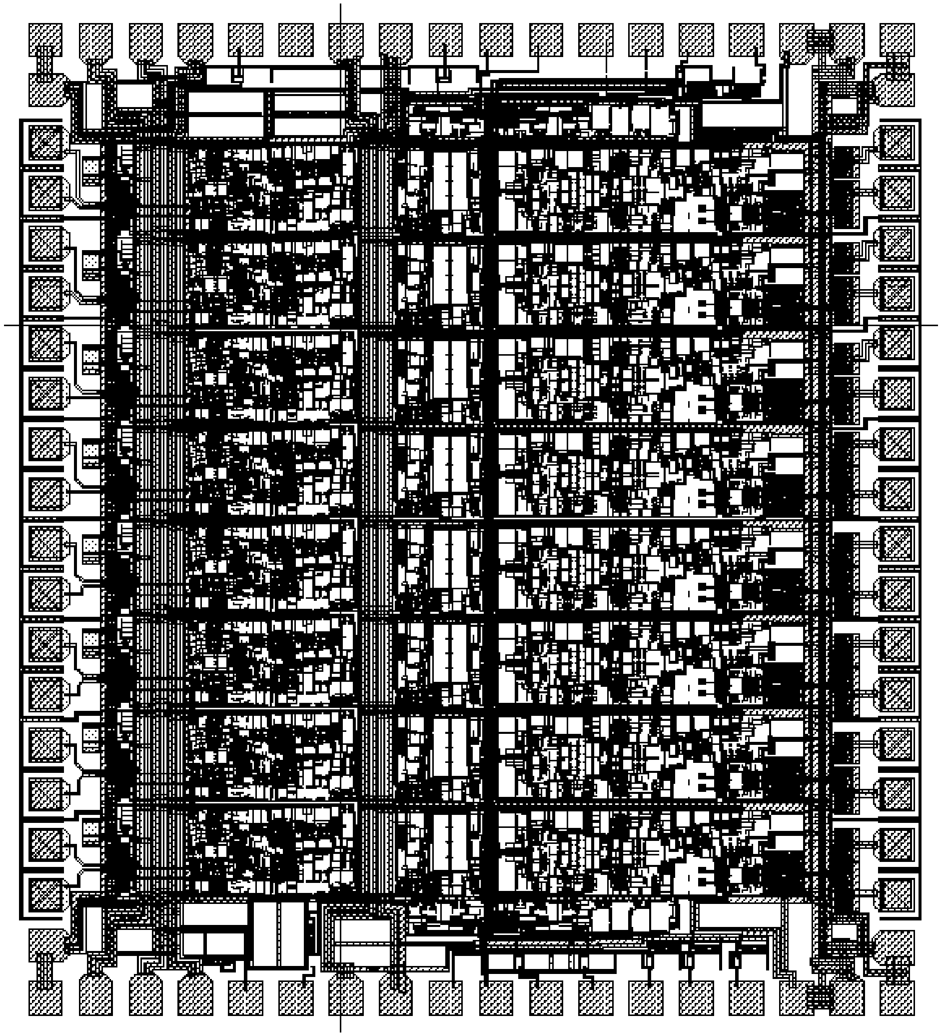
0.8 um CMOS SOI rad-hard technology available

SEL/SEU resistance is improved by thin SOI structure

Layout not directly compatible with rad-soft equivalents

Guaranteed 1Mrads by manufacturer

ASDBLR



6.5ns preamp, shaper, tail cancellation, discriminator

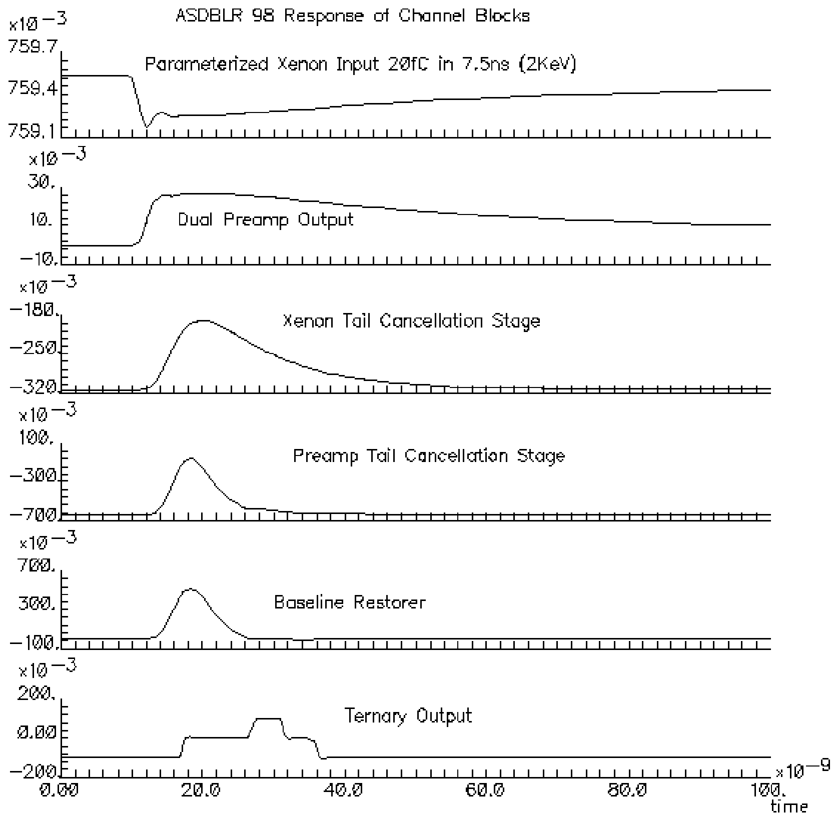
8 channels, 36mW/ch

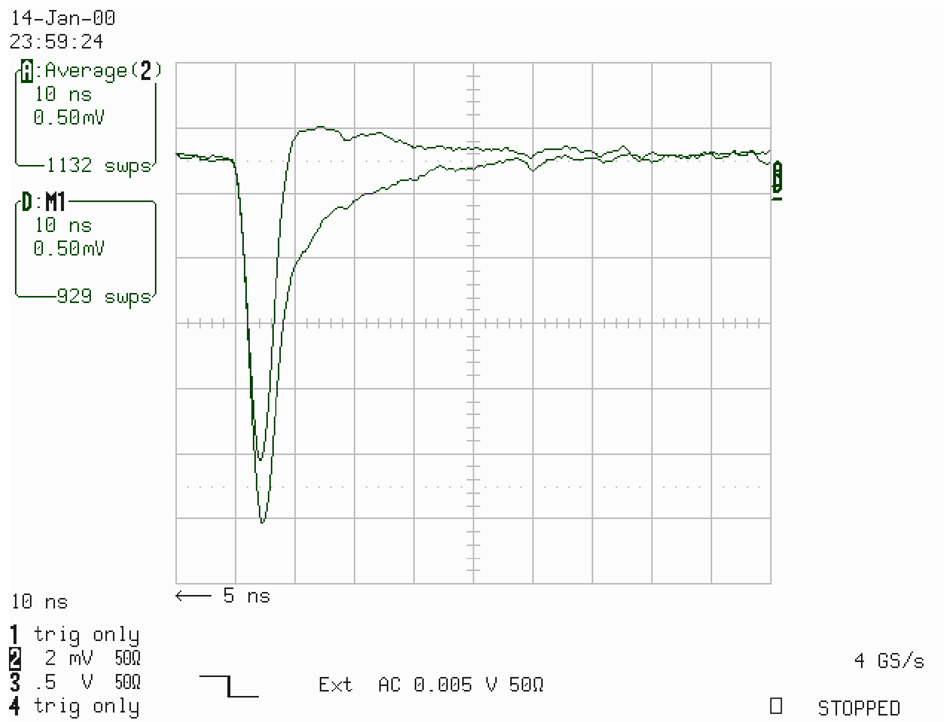
Irradiated up to 1x1014n/cm2**

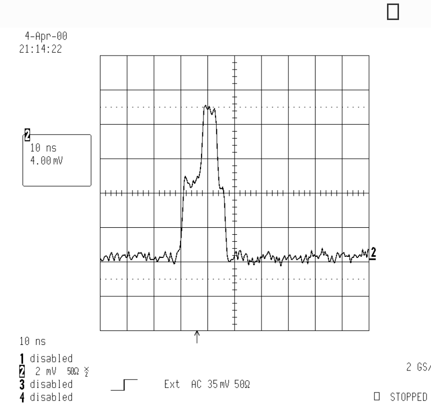
No change in 3fC threshold

TRT readout in ATLAS

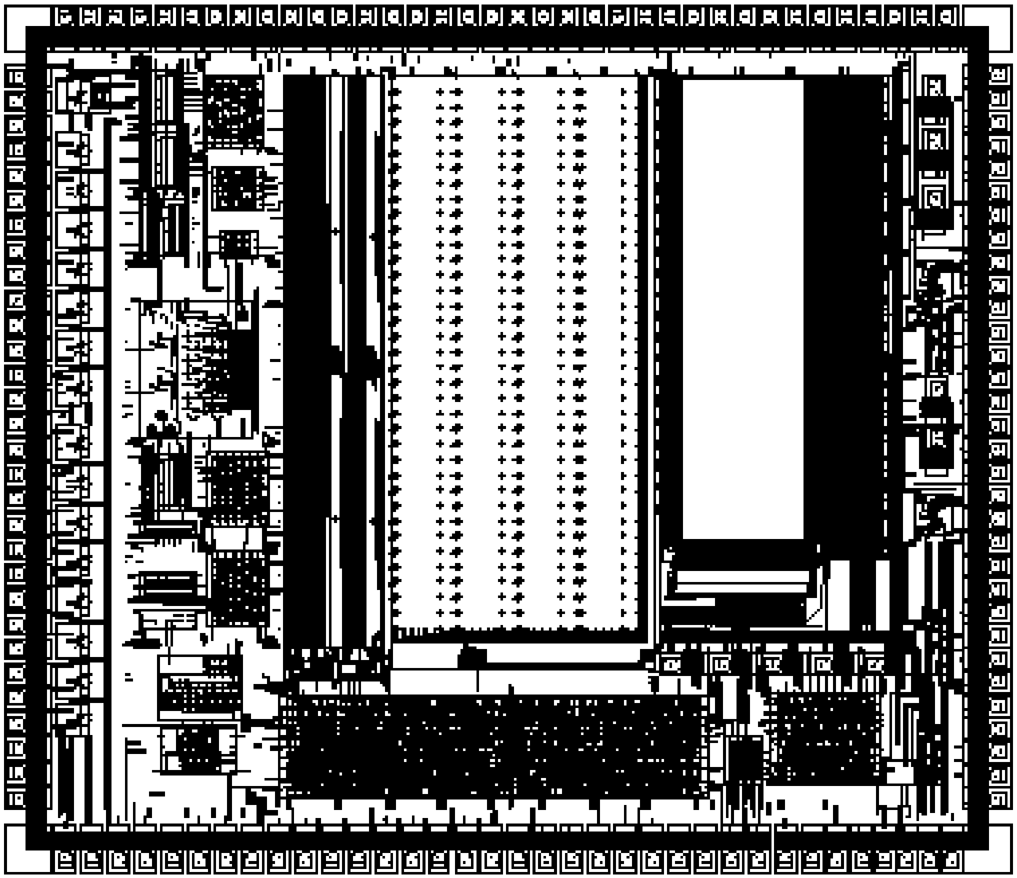
ASDBLR Data


ASDBLR 98 Response of Channel Blocks
Parameterized Xenon Input 20fC in 7.5ns (2KeV)
Dual Preamp Output
Xenon Tail Cancellation Stage
Preamp Tail Cancellation Stage
Baseline Restorer
Ternary Output
x10^-3
759.7
759.4
759.1
30.
10.
-10.
-180.
-250.
-320.
100.
-300.
-700.
700.
300.
-100.
200.
0.00
-200.
0.00
20.0
40.0
60.0
80.0
100.
x10^-9
time


14-Jan-00
23:59:24
A: Average(2)
10 ns
0.50mV
1132 swps
D: M1
10 ns
0.50mV
929 swps
10 ns
← 5 ns
1 trig only
2 2 mV 50Ω
3 .5 V 50Ω
4 trig only
Ext AC 0.005 V 50Ω
4 GS/s
STOPPED


4-Apr-00
21:14:22
10 ns
1 disabled
2 2 mV 50Ω
3 disabled
4 disabled
Ext AC 35mV 50Ω
2 GS/s
STOPPED

DTMROC



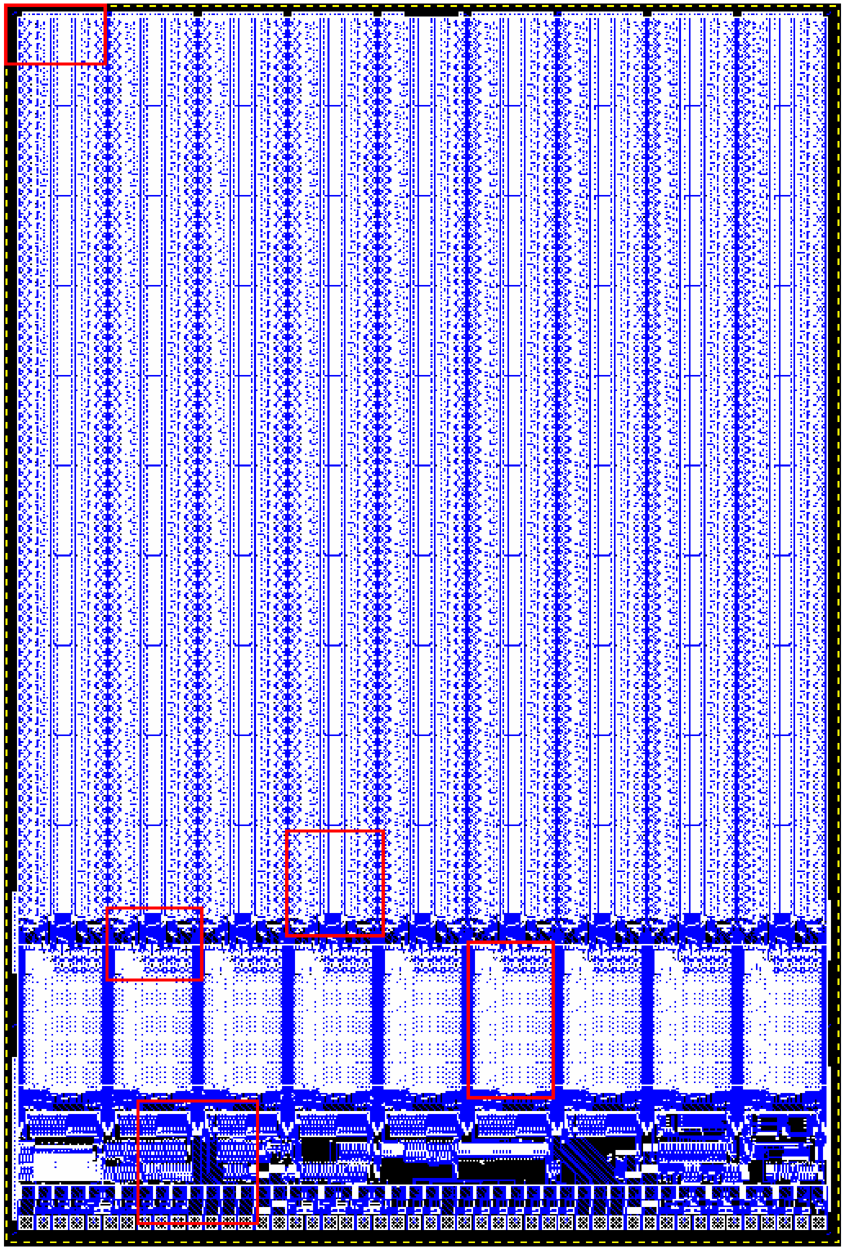
16 channels, 9 bits per channel pipeline memory

Internal DLL (3,2ns) for precise time identification

Analog functions : DACs, calibration pulse (shaper) for ASDBLR

TRT readout in ATLAS

Pixel



FE-D :

18x160 pixel cells 50x400um2

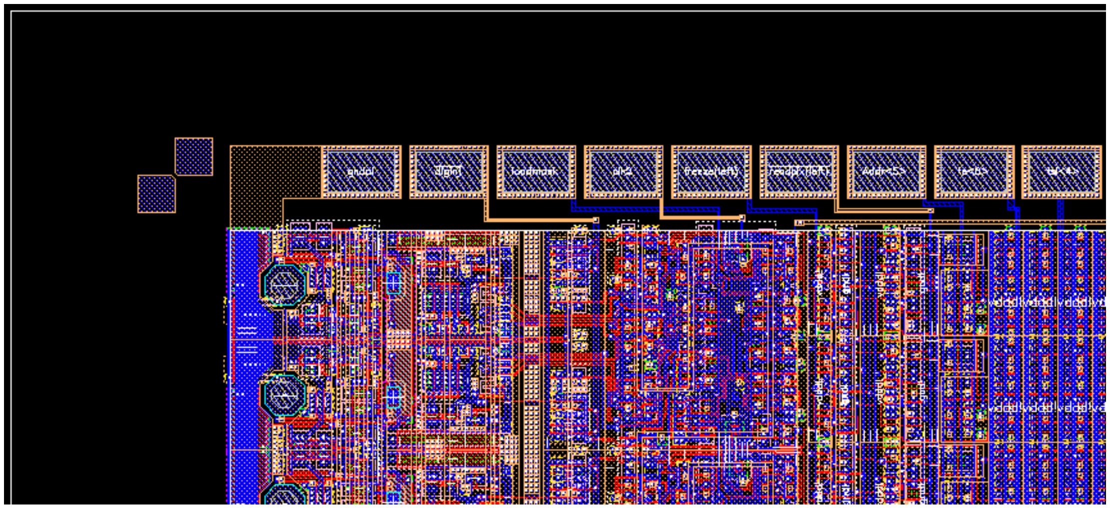
Total 725000Tr.

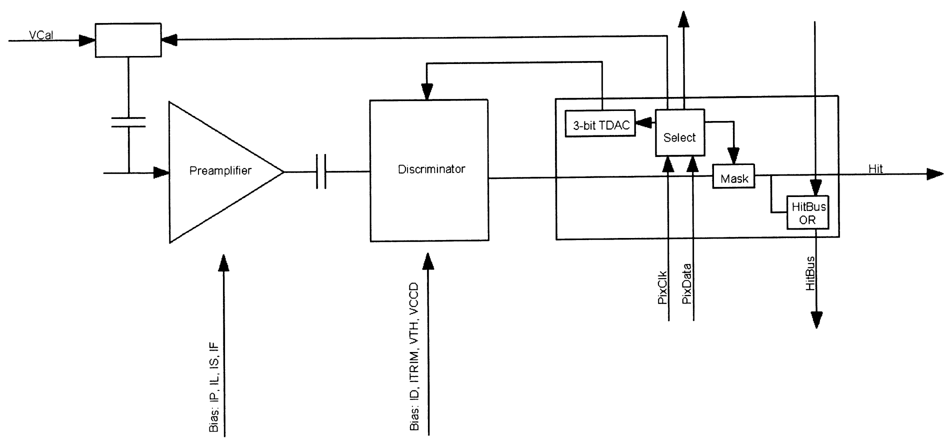
7.4 x 11 mm2

Pixel = preamplifier, discriminator timestamp, etc ...

Pixel readout in ATLAS

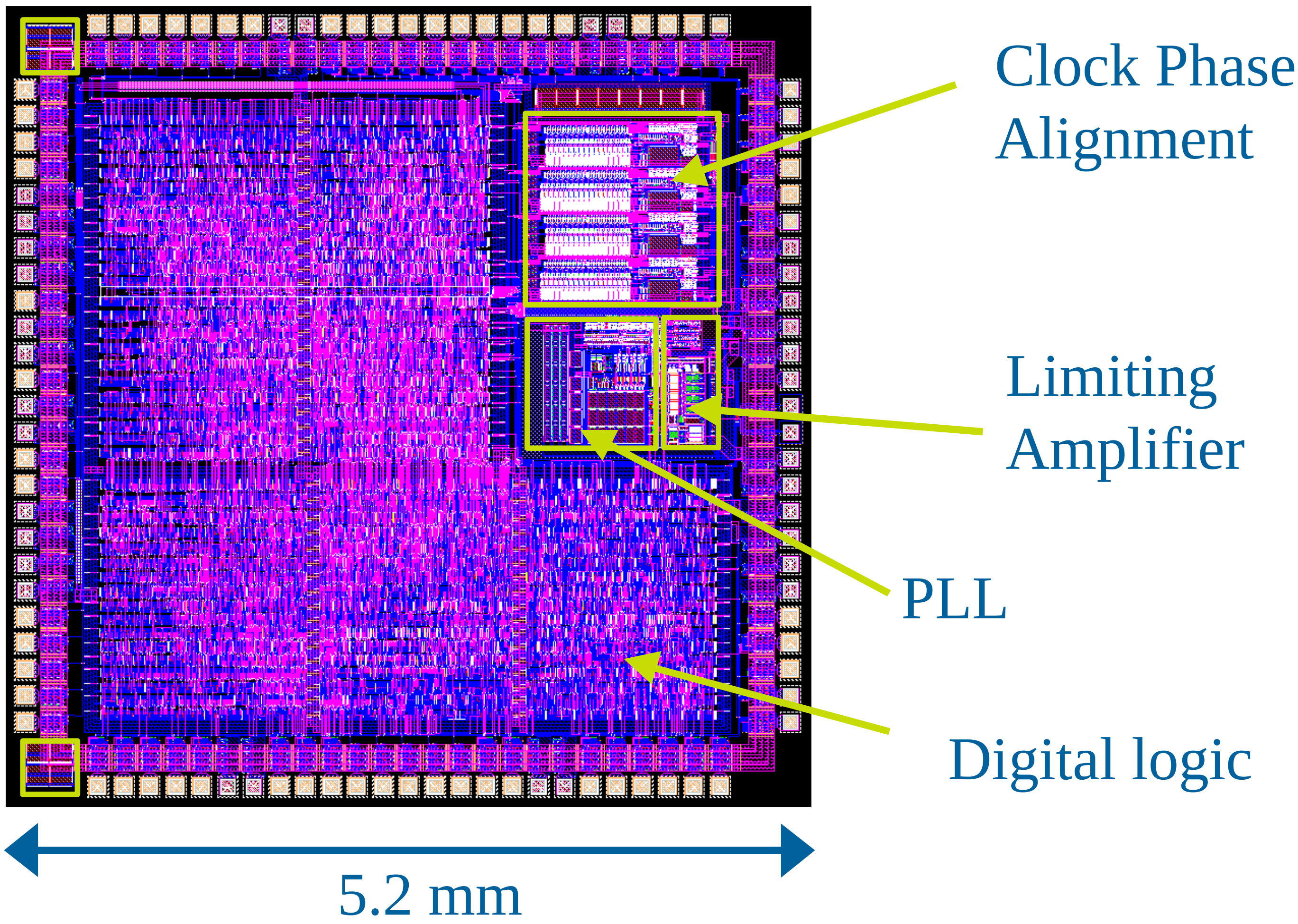
Pixel



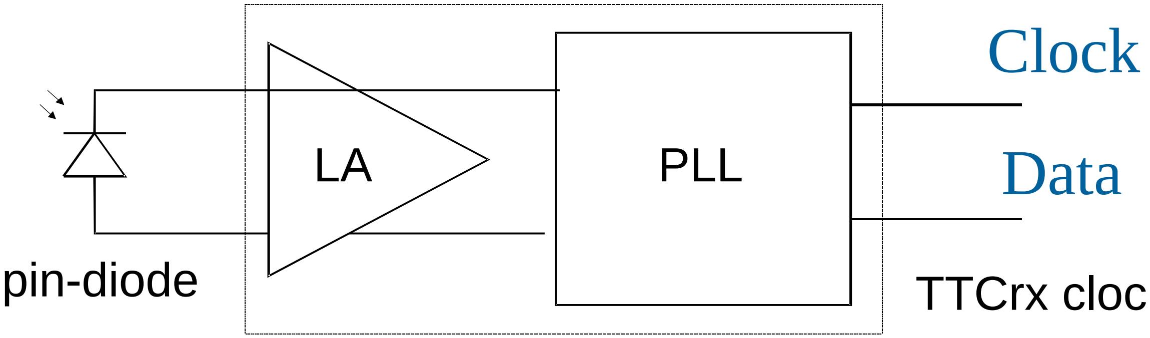


VCal
Preamplifier
Discriminator
3-bit TDAC
Select
Mask
HitBus
OR
Hit
PixClk
PixData
HitBus
Bias: IP, IL, IS, IF
Bias: ID, ITRIM, VTH, VCCD

TTC-Rx


Clock Phase Alignment
Limiting Amplifier
PLL
Digital logic
5.2 mm

TTC-Rx



TTCrx clock and data recovery part

Clock deskew function

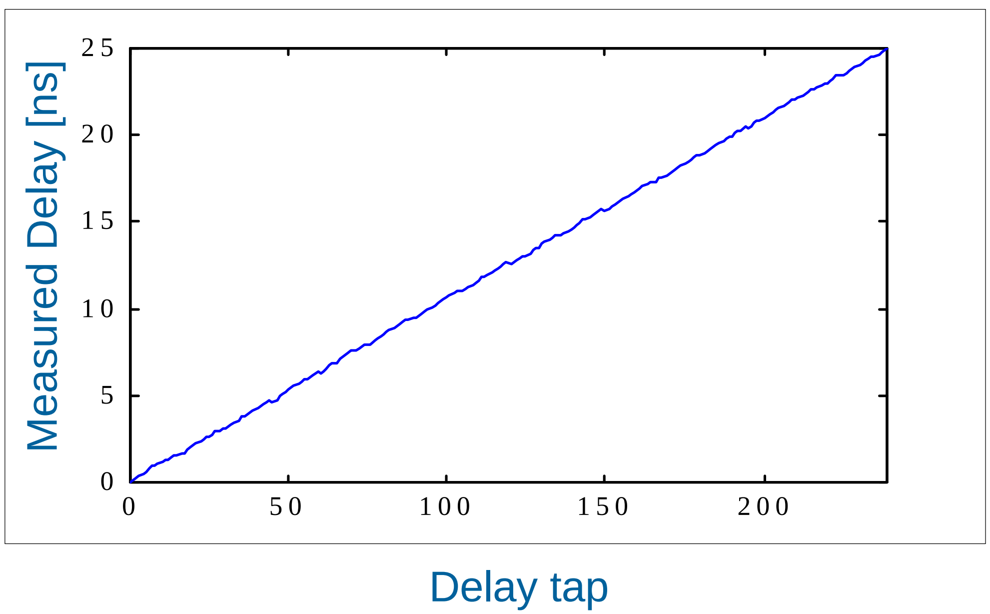
Δ = 104.8 ps

σ_{diff} = 48 ps

pp_{diff} = ±162 ps

σ_{int} = 80 ps

pp_{int} = ±185 ps



General Design Issues

DIGITAL

• Irradiation results in additional speed degradation (Vt drift, mobility degradation)

• Power consumption change before/after irradiation not under control (design dependant)

• SEU is an issue

ANALOGUE

• All aspects of "analogue" functions are affected by radiation : noise, offsets, stability, BW, operating point

• Control over biasing voltages or currents (when possible) allows some compensation of radiation effects

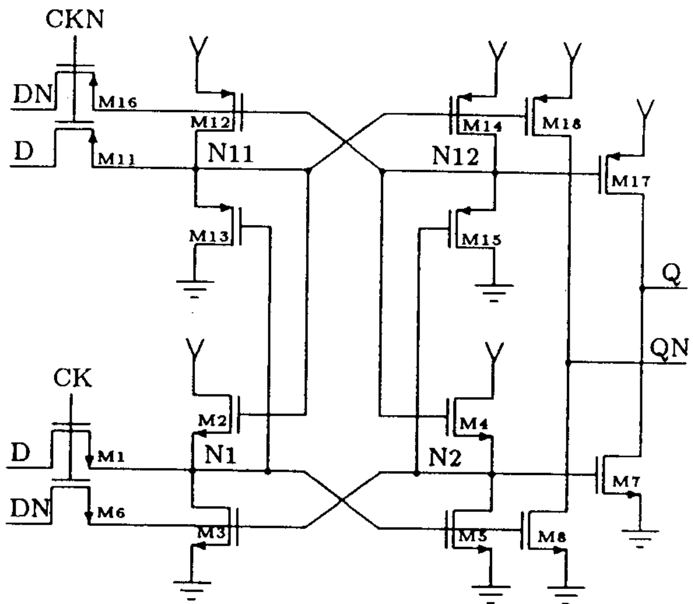
• SEU (generally) not an issue

SEU design solutions

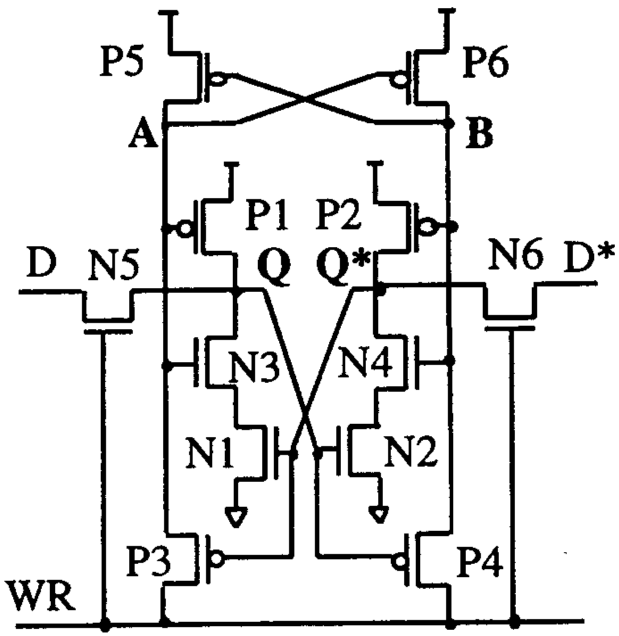
Different solutions depending on "severity"

- SEU-free logic :
  - double redundancy + major voting circuitry
  - simple redundancy + error detection
- SEU-detection :
  - Error detection techniques
  - Watchdog
- SEU at system level :
  - Redundancy & EDAC
  - Status Read & Reinitialisation
  - Watchdog & Reinitialisation

SEU resistant design



SEU tolerant RAM cell



HIT1 RAM cell

SEU risk vs. Application

SEU remedy is dependant on risk/cost :

In "LHC" Experiment :

SEU in data block is acceptable (add. Noise)
SEU in control functions results in loss of function until reinitialisation is done

Redundancy implementation is limited by constraints on available space, system BW

In Space : Redundancy and error correction are generally used

Digital Design Issue

Irradiation effect generally is additional speed penalty :

Avoid complex gates structures

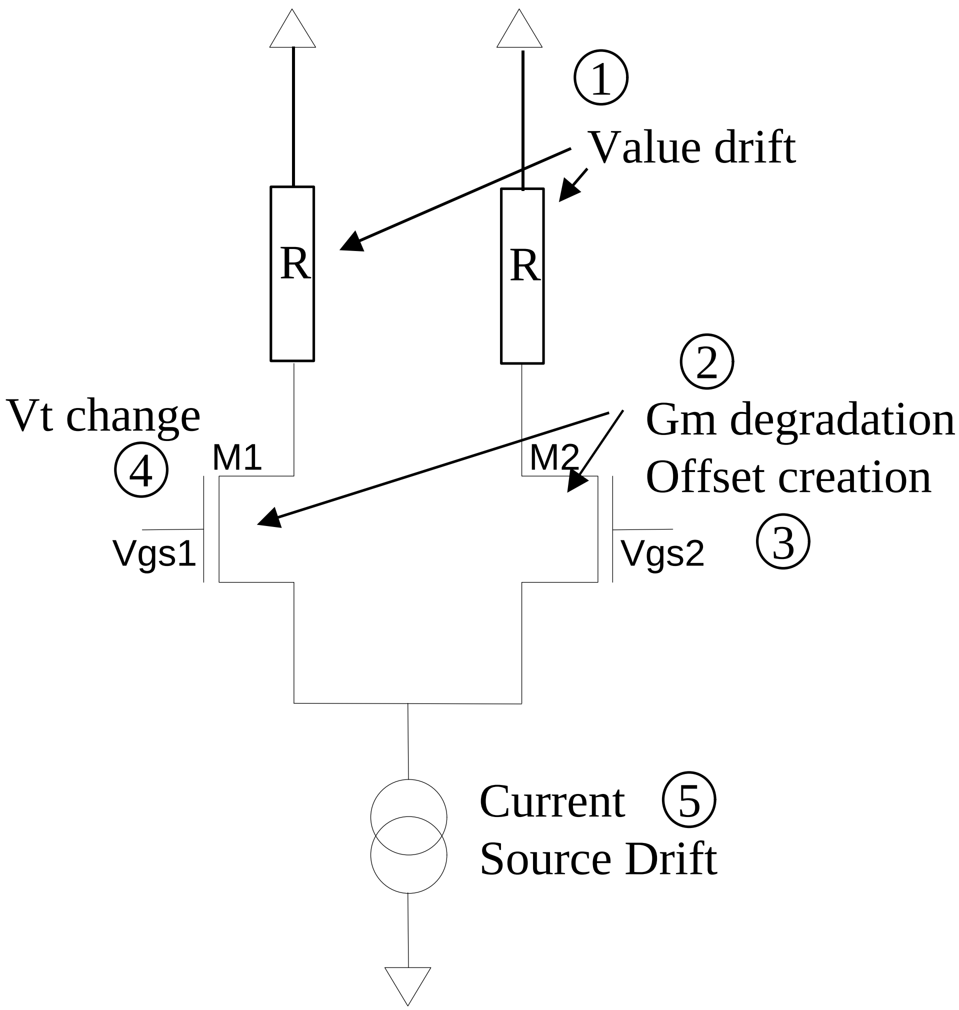
Rad-Hard Technologies (low volume process) results in limited manufacturer control over technology (compared to standard process) :

Avoid complex gates structures

Avoid dynamic logic if not needed

Digital Design Issue

Analog Design Issues



① ④ ⑤ = Operating point loss

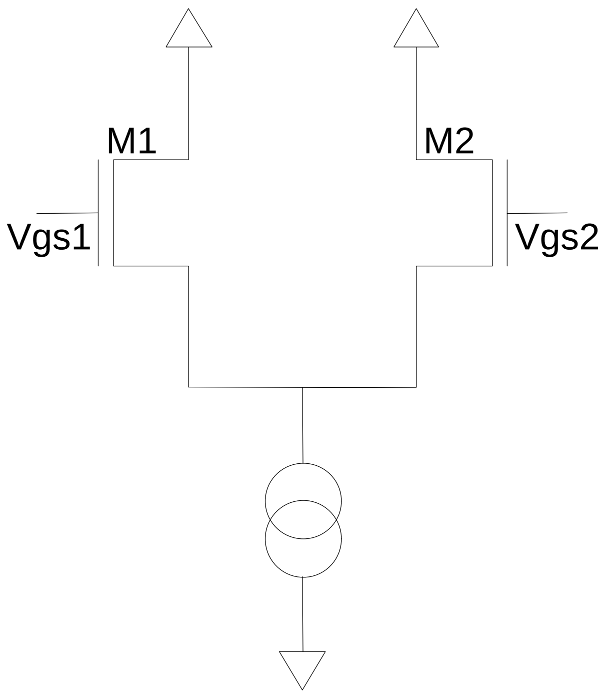
③ = Offset Increase

② ⑤ = Noise change

① ② ⑤ = BandWidth Change

Analog Design Issues

Amplifier offset



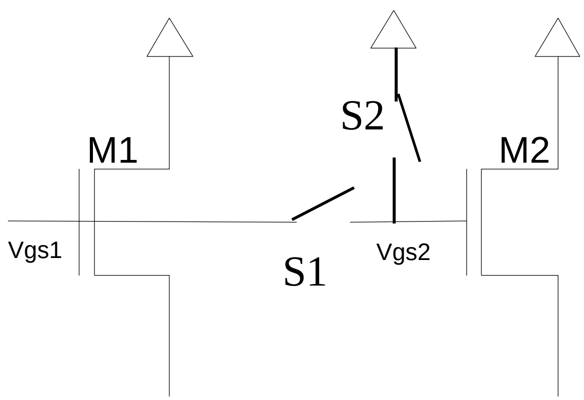
If during operation under irradiation, Vgs1 is almost always less than Vgs2, Vt drifts for M1 or M2 are different :

Large input offset creation

This situation is frequent for comparators, used for input level detection, threshold discrimination, etc ...

Analog Design Issues

Current mirror switching :



Vt drift on M2 depends on S1/S2 status during irradiation :

M2 current is different from M1 current
if S2 closed, S1 open during irradiation

A First Summary

RAD-HARD TECHNOLOGY IS EFFECTIVE

- Proven functionality and performance up to “LHC Experiments” dose

BUT

- Low Volume Production is an issue for manufacturer
- Designs are not conventional (from HEP users side)
- Radiation environment not completely “understood”

Threshold spread - does matching degrades after irradiation

24 GeV protons
3 x 10^{14} p/cm^2

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PostScript printer, but not to
other types of printers.

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with a preview included in it.
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PostScript printer, but not to
other types of printers.

Threshold spread - does matching degrades after irradiation

Neutrons

2 x 10^{14} n/cm^2

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ThrBeforeNoT.eps
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with a preview included in it.
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other types of printers.

Threshold spread - does matching degrades after irradiation

10 keV X-ray
10 Mrad

Title:
D:\ABCDMODXRAY\W7TRIM0215\matchnoirr.eps
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with a preview included in it.
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other types of printers.

Title:
D:\ABCDMODXRAY\W7TRIM0215\matcha10.eps
Creator:
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Preview:
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with a preview included in it.
Comment:
This EPS picture will print to a
PostScript printer, but not to
other types of printers.

Observations:

•matching degrades more after proton irradiation compared to neutron irradiation for comparable fluences

•no degradation of matching after X-ray irradiation

A Second Summary

RAD-HARD TECHNOLOGY IS :

- SEL/SEU resistance
- Foundry guaranties parameters drift values after irradiation

BUT

- Design time is “longer” than conventional technology
- Design characterisation & validation is “longer” than conventional technology