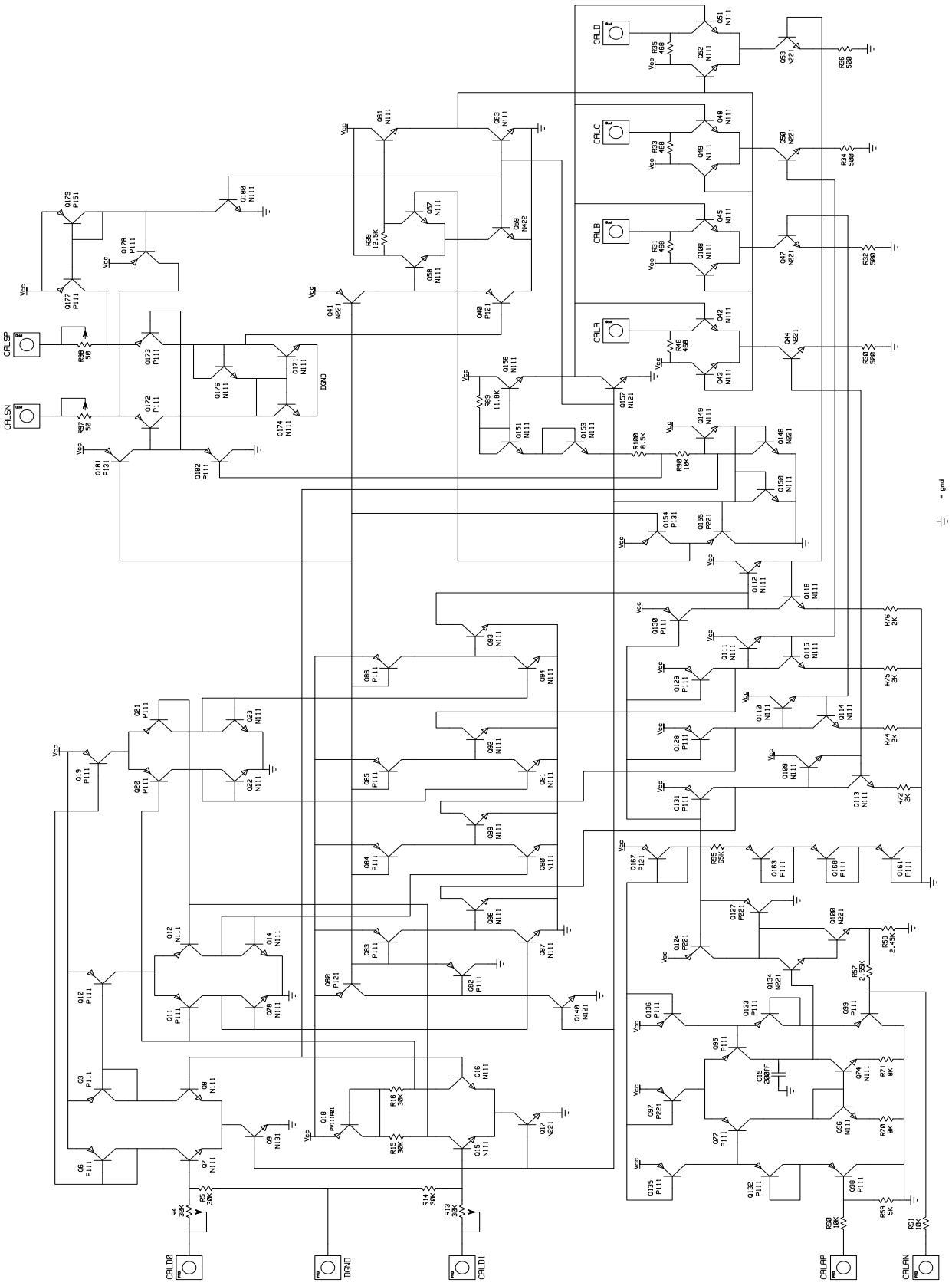


Figure 13. Calibration network schematic. p-strip readout IC

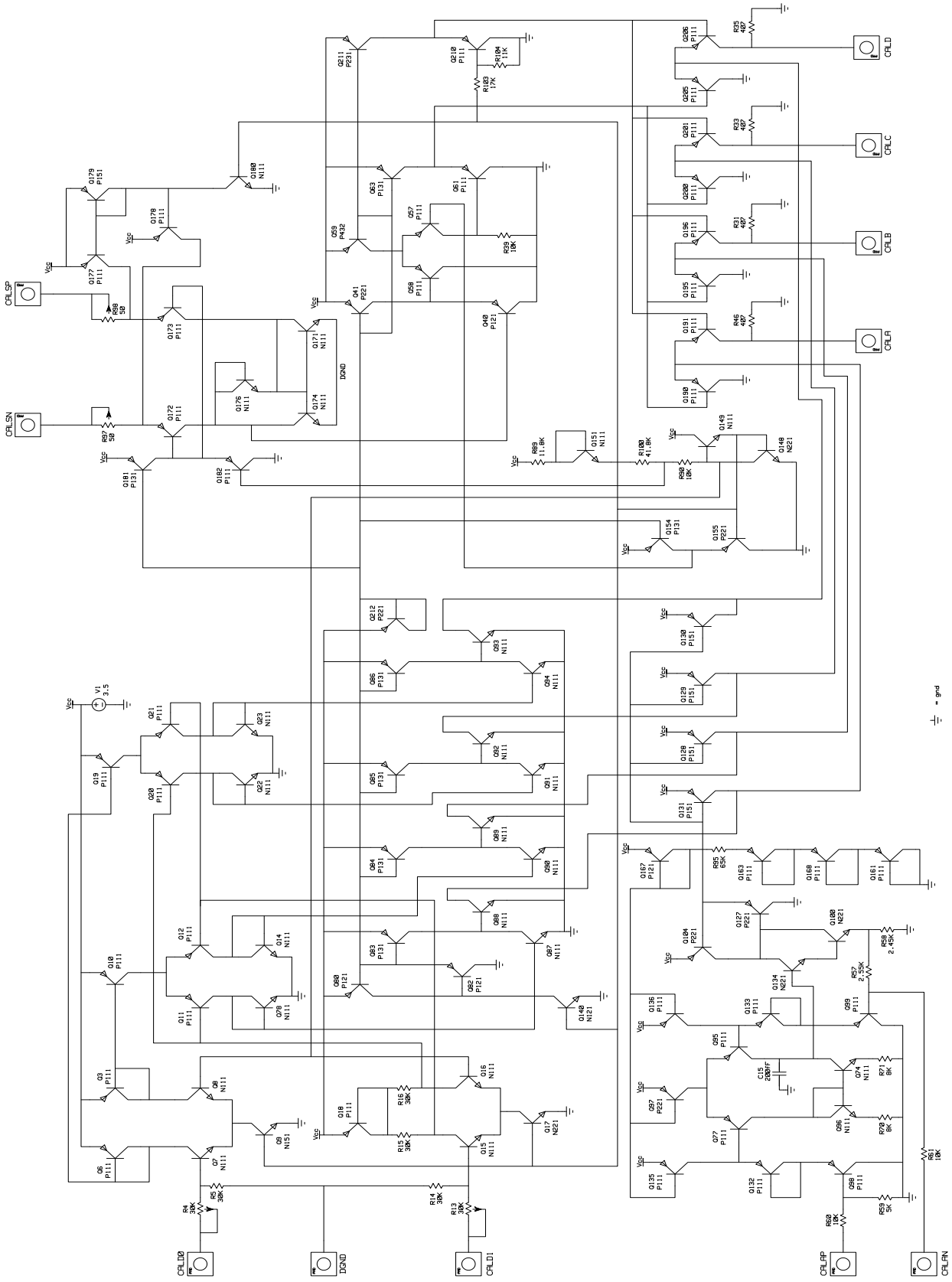


Figure 12. Calibration network schematic. n-strip readout IC

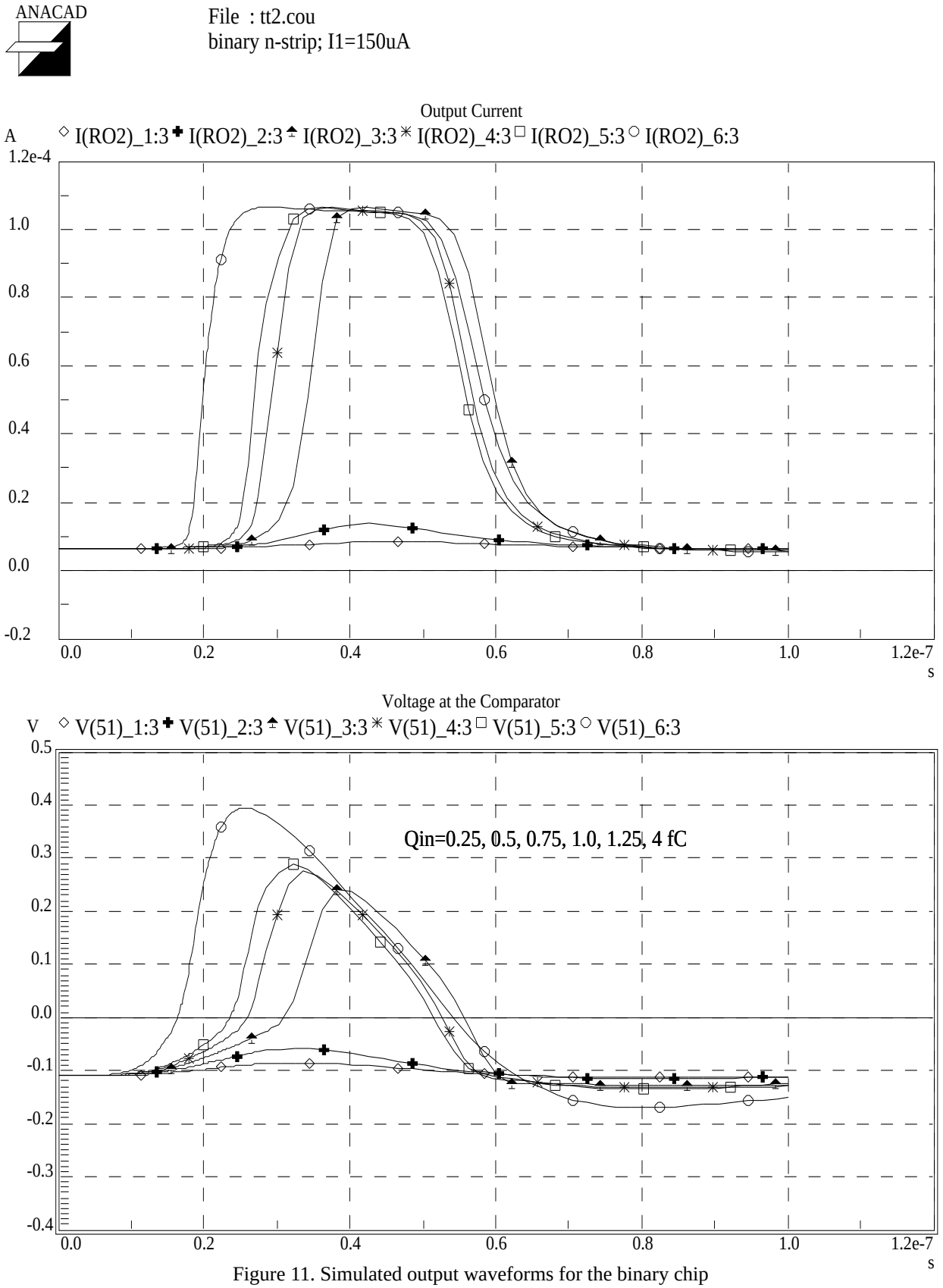
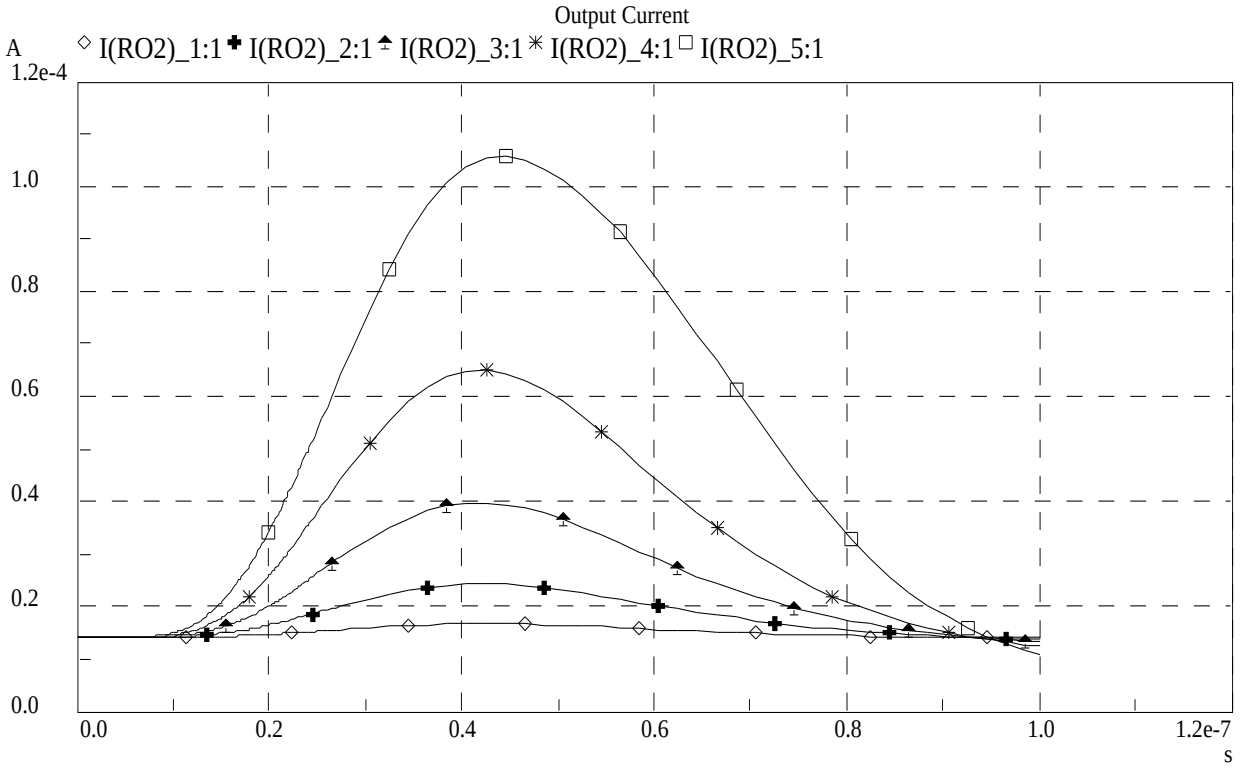


Figure 11. Simulated output waveforms for the binary chip

analog p-strip; I1=150uA



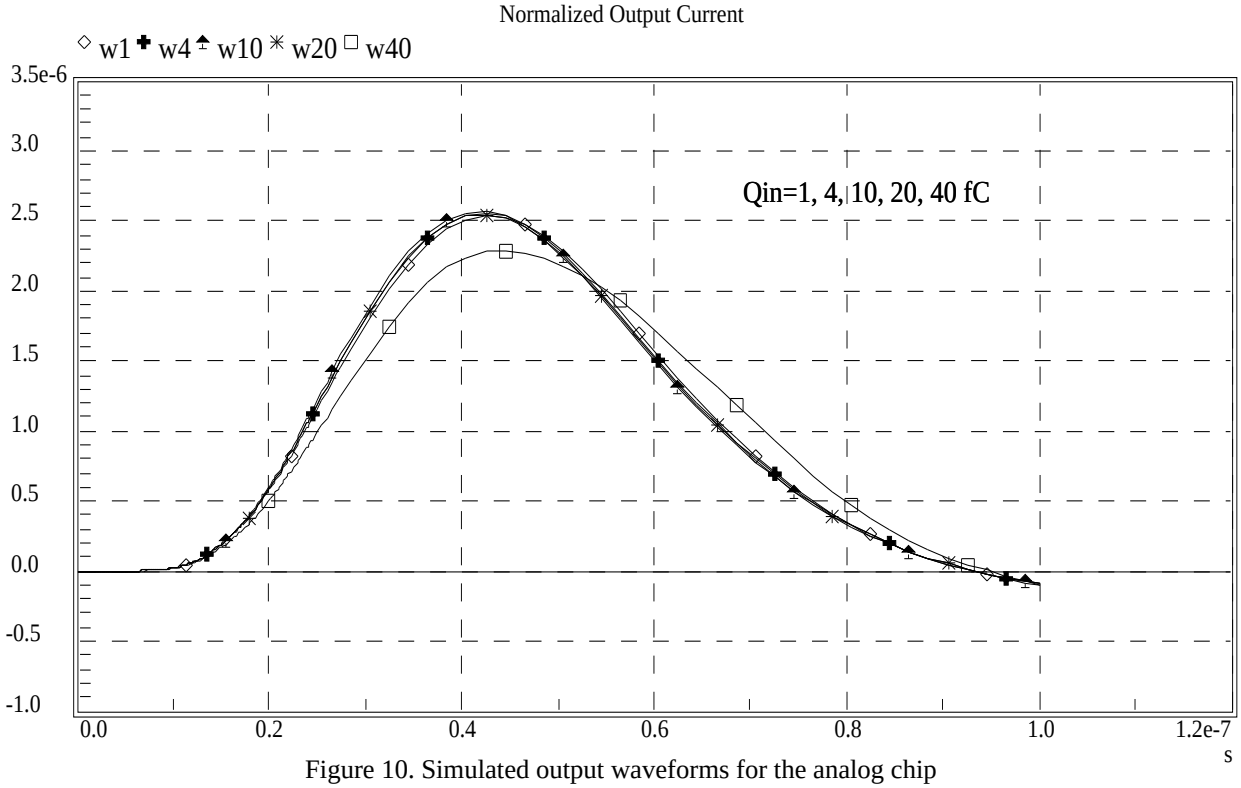


Figure 10. Simulated output waveforms for the analog chip

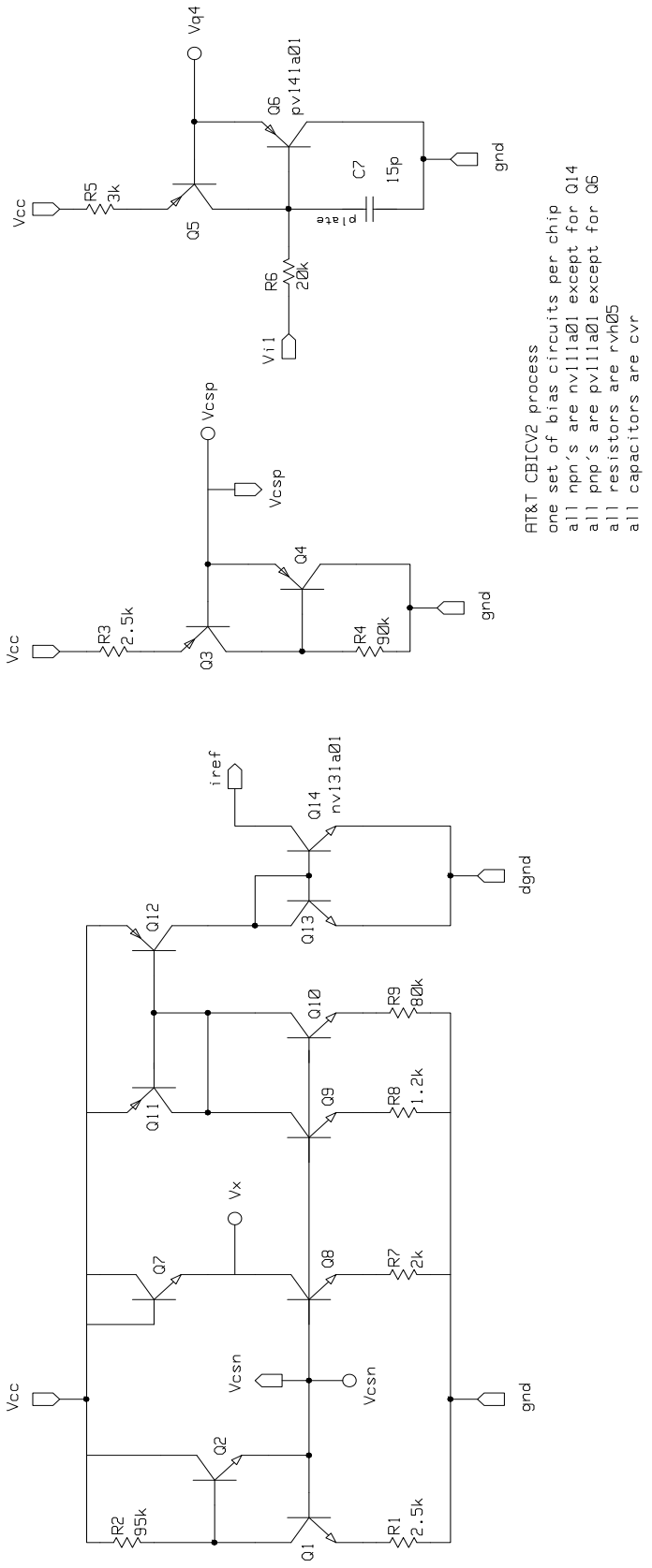


Figure 9. Bias network schematic. Binary readout IC

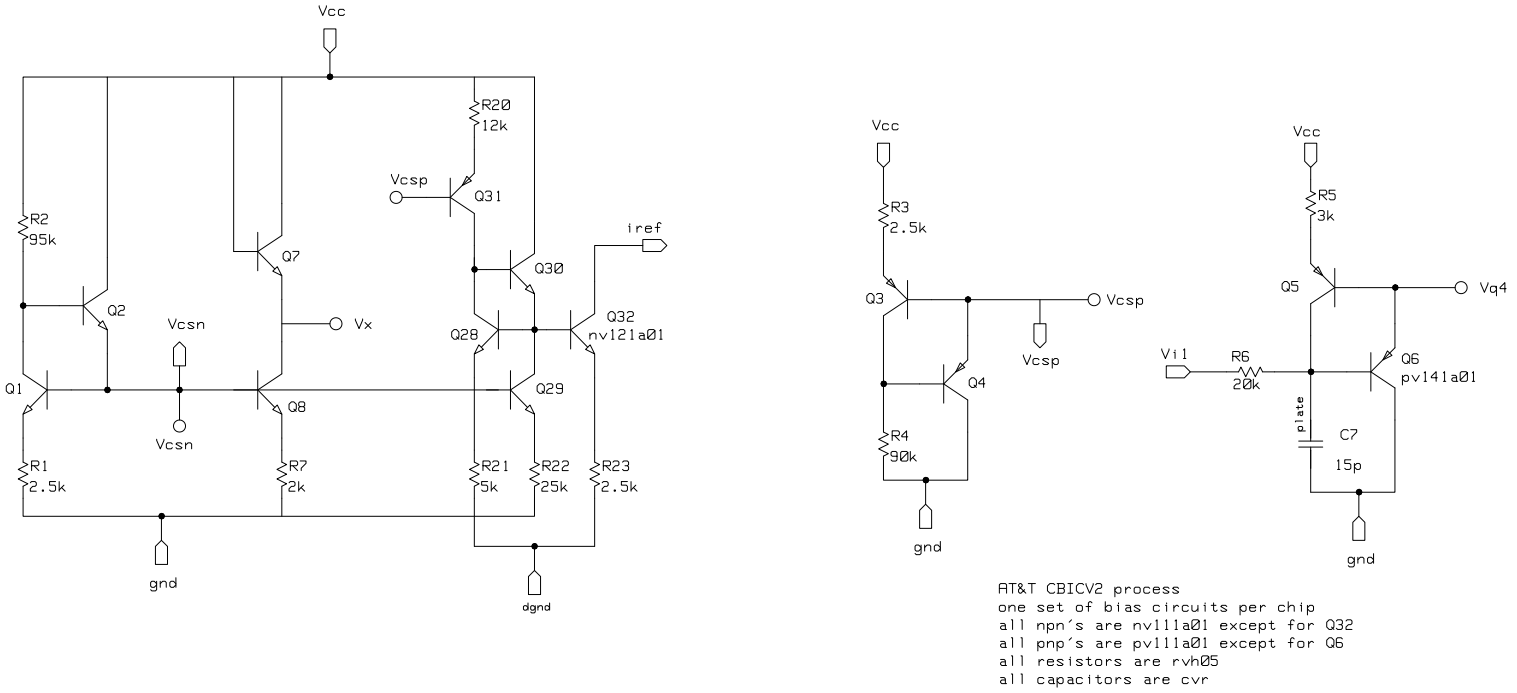


Figure 8. Bias network schematic. Analog readout IC

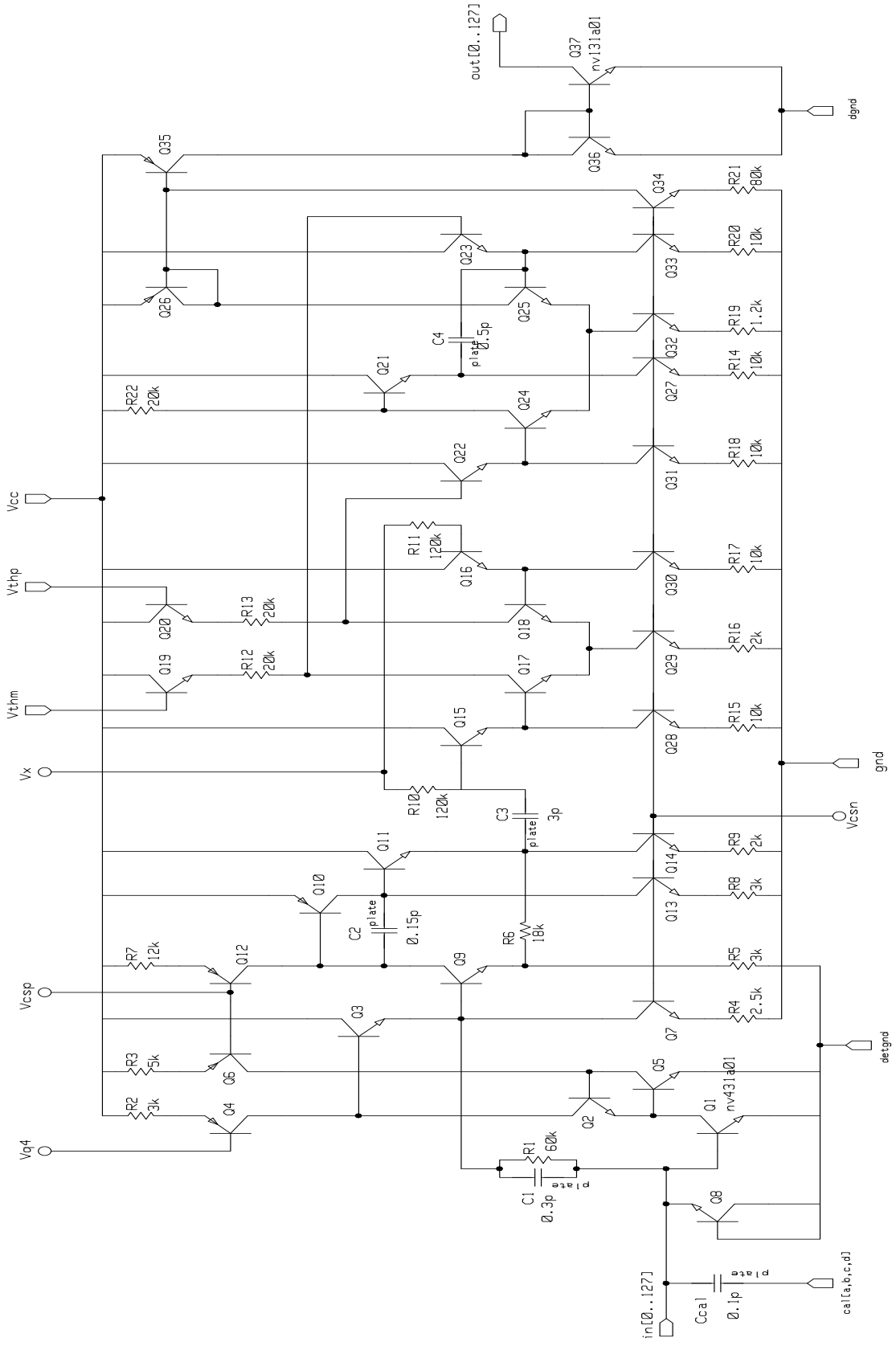


Figure 7. Channel schematic. Binary p-strip readout IC

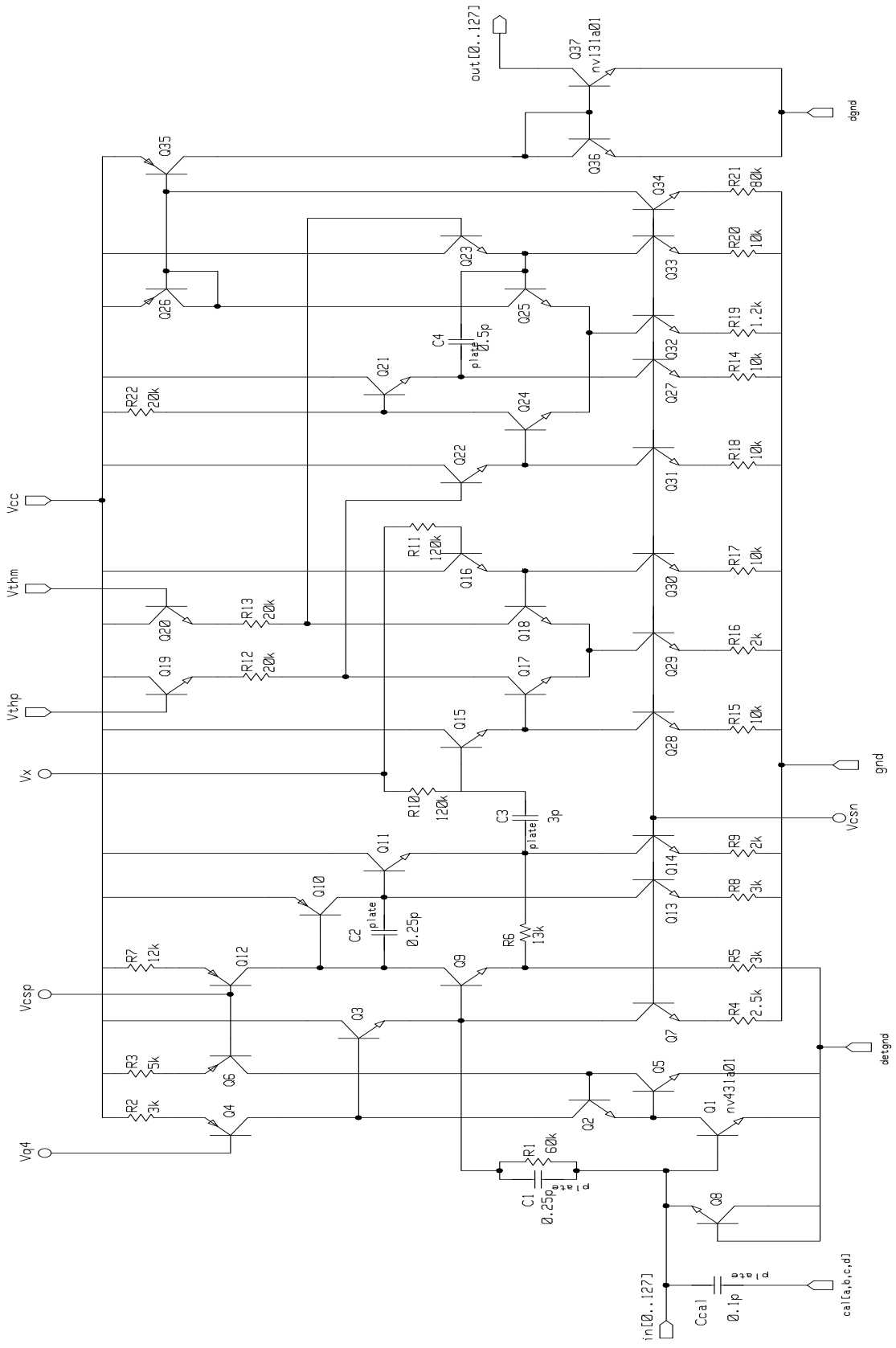


Figure 6. Channel schematic. Binary n-strip readout IC

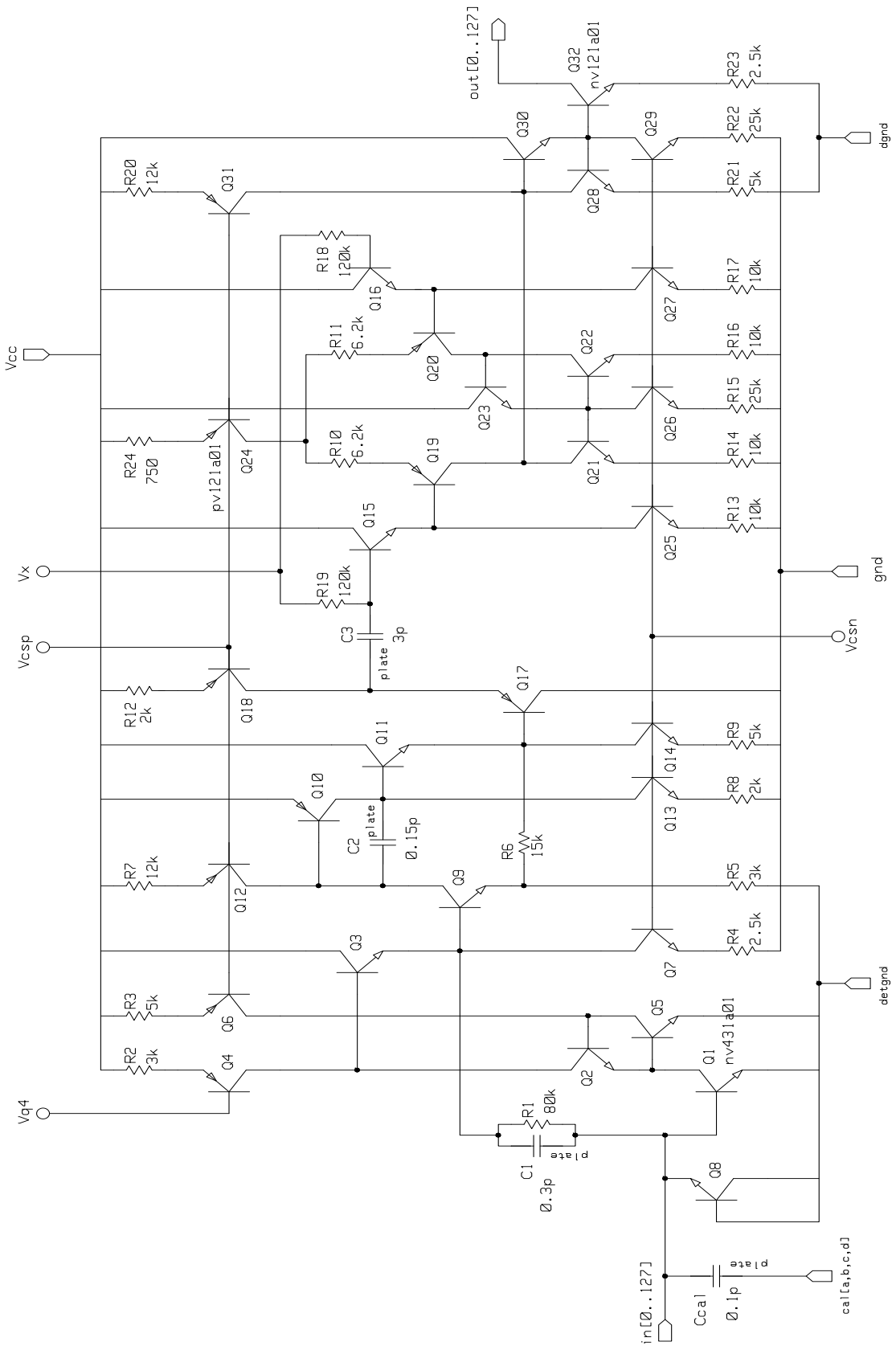


Figure 5. Channel schematic. Analog p-strip readout IC

AT&T CBICV2 process
all npns are nv111a01 except for Q1 and Q32
all pnps are pv111a01 except for Q24
all resistors are rvh05
all capacitors are cvr

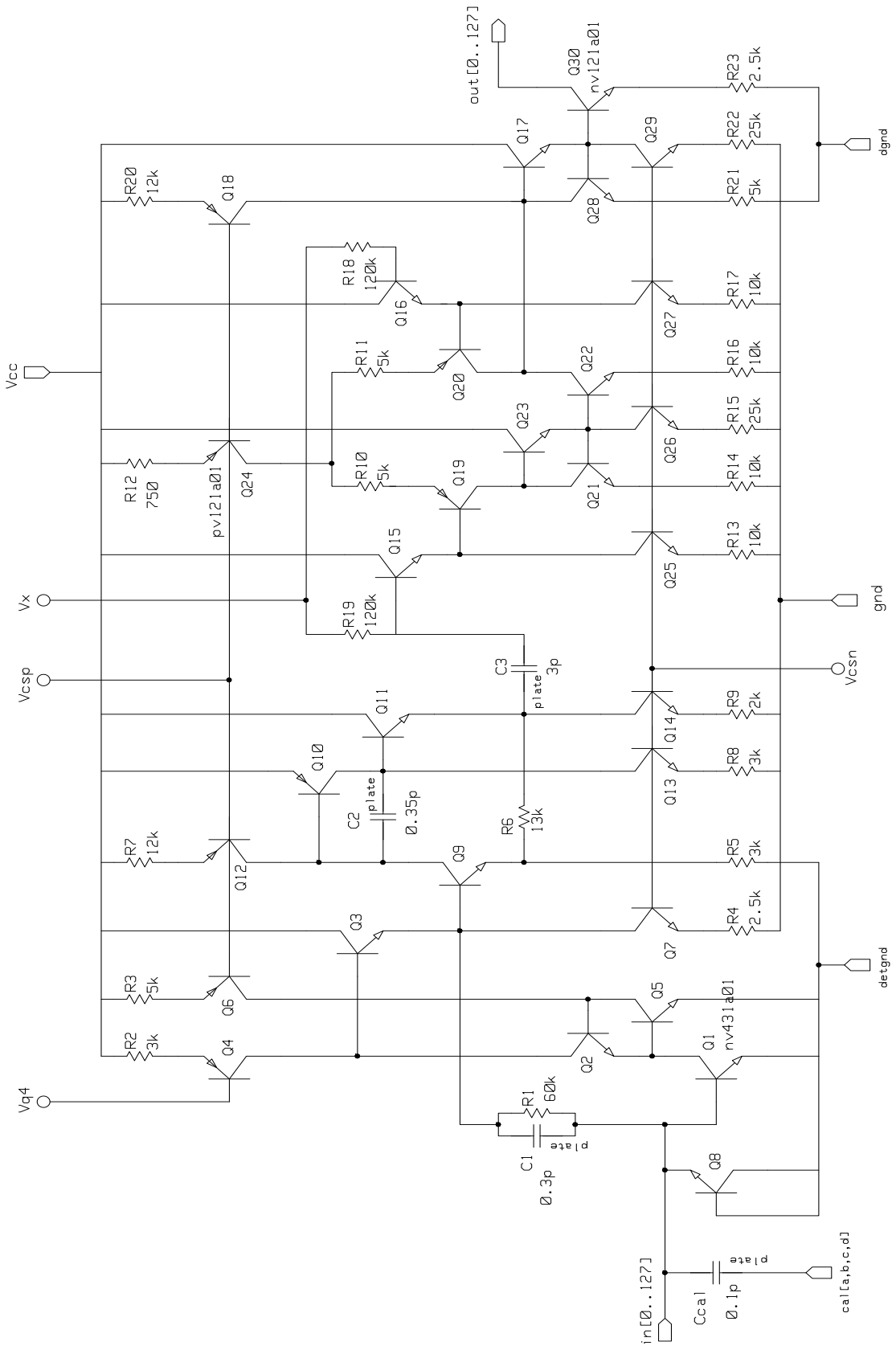


Figure 4. Channel schematic. Analog n-strip readout IC

Figure 3. Binary readout IC outline

Figure 2. Analog readout IC outline

signal is a differential signal carried on two pads **calsp** and **calsn** which are intended to be each driven by a PMOS open drain designed to source current. The signal should be quiescently in the “inactive state” with current sourced by the **calsp** pad and not sourced by the **calsn** pad. A strobe pulse consists of the two pads going to the “active state” (current not sourced by the **calsp** pad and sourced by the **calsn** pad), remaining in the “active state” for the required time (~400 ns) and then returning to the “inactive state”. The electrical specifications for the two single ended address signals **cald0** and **cald1** are shown in Table 5. The electrical specifications for the differential pair forming the calibration strobe signal are given in Table 6. It is assumed that the quiescent condition is with **calsp** in the “On” state

	Minimum	Nominal	Maximum	
“Off” State Current	0	0	5	μA
“On” State Current	70	100	150	μA
“On” State Voltage	3.2	3.3	3.5	V
Output Impedance	20			kΩ
Rise Time	0.5	1.0	5.0	ns
Duration		400		ns

Table 6: Electrical specifications for **calsp** and **calsn**

and **calsn** in the “Off” state. When the strobe pulse is active, **calsp** goes to the “Off” state and **calsn** goes to the “On” state for the duration of the pulse. In both states the receiver biases the connection. The electrical specifications for the differential dc amplitude controls are indicated in Table 7. The maximum calibration range is 12 fC. The inputs **calap** and **calan** have unbalanced input currents. The input **calan** sources up to 30 μA of current for 1 Volt differential input while **calap** looks like a 15 kΩ load to ground.

	Minimum	Nominal	Maximum		Input Resistance [kΩ]
calan	0.1	0.5	1.0	V	12.5
calap	0.1	1.0	2.5	V	15
V(calap) - V(calan)	0	0.1 ($\Rightarrow$ 1 fC)	1.2	V	

Table 7: Electrical specifications for **calan** and **calap**

References

[1] I. Kipnis, H. Spieler and T. Collins, “An analog front-end bipolar-transistor integrated circuit for the SDC silicon tracker,” *IEEE Transactions on Nuclear Science*, vol. 41, no. 4, pp. 1095-1103, Aug. 1994.

[2] E. Spencer *et al*., “A fast shaping low power amplifier-comparator integrated circuit for silicon strip detectors,” in *Proc. IEEE Nuclear Science Symposium*, 1994.

Cal Input Step (V) = Qcal (C) / 0.1 pF (e.g. V = 40 mV, for a 4 fC signal)

The polarity of the leading voltage step should be positive for the p-strip and negative for the n-strip readout chips. The calibration lines are connected to the channels following the pattern indicated in Table 4 (see also Figure 1).

As an alternative to the direct calibration method described above, and to avoid distributing a fast (t_r ~ 10 ns) calibration pulse throughout a large system, the CAFE chips feature a custom on-chip calibration circuit requiring no fast analog signals. Figures 12 and 13 present the calibration circuits for the n-strip (analog and binary) and p-strip (analog and binary) ICs, respectively. The calibration circuits were designed by Ned Spencer from the University of California at Santa Cruz. Credit, and all difficult questions, should go to him (ned@scipp.ucsc.edu, 408-459-2694).

The custom calibration network consists of a chopper circuit which will create the necessary voltage step when supplied with a dc voltage to set the height of the step and a strobe pulse to determine the timing of the step. Two address signals are provided to determine to which one of the four buses the step will be applied (see Table 4). The dc voltage is applied as a differential dc level to two pads (**calap** and **calan**) on the top and bottom edge (as viewed in Figures 2 and 3) of the IC. The two address lines are single-ended voltage levels applied to two pads (**cald0** and **cald1**) located at the back edge of the CAFE IC as are the two pads (**calsp** and **calsn**) for the differential strobe pulse. The dc level is applied differentially to make it immune to noise and dc offsets. The strobe pulse is expected to be a differential current signal driven by two complementary open drain outputs. This is to minimize any noise created during the strobe pulse which would be in time with the charge deposited at the input channels. The two address lines are allowed to be single-ended voltage levels because it is assumed that they are set a long time (relative to front-end shaping times) before any calibration strobe occurs and they must be held stable until long after the pulse is applied.

cald1	cald0		
0	0	cala	in3, in7, in11,..., in127
1	0	calb	in1, in5, in9,..., in125
0	1	calc	in2, in6, in10,..., in126
1	1	cald	in0, in4, in8,..., in124

Table 4: On- and off-chip calibration signals to channel mapping

The pads on the CAFE ICs connected directly to the four calibration buses are intended for use in single chip or module tests on the bench where circuitry external to the detector module can be made available. However, no such circuitry is envisioned for the final detector module. Therefore, for a fully assembled system, it is planned that the pipeline and signal processing IC (PPIC), which can be given directives via the module command line, can supply the address and strobe signals. The dc level to set the calibration amplitude can be supplied by a DAC (one per detector module) or brought on a cable to the module. This dc voltage can be daisy-chained from CAFE to CAFE as identical pads are available on both sides of the chip and the voltage drop due to current draw will be negligible.

The PPIC must provide the two address signals and a differential calibration strobe signal. All of these are applied to pads at the back edge of the CAFE ICs. The two address signals (**cald0** and **cald1**) are intended to be CMOS levels which should be controlled by the PPIC. The two signals should not be gated by any other calibration timing signal in the PPIC but rather be a fixed level, stable during the entire period of a calibration pulse. The strobe

	Minimum	Nominal	Maximum	
“1” State Level	3.8	4.0	6.4	V
“0” State Level	- 0.4	0	1.0	V
Current	56	68	80	μA
Rise Time			10	ns
Duration	Held by driver during entire cal operation			

Table 5: Electrical specifications for **cald0** and **cald1**

For the binary versions, **iref** gives the hit current of about 100 μA, to enable the digital pipeline IC to generate a digital threshold. The same dc conditions outlined above for the channel outputs apply to **iref**.

Bias and Control Signals

There are 5 separate dc signals (Table 3) required for the operation of the CAFE ICs. Some of the ground signals can be tied together off-chip on the mounting assembly. Table 3 shows the nominal current per chip for each supply.

Supply		Voltage [V]	Current per chip [mA]
Vcc	For I_{Vi1}= 150 ↔ 300 μA	3.5	45 ↔ 67
gnd	For I_{Vi1}= 150 ↔ 300 μA	0	22 ↔ 22
detgnd	For I_{Vi1}= 150 ↔ 300 μA	0	23 ↔ 45
dgnd	connected to the ground of the signal processing IC	0	1 (binary) 3 (analog)
Vi1	mirror current through the input transistor Q1	2 - (23k*I_{Vi1})	0.15 to 0.3
Vthp	binary versions only	3.5	0.012
Vthm	binary versions only Nominal threshold, Vth = 100 mV ⇒ Vthm = 3.4 V	Vthp - threshold	0.012

Table 3: Bias and control supplies

The current flowing out of the **Vi1** pad is equal to the collector current through the input transistor Q1. It can be adjusted from 150 to 300 μA, to optimize the noise performance (see Table 1). There is an on-chip 20 kΩ resistor in series with **Vi1** (Figures 8 and 9), to enable a number of chips on a module to be controlled in parallel from a voltage supply. Depending on the noise performance required, an off-chip resistor in series with **Vi1** could be added, to account for chip-to-chip resistor variations.

For the binary chips, the comparator threshold is applied differentially, and is given by **Vthp** minus **Vthm**. The signal **Vthp** should be referenced to the **Vcc** potential (3.5 V). The gain at the input of the comparator, where the threshold is set, is about 100 mV/fC. Figure 11 shows simulated waveforms at the input of the comparator for different input charges, with a threshold of 100 mV.

Calibration

The calibration operation in CAFE is performed, at the discretion and preference of the user, either by directly applying a fast analog voltage step or, by using the custom on-chip calibration circuit and providing a dc level plus some digital timing pulses. The CAFE chips are equipped with 100 fF calibration capacitors connected to the input node of each channel. Each capacitors is connected to one of four buses with every fourth channel connected to the same bus. When a voltage step is applied to one of these buses, the capacitors deposit charge into the front-end amplifiers which mimic the charge collected from a detector strip. At some point the voltage step must be neutralized with a reverse voltage step to bring the bus back to its quiescent state. This reverse voltage step must occur at a time after the initial voltage step which is long compared to the shaping time of the front-end circuit so as not to affect the signal to be processed.

There are four input pads (**cala**, **calb**, **calc** and **cald**) on the top and bottom edge (as viewed in Figures 2 and 3) which connect directly to these four calibration buses. Voltage steps can be applied directly to these four pads by external circuitry. If such direct access to the calibration buses is desired, ac coupling should be used to these pads, because the on-chip calibration circuit loads these buses with a 400 Ω resistor to either **Vcc** or **gnd** (depending on the polarity of the calibration circuit). The equivalence of voltage step amplitude to effective input charge is:

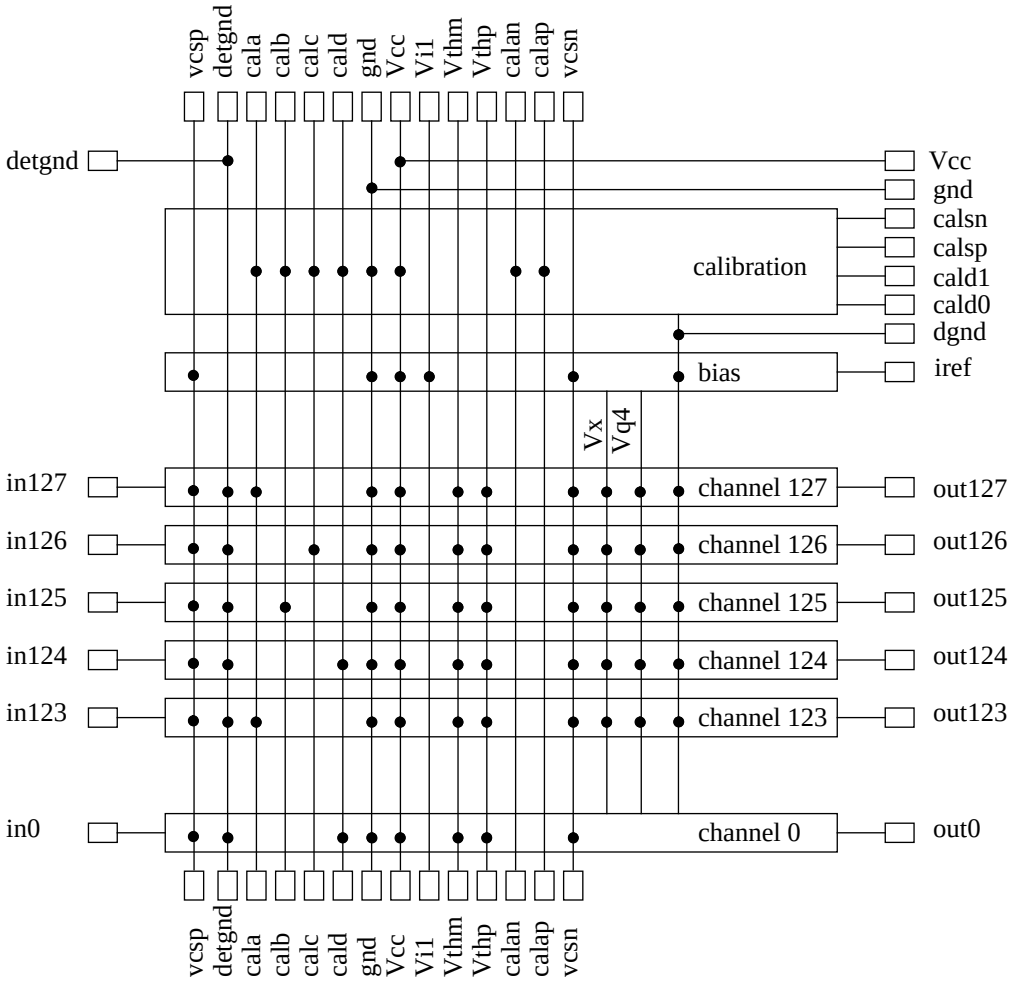


Figure 1. Outline schematic

protection diode to clamp the input node within a Vbe of **detgnd** in the event of a strip malfunction.

Channel Outputs

There are 128 open-collector outputs to connect to the PPICs. The output should be dc coupled. Under normal operating conditions the quiescent voltage at the output should be greater than a Vbe above **dgnd**, and less than 5 volts above **dgnd**, to prevent the output transistor from saturating or breaking down. For testing purposes it is still preferable to apply a bias voltage as indicated above. Experience with similar ICs suggest that the outputs may remain unconnected, without significant signal degradation due to current injection into the substrate. This, however, will have to be verified for the CAFE chips.

The output nodes should have a load time constant of 1 - 2 ns, to preserve the correct waveform. For chip-to-chip interconnect where the node capacitance is about ~ 1 pF, the equivalent input impedance of the receivers in the signal processor chip should be roughly less than 1 kΩ. For test purposes, 50 Ω amplifiers can be used.

For the analog ICs, the output has a quiescent current of 15 μA. The peak gain is 2.5 μA/fC with a limiting value of about 100 μA (corresponding to 10 MIPS). For the binary ICs, the output has a quiescent current of 6 μA and a hit current of about 100 μA. Figures 10 and 11 show simulated output waveforms for different input charges, for the analog and binary chips, respectively.

In addition to the 128 channel outputs, there is one open-collector dc signal named **iref**, that provides baseline information to the signal processing circuits. For the analog chips, **iref** supplies the quiescent current of about 15 μA.

Santa Cruz. The CAFE chips are optimized for a silicon strip detector having the characteristics indicated in Table 2.

DC Coupled		
Center-Tapped		
Strip Length	12	cm
Strip Resistance	25	Ω/cm
Strip Capacitance (n-strip)	1.5	pF/cm
Strip Capacitance (p-strip)	1.2	pF/cm
Maximum dc Leakage Current	2	μA/strip

Table 2: Silicon Strip Detector Characteristics

The ENC figures in Table 1 are for a single channel, delta current pulse, source capacitor, and pre-irradiation case. The noise analysis and simulated performance for multi-channel, post-irradiation and for the binary cases have been presented during the design reviews of the chip and are not included here because of their complexity. A summary of those results is available in the transparency copies of the ATLAS SCT Meeting, LBL, March 6-10, 1995. For further background reading, refer to [1], [2].

Chip Outline

Figure 1 shows an outline schematic of the binary ICs (the analog outlines are identical except for the signals Vthp and Vthm not being present). There are 128 front-end channels, one bias network, and one calibration circuit per IC. Some of the control and bias signals are bussed across the chip and have pads at the top edge and bottom edge of the die. The top and bottom pads are duplicated to provide redundancy and ease of assembly (they can be wire bonded from either side). To avoid current loops, a given control or bias signal should not be connected from both sides; only from the most convenient one. The preference is to connect the top row, therefore wider pads are provided there.

Also, to allow assembling two dice next to each other (to directly connect to a 50 μm pitch detector), additional pads for the power supplies **Vcc**, **gnd** and **detgnd** are provided at the input and output pad columns. The preference is to connect the supplies to the pads on the top or bottom edges, and not to pads on the front or back edges. Again, to prevent current loops, a given supply should not be brought into the chip on two different pads.

The analog and binary chip outlines in Figures 2 and 3, document the dimension and location of all the pads. The finished (separated) die size is approximately 4,425 μm x 6,200 μm. The input pads on the front edge of the IC are on a 47 μm pitch. The output pads on the back edge are on a 44.5 μm pitch. Input and output pads have a passivation opening of 130 μm x 60 μm. Each 100 mm wafer has approximately 58 dice from each type. The back-side of the die is polished silicon. It is electrically connected to the **gnd** pad (see below in the bias section) and should not be connected externally to any other potential. Preferably, the back-side should be connected to the ground plane carrying the **gnd** potential. All pads are fabricated with a single layer of 1.3 μm thick TiPtAu metal.

The circuit schematics of a single channel, for each of the four chip versions, are shown in Figures 4 through 7. The analog n- and p-strip readout ICs use the same bias network and identical chip outline. The binary n- and p-strip readout ICs use the same bias network and identical chip outline.

All reference currents and voltages are generated on chip. Figures 8 and 9 present the bias networks for the analog and binary chips, respectively. Pads for the reference nodes **vcsn** and **vcsp** are available on the top and bottom edges for testing and monitoring purposes and should not be bonded out. Reference nodes **Vx** and **Vq4** are generated by the bias networks and distributed to all channels but are not brought out to pads.

Channel Inputs

There are 128 inputs to connect to the silicon detector. Their quiescent voltage is a Vbe (approximately 0.7 V) above **detgnd**. For testing purposes they can be left open or be connected to external capacitors. If a dc connection is made, the maximum dc current that can flow into or out of a channel is specified at 2 μA. All channel inputs have a

From: Issy Kipnis, Lawrence Berkeley Laboratory, (510) 486-4619, i_kipnis@lbl.gov

To: ATLAS Semiconductor Tracker Collaboration

Subject: CAFE: A Complementary Bipolar Analog Front-End Integrated Circuit for the ATLAS SCT

This is the documentation on the CAFE chip: a 128-channel integrated circuit (IC) containing the analog front-end electronics for the silicon strip detectors in the ATLAS semiconductor tracker (SCT). The circuit was fabricated by AT&T Microelectronics in Reading, PA, using their 10 GHz f_T, complementary bipolar CBIC-V2 technology. This document does not cover the design details of the IC, rather, it is intended to be a "user's reference".

In each of the proposed ATLAS front-end architecture options, detector signals are amplified, shaped, and stored in on-detector pipelines until a read-out request is prompted. The amplification and shaping functions are, in principle, common to all options. The storage and further signal processing varies depending on the choice of architecture. Accordingly, two versions of the front-end IC have been developed: (1) an analog circuit, consisting of a low-noise integrator, shaper and a voltage-to-current converter, to feed an analog pipeline processor integrated circuit (PPIC), and (2) a binary circuit, consisting of a low-noise integrator, shaper and discriminator, to drive a digital PPIC. Further, it is not yet known whether the readout electronics will be connected to n- or p-strip detectors, therefore both options were developed for each of the above version. In all, the CAFE chip comes in four flavors:

CAFE-an	analog n-strip readout
CAFE-ap	analog p-strip readout
CAFE-bn	binary n-strip readout
CAFE-bp	binary p-strip readout

The expected simulated performance of the CAFE chips is shown in Table 1. The design of the IC was performed using realistic simulated current waveforms from both sides of the silicon strip detector, as provided by UC

Analog Readout			
Gain		2.5	μA/fC
Peaking Time		25	ns
Limiting Signal Range		10	MIPS
Double Pulse Resolution (Qs=4 fC)		50	ns
Double Pulse Gain Inaccuracy		< 10	%
Equivalent Noise Charge	Pd=1.2 mW, I_{Vi1}=150 μA	400 + 50/pF	el. rms
	Pd=1.8 mW, I_{Vi1}=300 μA	550 + 33/pF	
Supply Voltage		3.5	V
Power Dissipation per Channel		1.2 - 1.8	mW
Binary Readout			
Gain at the Comparator		100	mV/fC
Peaking Time		25	ns
Output Pulse Amplitude		100	μA
Double Pulse Resolution (Qs=4 fC)		50	ns
Time Walk (Qs=1.25 - 10 fC)		< 15	ns
Supply Voltage		3.5	V
Power Dissipation per Channel		1.2 - 1.8	mW

Table 1: Simulated Performance of the CAFE chips