3.3
Pin Description

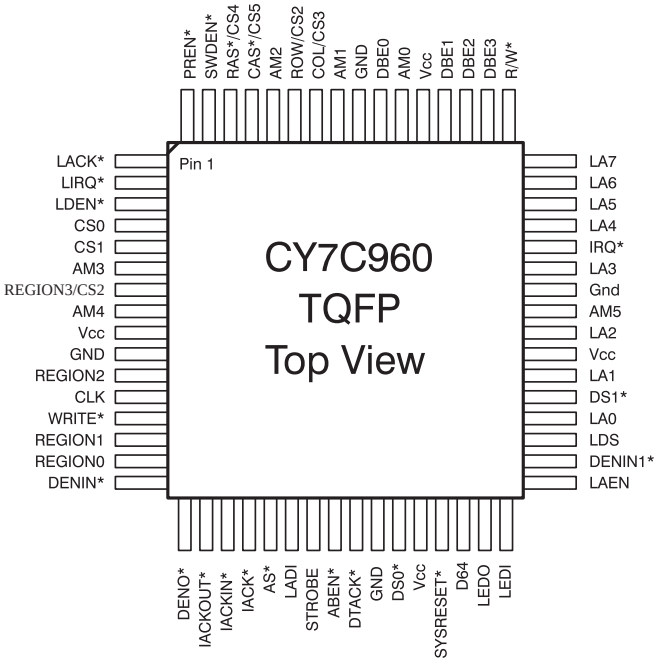

Figure 3−8. CY7C960 Pin Assignment (TQFP)

3.3.1 VMEbus Signals

AM[5:0] − VMEbus Address Modifier

Input: Yes
Output: No

Signals AM[5:0] are the VMEbus Address Modifier inputs. These input signals are used to decode the VMEbus transaction type. The CY7C960 provides support for all predefined and user-defined VMEbus Address Modifiers.

AS* – VMEbus Address Strobe

Input: Yes
Output: No
Active: Low

Address Strobe is the VMEbus signal that informs VMEbus slaves that a valid address is on the VMEbus. This signal is used by the CY7C960 to qualify the VMEbus Address Modifiers AM[5:0] and REGION[3:0] inputs to determine if a slave cycle should be performed.

DS0*, DS1* – VMEbus Data Strobe

Input: Yes
Output: No
Active: Low

DS0* and DS1* are the VMEbus Data Strobe inputs. These signals inform the CY7C960 that either an address broadcast or data phase of the VMEbus cycle has begun. These signals in conjunction with the VMEbus LWORD* and LA[1] signals encode the data transfer width or number of bytes, 1 through 4. This information is necessary to enable the appropriate CY7C964 data bytes.

IRQ* – VMEbus Interrupt Request

Input: No
Output: Yes
Drive: 48 mA
Active: Low

The IRQ* signal is driven by the CY7C960 to indicate that the local interrupt request signal is active. The IRQ* pin should be connected to one of the 7 VMEbus interrupt request signals IRQ[7..1]* in order to implement a standard VMEbus interrupt requester. This signal may also be used, following a power-on reset, as part of the configuration protocol using the VMEbus to load the device configuration registers. In this case it shall be connected to VMEbus IRQ2*.

IACK* – VMEbus Interrupt

Input: Yes
Output: No
Active: Low

The IACK* signal further qualifies the VMEbus address transaction. If this signal is asserted the CY7C960 decodes the VMEbus address transaction as an Interrupt Acknowl-

edge cycle. During the interrupt acknowledge cycle the CY7C960 will match three bits of the VMEbus address (A[3:1]) against the user-programmed internal level. If the levels match, IACKIN* is received active, and a VMEbus interrupt is pending from the device, then the VMEbus interrupt acknowledge is completed by the enabling of a vector onto the VME data bus. This vector is user defined, and enabled using the LDEN* signal. CY7C960 assumes that it is an 8-bit interrupter, and hence responds to all interrupt acknowledge cycles without regard to the size of the STATUS/ID requested. If a VMEbus interrupt is not pending or IACKIN* is not asserted to the device this VMEbus address cycle will be disregarded.

IACKIN* – VMEbus Interrupt Acknowledge In

Input: Yes
Output: No
Active: Low

The IACKIN* signal informs the CY7C960 that no other up-stream (daisy chain) VMEbus device has responded to the VMEbus Interrupt Acknowledge cycle. When IACKIN* is asserted to the CY7C960 during a VMEbus Interrupt Acknowledge, cycle the device determines if a VMEbus interrupt is pending of the same level being acknowledged. If so the CY7C960 generates a local interrupt acknowledge cycle to respond to the pending interrupt. If a local interrupt is not pending the device asserts IACKOUT*, passing the chain to the next interrupter on the VMEbus backplane.

IACKOUT* – VMEbus Interrupt Acknowledge Out

Input: No
Output: Yes
Drive: 8 mA
Active: Low

The CY7C960 asserts the IACKOUT* signal during VMEbus interrupt acknowledge cycles if there is no VMEbus interrupt pending on the device, or if the VMEbus interrupt level being acknowledged does not match that being requested by the CY7C960.

SYSRESET* – VMEbus System Reset Input

Input: Yes
Output: No
Active: Low

The SYSRESET* input to the CY7C960 halts all local and VMEbus operations and causes the device to reinitialize all internal register bits. This reinitialization is either performed

by reading the external serial PROM or by an Initialization Master on the VMEbus. When SYSRESET* goes Low, all outputs from the CY7C960 become three-state until the first rising edge on the CLK input.

WRITE* – VMEbus Write Input

Input: Yes
Output: No
Active: Low

The VMEbus WRITE* input encodes the type of VMEbus data cycle in progress. This signal is asserted when a VMEbus WRITE operation is in progress. During such a transaction, if the VMEbus address decodes properly, the CY7C960 responds by asserting the local R/W signal and performing the appropriate local cycle.

DTACK* – VMEbus Data Acknowledge Output

Input: No
Output: Yes
Drive: 64 mA
Active: Low

The DTACK* signal is asserted by the CY7C960 when a valid VMEbus transaction is in progress and the transaction has remained valid for the proper length of time. The assertion of this signal informs the VMEbus Master that the slave has either accepted the data during write operations or has sourced the data during read operations. This signal is a rescinding output.

3.3.2 Local Signals

LWORD* – Long Word

Input: Yes
Output: No
Active: Low

This is the local version of the VMEbus signal LWORD* which, when active, indicates either a D32 or D64 transfer over the VMEbus. The VMEbus LWORD* signal is connected directly to the A[0] bidirectional pin of the least significant CY7C964. The LA[0]

bidirectional pin of the least significant CY7C964 is in turn connected directly to the LWORD input of the CY7C960. This signal in conjunction with the DS0*, DS1*, and LA[1] signals encode the data transfer width or number of bytes, 1 through 4. This information is necessary to enable the appropriate CY7C964 data bytes.

LA[1] / PCLK – Local Address Signal / Init PROM Clock

Input: Yes
Output: Yes
Drive: 8 mA

During CY7C960 initialization this pin sources or receives a serial-PROM-compatible clock. The state of this pin is sampled immediately after the power-on reset period expires. If it is sampled High, then the CY7C960 will source a PROM clock signal (PCLK) during local initialization. If it is sampled Low then the CY7C960 will accept an external clock which will advance data through its internal serial chain.

If the CY7C960 receives a High data bit on PDATA during the first initialization clock cycle, this signal becomes LA[1] and the device expects to be configured from the VMEbus. If the device receives a Low data bit on PDATA during the first initialization clock cycle, the CY7C960 will either source or receive a clock from this pin and proceed to load configuration data from the local serial data source.

After initialization, this pin carries the local address signal LA[1].

LA[2] / PDATA / AM[0] – Local Address / Init PROM Data / Local AM code

Input: Yes
Output: Yes
Drive: 8 mA

During device initialization the CY7C960 receives the serial data stream on this signal: if the local serial method is used, then the serial configuration data comes from the PROM; if the VMEbus method of configuration is used, then the VMEbus A[2] signal is used to carry the serially-encoded configuration data, and the appropriate CY7C964 is enabled by the CY7C960 to provide this data to PDATA. After system initialization this signal becomes local bidirectional address signal LA[2] or LA[2]/AM[0] depending on the programming.

If the CY7C960 is programmed for LA/AM multiplexing then the VMEbus signals AM[5:0] will be driven on LA[7:2] by the CY7C960 between VMEbus accesses. A rising edge on

LADI is used by local external decoding circuitry to latch the AM codes before this bus changes from providing AM information to providing LA information. The CY7C960 will assert LAEN after LADI rises which disables the CY7C960 LA[7:1] drivers and at the same time enables the CY7C964 LA[7:0] drivers. See section 3.5.3.1.

LA[7:3] / AM[5:1] – Local Address Signals

Input: Yes
Output: Yes
Drive: 8 mA

LA[7:3] make up the remainder of the local bidirectional address bus. The CY7C960 only sources local addresses during VMEbus block transfer operations. During single cycle and interrupt acknowledge accesses the lowest order address byte is sourced from the respective CY7C964. The CY7C960 begins to source the least significant byte of local address information starting with the second cycle in a VMEbus block transfer. This is done to increment the local address by the proper amount, 1, 2, or 4, depending on the VMEbus word size of the transfer.

If the CY7C960 is programmed for LA/AM multiplexing, then the VMEbus signals AM[5:0] will be driven on LA[7:2] by the CY7C960 between VMEbus accesses. A rising edge on LADI is used by local external decoding circuitry to latch the AM codes before this bus changes from providing AM information to providing LA information. The CY7C960 will assert LAEN after LADI rises which disables the CY7C960 LA[7:1] drivers and at the same time enables the CY7C964 LA[7:0] drivers.

PREN* – Serial PROM Enable

Input: No
Output: Yes
Drive: 8 mA
Active: Low

The PREN* signal enables the serial initialization PROM. The CY7C960 asserts this signal when it receives an active SYSRESET* input from the VMEbus or after a power-on reset period. The PREN* signal remains active for the duration of the CY7C960 local initialization cycle.

LDEN* – Latch Data Enable

Input: No
Output: Yes

Drive: 8 mA
Active: Low

The LDEN* signal is used in conjunction with the PREN* signal to select one of several potential latched-data sources. During the initialization sequence, PREN* and LDEN* are both driven Low at the time that the Address Mask and Compare registers of the CY7C964s are to be loaded. When LDEN* is driven Low when PREN* is High, this signifies that an interrupt vector is to be enabled onto the local bus for the interrupt acknowledge cycle in progress.

RAS* / CS[4] – Row Address Strobe / Chip Select 4

Input: No
Output: Yes
Drive: 8 mA
Active: Programmable

The RAS*/CS[4] output on the CY7C960 is a dual-purpose pin whose function is selected during the initialization period. When configured to do so, this output controls the row address strobe function for DRAM. In the general-purpose I/O configuration, this output is a user-programmable chip select.

CAS* / CS[5] – Column Address Strobe / Chip Select 5

Input: No
Output: Yes
Drive: 8 mA
Active: Programmable

The CAS*/CS[5] output on the CY7C960 is a dual-purpose pin whose function is selected during the initialization period. When configured to do so, this output controls the column address strobe function for DRAM. In the general-purpose I/O configuration, this output is a user-programmable chip select.

ROW / CS[2] – Row Address Enable / Chip Select 2

Input: No
Output: Yes
Drive: 8 mA
Active: Programmable

The ROW/CS[2] is a dual-purpose signal whose function is selected during the initialization period. When configured to do so, this output acts as a row address enable signal, to be used

in conjunction with RAS. In the general-purpose I/O mode, this output becomes a user-programmable chip select.

When configured for DRAM operation, CY7C960 still provides CS[2] as an output from another pin: CS[2]/REGION[3].

COL / CS[3] – Column Address Enable / Chip Select 3

Input: No
Output: Yes
Drive: 8 mA
Active: Programmable

The COL/CS[3] is a dual-purpose signal whose function is selected during the initialization period. When configured to do so, this output acts as a column address enable signal, to be used in conjunction with CAS. In the general-purpose I/O mode, this output becomes a user-programmable chip select.

DBE[3:0] – Data Byte Enables [3:0]

Input: No
Output: Yes
Drive: 8 mA
Active: Programmable

These four signals provide the byte enables for local circuitry, either DRAM or I/O. The size of the VMEbus data transaction is decoded by CY7C960 from the state of the DS0*/DS1*/LWORD*/A1 VMEbus signals, and the appropriate byte enable signals are driven. The active state of the signal is user-programmable during configuration. DBE3 represents LD[7:0]. DBE0 represents LD[31:24].

CS[1:0] – Chip Select [1:0]

Input: No
Output: Yes
Drive: 8 mA
Active: Programmable

These two signals are chip select outputs that are available whether the CY7C960 is configured for DRAM or for I/O operations. The behavior of these pins is determined during configuration.

R/W* – Read/Write

Input: No
Output: Yes
Drive: 8 mA

R/W* is the local signal that determines if the cycle in progress is a read operation or a write operation. The CY7C960 asserts this signal Low during write operations.

LIRQ* – Local Interrupt Request

Input: Yes
Output: No
Active: Low

LIRQ* is the local interrupt request input. Asserting this active Low input causes the CY7C960 to assert the VMEbus IRQ* output signal.

LACK – Local Data Acknowledge/Local Bus Hold-off

Input: Yes
Output: No

The LACK input is used to acknowledge a local data transfer cycle. Asserting this active Low signal causes DTACK* to be driven on the VMEbus. The user may assert this signal continuously, which causes the CY7C960 to time data cycle acknowledgements: or the user may withhold assertion of LACK in order to handshake the acknowledge.

If the CY7C960 has been programmed for local bus hold-off mode, then LACK is also used to keep the CY7C960 off the local bus. If LACK is deasserted after LADI falls between VMEbus operations then the CY7C960 will three-state its local drivers and place itself in stand by until LACK is asserted again.

REGION[2:0] – Local Slave Decode Inputs

Input: Yes
Output: No

The REGION[2:0] inputs are user-programmable address decode inputs. External decoder circuitry, such as the CY7C964's, drives these signals when VMEbus addresses match user-defined values. CY7C960 uses these signals together with the REGION[3] and AM codes to determine its reaction to the VMEbus cycle. (See section 3.9.1, Region Mapping.)

CS[2] / REGION[3] – Chip Select [2] / Local Slave Decode Input

Input: Yes
Output: Yes
Drive: 8 mA
Active: Programmable

The CS[2]/REGION[3] signal pin has two user-configurable modes of operation. If CY7C960 is configured for I/O operation, the pin becomes the REGION[3] input, providing another decode input, a total of 4. If CY7C960 is configured for DRAM, then only three REGION inputs are required, and the pin becomes CS[2]. (See section 3.9.1, Region Mapping.)

CLK – Clock Input

Input: Yes
Output: No

The CY7C960 will operate with any input frequency less than 80 MHz. However, the VMEbus will suffer in performance if this clock is slower. All output events occur off the rising edge of the clock input. All internal states are timed by this signal.

3.3.3 Local Buffer Control Signals

LDS – Local Data Select

Input: No
Output: Yes
Drive: 8 mA

During multiplexed data VMEbus transactions this pin is used by the CY7C964s to select internal registers. During initialization, this signal determines which of the mask or compare registers is loaded within the CY7C964s.

LADI – Latch Address In

Input: No
Output: Yes
Drive: 8 mA

The Latch Address In signal controls the address latches within the CY7C964 that contain address information to be written to the local bus. The LADI signal is asserted shortly after

the CY7C960 detects an assertion of the VMEbus AS* signal and can be used externally to to latch local AM codes or LA[31:1] values. In system designs that use the CY7C960 with the CY7C964s this signal can directly connect to the LADI inputs on the CY7C964s.

LAEN – Local Address Enable

Input: No
Output: Yes
Drive: 8 mA
Active: Programmable

The Local Address Enable signal enables the local address output buffer within the CY7C964s. The state of this pin is sampled immediately after the power-on reset period expires. If it is sampled High then the LAEN signal will be active Low. If it is sampled Low then the LAEN signal will be active High.

In system designs that use the CY7C960 with four CY7C964s, this signal is connected to only the least significant device and is active High by default via a weak internal pull-down resistor. The LAEN inputs of the other three devices are tied High, or controlled by external logic allowing multi-port local bus accesses. This convention allows the CY7C960 to disable the address from the least significant CY7C964 so that it can source the least significant byte of local address during block transfer operations.

LEDI – Latch Enable Data In

Input: No
Output: Yes
Drive: 8 mA

LEDI is designed to control a transparent latch of the type used within the CY7C964. If this output is Low, data from the VMEbus flows through to the local data bus. Asserting this signal High closes the latch, maintaining the data present at the rising edge. System designs that use the CY7C960 with CY7C964s can tie this output directly to the associated LEDI input on all of the CY7C964s.

LEDO – Latch Enable Data Out

Input: No
Output: Yes
Drive: 8 mA

LEDO is designed to control a transparent latch similar to the type used within the CY7C964. If this output is Low, data from the local data bus flows through to the VMEbus.

Asserting this signal High closes the latch, maintaining the data present at the rising edge. System designs that use the CY7C960 with CY7C964s can tie this output directly to the associated LEDO input on all of the CY7C964s.

DENO* – Data Enable Out

Input: No
Output: Yes
Drive: 8 mA
Active: Low

The DENO* output controls the VMEbus data bus drivers in the CY7C964s. When data is to be driven onto the VMEbus, a Low level is driven from this output. A High level on this output signifies that the VMEbus drivers are high impedance. This pin should be connected to all the DENO* pins on the CY7C964s.

DENIN*, DENIN1* – Data Enable In Signals

Input: No
Output: Yes
Drive: 8 mA
Active: Low

The DENIN* and DENIN1* outputs control the latching of sections of the VMEbus data. These two control signals in association with the local SWDEN* signal allow all VMEbus transfer widths to be transmitted to the local peripherals. These signals are intended to be connected to the DENIN* and DENIN1* inputs on all the CY7C964s to enable the local bus drivers. See section 3.6.3, Swap Buffer Control.

ABEN* – Address Bus Enable

Input: No
Output: Yes
Drive: 8 mA
Active: Low

ABEN* is the VMEbus address bus enable out signal. The CY7C960 asserts this signal Low during VMEbus D64 block transfer read operations, to enable the second longword of data information onto the VMEbus. This output should be connected to the corresponding ABEN* inputs on all four CY7C964s. A pull-up resistor is also needed on this pin for proper operation.

STROBE – CY7C964 Strobe Control

Input: No
Output: Yes
Drive: 8 mA

The STROBE output allows the CY7C960 to control the register loading on the CY7C964s. Loading the CY7C964 Address Mask and Compare registers requires assertion of the STROBE signal, with the LDS signal providing the signal that determines which of the two registers, mask or compare, is loaded. The STROBE output performs this function during system initialization. Designs that use four companion CY7C964s should tie this output to the associated STROBE input on all four CY7C964 devices.

D64 – CY7C964 D64 Control

Input: No
Output: Yes
Drive: 8 mA

The D64 output informs external hardware that a D64 VMEbus block transfer operation is in progress. When a D64 VMEbus address decode cycle is valid this signal asserts High. Designs that use four companion CY7C964s should tie this output to the associated D64 input on all four CY7C964 devices.

SWDEN* – Swap Data Enable

Input: No
Output: Yes
Drive: 8 mA
Active: Low

The SWDEN* signal controls a local swap buffer. This buffer is used to move data to the proper section of the local data bus during appropriate byte and word width transfers. The CY7C960 local bus ordering convention matches that of the MC68020. This signal asserts Low when a byte or word width transfer, which always are moved on D[15:0] of the VMEbus, must end up on D[31:16] of the local data bus. (See section 3.6.3, Swap Buffer Control.)