3.6
CY7C964 Interface

3.6.1 CY7C964 Overview

The CY7C960 is designed for use with the CY7C964 VMEbus Interface Logic Circuit. This device is fully described in Section 4, The CY7C964 Bus Interface Logic Circuit. The CY7C960 provides all the control and timing for the interface with the CY7C964. Interface timing as generated by the CY7C960 is designed for CY7C964 delay characteristics.

The CY7C964 contains a collection of counters, latches, and multiplexers used to facilitate data handling during any of the many VMEbus data transactions. Three-state high drive buffers allow direct connection to VME and local address and data busses. Additionally, the CY7C964 contains an address comparator with mask function to allow the CY7C964 to form part of the user's slave address decoder. Defined as a companion to the VIC068A/ VIC64 devices, the CY7C964 has been designed into many high-performance VME64 CPU boards. In concert with the CY7C960, it performs the functions of address decoder, D64 data multiplexer, and local address counter, to facilitate the design of high-performance slave systems.

3.6.2 CY7C964 Connections

The signals that are provided by the CY7C960 for use by the CY7C964 are: LADI, LEDI, LEDO, DENO*, ABEN*, DENIN*, DENIN1*, LAEN, STROBE, LDS, and D64 using dedicated pins. These signals are described in the pin description section.

LADI (Latch ADdress In) controls a transparent latch which connects the VMEbus address to the local address. The default state of the signal ensures that the VMEbus address is driven to the local pins, allowing the implementation of VMEbus address decoder circuitry on the local address bus. The LAEN (Local Address ENable) input is tied High on all but the

least significant CY7C964 to ensure that the local address is always enabled. The least significant CY7C964 has its LAEN pin controlled by the CY7C960 to allow the CY7C960 to source the LSB of address during block transfers when the address has to increment by 1, 2, or 4 (dependant on the transfer type: single, double, or quad byte). Note that in order to take advantage of the "local bus holdoff" feature of the CY7C960, it is necessary to control LAEN of the upper 3 CY7C964 devices. LAEN must be driven Low during holdoff.

LEDI (Latch Enable Data In) and LEDO (Latch Enable Data Out) control the VMEbus and local data transfer latches in the CY7C964. Data read from local resources must be set up to LEDO for burst transfers, while LEDI provides data hold time during burst transfers when data is captured from the CY7C964. These signals, by holding data in the interface allow "write posting" and "read-ahead" performance features.

DENO* (VMEbus Data ENable Out) and the pair of signals, DENIN* and DENIN1* (local Data ENable IN) are normally used for local and VMEbus data enable. DENIN* and DENIN1* are also active during address broadcast of A64 and A40 VMEbus transactions. They are used to inform an external address decoder when the data bus can be sampled for the high-order address information.

During D64 and MD32 data cycles, the function of DENO* and DENIN*/DENIN1* are identical to LEDO and LEDI respectively. A two-stage pipelined latch inside the CY7C964 is controlled in the data sourcing case by LEDO and DENO* working in concert, and in the data capture case by LEDI and DENIN*/DENIN1* working in concert.

Each VMEbus data cycle is served by two local data cycles. The second cycle for slave read must set data up to the falling edge of DENO*. For slave write, data hold on the second cycle is provided by the assertion of DENIN* (D64) or DENIN1* (MD32).

LDS is used during D64/MD32 slave write transfers to control the VMEbus address to local data demultiplexing, and during the initialization period to control the selection of the address mask and compare registers. During multiplexed slave data capture, LDS is the signal which controls data hold time with respect to the deassertion of CAS* and/or DBE.

ABEN* (VME Address Bus ENable) is active only during multiplexed data transactions to enable the VMEbus address pins during D64 or MD32 transfers.

D64 is the signal that informs the CY7C964s that the data phase of multiplexed data transfer is in progress and the on-chip pipelining should be used to multiplex or demultiplex the local

data. The CY7C964 is expressly designed to demultiplex D64 and MD32 VME transactions to a non-multiplexed 32 bit local data bus.

STROBE is a timing signal used to load the on-chip address mask and compare registers of the CY7C964. It can be considered a latch enable signal which latches local data when High.

The on-chip counters of the CY7C964 are used for local address counting during slave D64 block transfers if the VMEbus master bursts to 2 Kbyte boundaries. Therefore the counter chains must be enabled by connecting the appropriate carry-out to carry-in pins. The VMEbus counters of the CY7C964 are not used by the CY7C960.

It is recommended that the following connections be made to ensure correct operation during the Reset period: Pull-up resistors attached to ABEN*, DENO*; pull-down resistor attached to LAEN. These connections prevent CY7C964 drivers from turning on during the brief periods of three-state operation during reset.

The CY7C964 has several signals which are not used for slave operations: BLT*, FC1, LADO, and MWB*. LADO and FC1 must be tied Low. BLT* and MWB* must be tied High for correct operation.

Figure 3–23 shows how the control signals for the CY7C964 are driven during initialization to load the Address Compare and Mask Registers. The significant signals are LDS, which selects which register to load, and STROBE, which actually strobes the data on the local bus into the appropriate register.

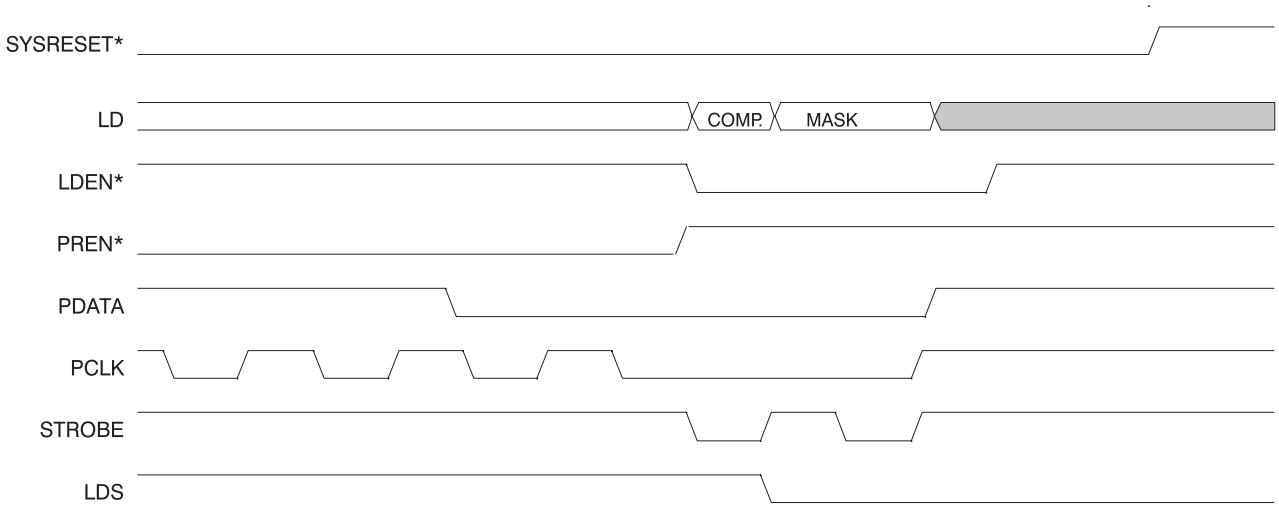

Figure 3–23. Example of CY7C964 Control Timing

3.6.3 Swap Buffer Control

The CY7C960 is designed to control the swap buffering necessary for handling D8 and D16 VMEbus transactions in combination with 32-bit local memory. *Figure 3−24* illustrates how VMEbus byte lanes relate to local memory. Note that the CY7C960 coordinates control of SWDEN* with DENIN*/DENIN1*. The CY7C964 Byte(0) and Byte(1) drivers are turned off during slave write transfers when SWDEN* is active. Because DENIN*/DENIN1* are used as latch control signals during multiplexed data transactions (D64 and MD32) DENIN* signaling to CY7C964 Byte(0) and Byte(1) must be modified by external logic IF (and only IF) and board is to handle BOTH D64 and A40/MD32 slave write transactions. The required circuitry is shown at the top of the figure below.

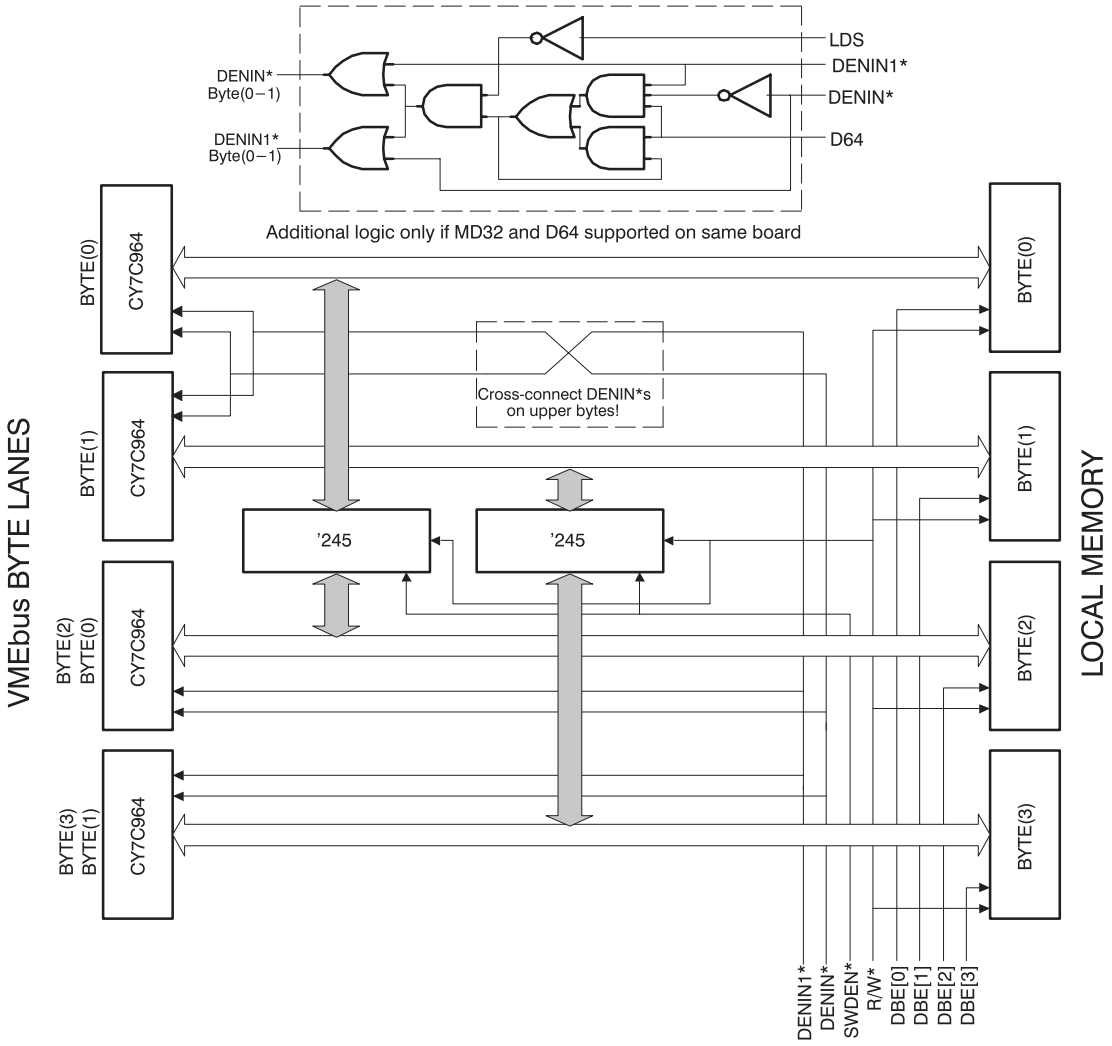

Figure 3−24. Swap Buffer Design