4.1

Introduction

The CY7C964 is a flexible collection of byte (8-bit) wide transceivers, latches, counters, multiplexers, and comparators that provide bus interface designs with a low-cost alternative to PLDs, ASICs, or discrete logic devices. It is based on a standard cell design that incorporates patented line drivers for reduced ground bounce and high noise immunity. The CY7C964 is a companion part to Cypress's VIC068A, VIC64, CY7C960, and CY7C961 VMEbus interface controller devices. It is completely compatible with all operating modes of these devices, such as dual-address path, block transfer boundary crossing conditions, block transfer initialization cycle, local DMA control, and D64 VMEbus block transfers. Signal-naming conventions correspond directly to the VIC068A/VIC64/CY7C960/961 buffer control signals, and the CY7C964 can be directly connected to these corresponding signals.

The CY7C964 can also be used as a generic-interface building block. Some examples include low-cost slave VMEbus controllers, VSB interfaces, or other interface applications. CY7C964s are cascadable, allowing easy interfacing to buses of any width. By combining multiple logic functions into one discrete part, the CY7C964 saves board space and reduces power consumption, which is becoming increasingly important to designers.