



4.4

Signal Descriptions

4.4.1 VMEbus Signals

A[7:0]

Input:	Yes
Output:	Yes, three-state
Drive:	48 mA

These are VMEbus-compatible address signal transceivers that can be directly connected to the VMEbus. A0 is the least-significant address bit. In flow-through modes of operation, these signals correspond one for one with local interface signals LA[7:0].

In VMEbus interface applications, including those using the VIC068A, VIC64, CY7C960, or CY7C961, these signals should be connected to the VMEbus address bus sequentially.

In CY7C960/961 designs, A0 on the least-significant CY7C964 should be connected to the VMEbus LWORD* signal.

D[7:0]

Input:	Yes
Output:	Yes, three-state
Drive:	48 mA

These are VMEbus-compatible data signal transceivers that can be directly connected to the VMEbus. D0 is the least-significant data bit. In flow-through modes of operation, these signals correspond one for one with local interface signals LD[7:0].

In VMEbus interface applications, including those using the VIC068A, VIC64, CY7C960, or CY7C961, these signals should be connected to the VMEbus data bus sequentially.

4.4.2 Local Signals

LA[7:0]

Input:	Yes
Output:	Yes, three-state
Drive:	8 mA

These are medium drive-strength local address transceivers that allow direct connection to memory, microprocessors and/or peripheral controllers. LA0 is the least-significant local address signal. In flow-through operating modes, these signals correspond one for one with the VMEbus signals A[7:0].

When implementing conventional VMEbus interfaces or using the CY7C964 with the VIC068A, VIC64, CY7C960, or CY7C961, these signals should be connected to the local address bus sequentially.

LD[7:0]

Input:	Yes
Output:	Yes, three-state
Drive:	8 mA

These are medium drive-strength local data transceivers that allow direct connection to memory, microprocessors and/or peripheral controllers. LD0 is the least-significant local data signal. In flow-through operating modes, these signals correspond one for one with the VMEbus signals D[7:0].

When implementing conventional VMEbus interfaces or using the CY7C964 with the VIC068A, VIC64, CY7C960, or CY7C961, these signals should be connected to the local data bus sequentially.

ABEN*

Input:	Yes
Output:	No

This is the VMEbus Address Bus ENable control signal. This signal controls the state of the VMEbus address transceivers A[7:0]. When asserted (driven Low), the transceivers are configured as outputs and are enabled.

When using the CY7C964 with the VIC068A, VIC64, CY7C960, or CY7C961 to implement VMEbus interfaces, this input should be connected to the ABEN* output of the controller.

BLT*

Input: Yes
Output: No

This signal controls the VIC-compatible block transfer operations that require local Direct Memory Access (DMA). If this input is driven Low, the CY7C964 will operate in the appropriate VIC-compatible block transfer mode (dependent on the states of the other buffer control logic).

When using the CY7C964 with the VIC068A, VIC64, or CY7C961, this signal can be directly connected to the controller BLT* pin. A rising edge of BLT* increments the local address counters if LCIN* is Low. Refer to the LCIN* signal description and Chapter 4.5, CY7C964 Operation, for the further information on the local address counter function.

D64

Input: Yes
Output: No

This signal is used to indicate to the CY7C964 that a VMEbus D64 block transfer is in progress. When High, the CY7C964 is instructed to use the high-performance two-state pipeline and multiplex or demultiplex 64-bit data to and from the VMEbus address bus.

When used in conjunction with the VIC64, CY7C960, or CY7C961, this pin can be directly connected to the SCON*/D64 signal. For applications that only support 32-bit block transfers, as is the case with the VIC068A, this input should be tied Low.

DENIN*

Input: Yes
Output: No

The Data ENable IN signal is used to control the three-state data transceivers LD[7:0]. If a logic Low level is presented to this input, LD[7:0] transceivers will be enable. In conventional VMEbus designs, this signal would need to be driven during master read or slave write operations.

When used in conjunction with the VIC068A, VIC64, CY7C960, or CY7C961, this input is typically connected to DENIN1* for CY7C964's controlling bus data lines D16 through D31, and DENIN* for the CY7C964's controlling bus data lines D8 through D15.

DENIN1*

Input: Yes
Output: No

The Data ENable IN 1 signal is used in conjunction with DENIN* to latch data from the VMEbus and provide a second enable control of the LD[7:0] transceivers for D64 transactions.

When used in conjunction with VIC64, CY7C960, or CY7C961, this input is typically connected to DENIN* for CY7C964's controlling bus data signals D16 through D31, and DENIN1* for the CY7C964's controlling bus data signals D8 through D15.

DENO*

Input: Yes
Output: No

The Data ENable Out signal is used to control the three-state transceivers D[7:0]. If a logic-Low level is presented to this input, the D[7:0] transceivers will be enabled. In conventional VMEbus design, the D[7:0] signals will be directly connected to the VMEbus. Used in this manner, this input must be asserted during master writes and slave read operations.

When used in conjunction with the VIC068A, VIC64, CY7C960, or CY7C961, this signal should be connected to the DENO* output on the controller.

FC1

Input: Yes
Output: No

The Function Code 1 input is used by the CY7C964 during block transfer operations to determine the source for the local address signals LA[7:0]. If the input is driven High, the internal Local DMA counter is selected as the source for LA[7:0]. If this input is Low, the Slave Block Transfer counter is the source for LA[7:0].

When used with the VIC068A, VIC64, or CY7C961, this signal can be directly connected to the FC1 pin of the controller. The controller will drive this pin to the proper level for slave or block transfer operations when it is master of the local system bus.

When used with the CY7C960, this signal should be tied to GND.

LCOUT*

Input:	No
Output:	Yes
Drive:	8 mA

The Local Carry Out signal is used by the CY7C964 for cascading the local address counter chains. This signal will drive Low when the local address counter has reached the maximum count (255). The signal generates a synchronous count enable for the next-most-significant CY7C964 in the cascade chain. This signal alone does not cause the local address counter to increment.

When cascading the CY7C964s, this signal should be connected to the LCIN* pin of the next most significant device. Refer to the description of the LCIN* pin for further information on the operation of the local address counters.

LDS

Input:	Yes
Output:	No

The Local Data Select input has two main functions: (1) as a control input for the data to address bus multiplexer during D64 VMEbus block transfers, (2) as a select bit for configuring the CY7C964 address comparison and mask registers. Refer to Chapter 4.5, CY7C964 Operation, for further information about how data is steered to and from the VMEbus address bus during block transfers. Typically this input will be connected to LA2 for VIC controllers and to the LDS output of CY7C960/961.

When configuring the CY7C964 internal address mask and address compare registers, this pin in conjunction with MWB* selects which registers to load. During a comparator register load cycle, LDS High will select the Address Compare register; otherwise the Address Mask register will be selected.

LADI

Input:	Yes
Output:	No

The Latch Address In signal controls a transparent VMEbus to local address latch within the CY7C964. When this input is High, the device will latch the data present on A[7:0]. This function is useful when building VMEbus interfaces for latching the VMEbus address during a slave access. If LADI is Low, the internal address latch will be in a flow-through mode.

LADI is also used to increment the slave block transfer local address counter. LADI is used in conjunction with LAEN to control the operation of the VMEbus to local address section of the CY7C964. For more information, refer to the description of LAEN.

When using the CY7C964 to implement VMEbus interfaces, this signal is used to maintain the local address during slave read and write cycles. For VMEbus designs that use a Cypress controller, this input should be connected to the LADI output of the controller.

LAEN

Input: Yes
Output: No

The Local Address ENable signal controls the three-state enable for signals LA[7:0]. When this signal is High, LA[7:0] drive the address local bus. Driving the signal Low places LA[7:0] in the high-impedance/input state.

When using the CY7C964 to implement VMEbus interfaces, this signal is driven High to maintain the local address VMEbus during slave cycles. For VMEbus interfaces using the VIC068A or VIC64, this pin should be connected to the LAEN output on the VIC. For CY7C960/961 designs, only the least-significant CY7C964 is connected to the LAEN output of the controller.

LEDI

Input: Yes
Output: No

The Latch Enable Data In signal controls a transparent VMEbus-to-local-data-bus latch within the CY7C964. When this input is High, the device will latch the data present on D[7:0]. This function is useful when building VMEbus interfaces for latching the VMEbus data during a master or slave access. If LEDI is Low, the internal address latch will be in a flow-through mode.

LEDI is used in conjunction with DENIN* and DENIN1* to control the operation of the address VMEbus-to-local-data section of the CY7C964.

When implementing VMEbus interfaces with the CY7C964, LEDI can be used to maintain the local data during VMEbus master read and slave write cycles. For VMEbus designs that use a Cypress controller, this input should be connected to the LEDI output of the controller.

LEDO

Input: Yes
Output: No

The Latch Enable Data Out signal controls a transparent local-data-to-VMEbus-data latch within the CY7C964. When this input is High, the device will latch the data present on LD[7:0]. This function is useful when building VMEbus interfaces for latching the VMEbus data during a master or slave access. If LEDO is Low, the internal address latch will be in a flow-through mode.

LEDO is used in conjunction with DENO* to control the operation of the local-to-VMEbus-data section of the CY7C964.

When implementing VMEbus interfaces with the CY7C964, LEDO can be used to maintain the VMEbus data during VMEbus master write and slave read cycles. For VMEbus designs that use a Cypress controller, this input should be connected to the LEDO output of the controller.

LADO

Input: Yes
Output: No

The Latch Address Out signal controls a transparent local-to-VMEbus address latch within the CY7C964. When this input is High, the device will latch the data present on LA[7:0]. This function is useful when building VMEbus interfaces for latching the local address during a master transfer. If LADO is Low, the internal address latch will be in a flow-through mode.

LADO is used in conjunction with ABEN* to control the operation of the local-to-VMEbus address section of the CY7C964.

When using the CY7C964 to implement a VMEbus interface, this signal can be used to maintain the local address during VMEbus slave read and write cycles. For VMEbus designs that use a VIC068A, VIC64, or CY7C961, this input should be connected to the LADO output of the controller.

LCIN*

Input: Yes
Output: No

Local Carry IN is a synchronous count enable for both the local master block transfer and slave block transfer local address counters. LCIN* is multiplexed within the CY7C964 and can be routed to either local block transfer address counter. When connected to the master block transfer local address counter, if LCIN* is driven Low, a falling edge on the BLT* signal will increment the address count. When this input is connected to the slave block transfer counter and driven Low, a rising edge of LADI will increment the address count.

When cascading CY7C964s, this signal should be connected to the LCOUT* signal of the next-least-significant device.

MWB*

Input: Yes
Output: No

The Module Wants Bus is a decoding/control signal for the CY7C964 that allows the device to discern the cycle type. When MWB* is active (Low), the CY7C964 assumes that a block transfer initiation cycle or a single-cycle VMEbus transfer is pending. Subsequent assertion of BLT* allows the CY7C964 to enter block transfer mode.

MWB* is also used to decode accesses to the CY7C964 address Mask and Compare registers. To load these registers, MWB* must be inactive (High).

STROBE

Input: Yes
Output: No

The STROBE signal controls the loading of the internal Address Mask and Compare registers. This signal operates in the same manner as an active-Low chip select for these registers. When STROBE is Low and MWB* is High, data present on LD[7:0] will be loaded into either the Address Mask or Compare registers.

Refer to Chapter 4.5, CY7C964 Operation, for further information on the use of MWB* to load the Address Mask and Compare registers.

VCOMP*

Input: No
Output: Yes
Drive: 8 mA

The VMEbus COMPare signal indicates whether the address presented on A[7:0] matches the pattern of the internal Address Compare register. If the two values are determined to match, VCOMP* will drive Low. (Note: The Address Mask register can mask bits of the Compare register, causing these bits to match anything.)

This signal is the output of an asynchronous comparator and is therefore susceptible to glitching during address transitions on A[7:0]. When used in conjunction with the VIC64 or VIC068A for conventional VMEbus implementations, these signals should be de-glitched externally. The decode delay feature of the CY7C960/961 eliminates the need to de-glitch for slave controller designs. External logic is required to cascade VCOMP* comparison outputs.

VCIN*

Input: Yes
Output: No

VMEbus Carry IN is a synchronous count enable for the local address counters. When VCIN* is Low and the device is not operating in the Dual-Address-Path mode, a rising edge on the LADO signal will increment the VMEbus address counter.

When cascading CY7C964s, this signal should be connected to the VCOUT* signal of the next-least-significant device.

For more information on the Dual-Address-Path mode, refer to Chapter 4.5, CY7C964 Operation.

VCOUT*

Input: No
Output: Yes
Drive: 8 mA

The VMEbus Carry Out signal is used by the CY7C964 for cascading the VMEbus address counter chains. This signal will drive Low when the VMEbus address counter has reached the maximum count (255). The signal generates a synchronous count enable for the next-most-significant CY7C964 in the cascade chain. This signal alone does not cause the VMEbus address counter to increment.

When cascading the CY7C964s, this signal should be connected to the VCIN* pin of the next-most-significant device. Refer to the description of the VCIN* pin for further information on the operation of the VMEbus address counters.