4.5
CY7C964 Operation

4.5.1 Overview

The CY7C964 is a general-purpose bus interface device that provides seamless support for the entire family of VMEbus interface controllers. The part is also suitable for many other general-purpose bus interface applications. *Figure 4−3* is the block diagram of the device, showing the array of latches, multiplexers, and counters.

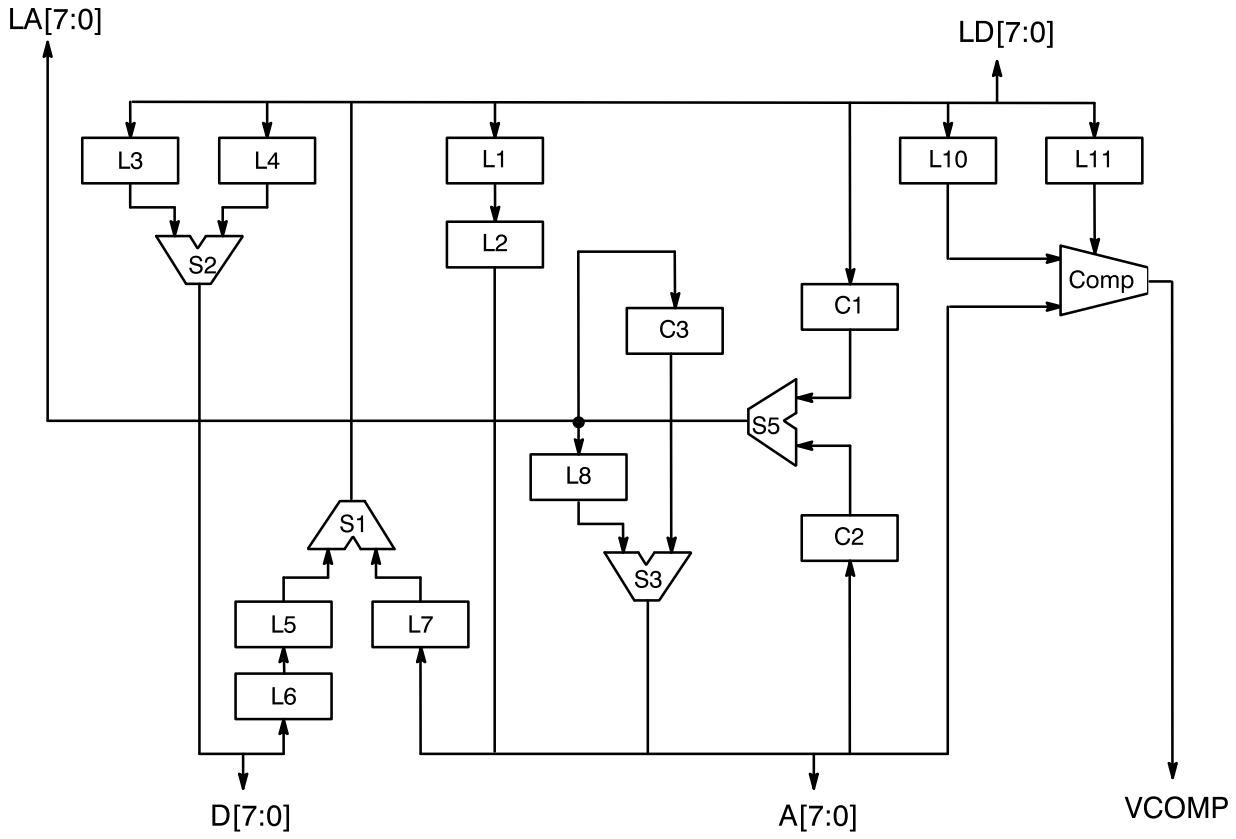

Figure 4−3. CY7C964 Block Diagram

This section of the document dissects the high-level block diagram into lower-level functional blocks. General operational and timing information is presented on a block-by-block basis. This information is provided for designers who wish to implement generically-controlled interfaces. The tables show the control signal logic sequence needed to operate or communicate with each of the functions. Timing parameters are included, which reference the switching characteristics listed later in this document.

The CY7C964 operation is controlled by the combination of external control signals and internal state logic. Three internal asynchronous state bit control the operating mode of the device. These bits are referred to as BLT_STATE, BLT_INIT, and DUAL_PATH. The BLT_STATE bit is set during block transfer operations. The block transfer initiation cycle generates a rising edge on the BLT_INIT signal. The DUAL_PATH signal is the output of a transparent latch within the device that latches the state of LADO. These internal state bits must be in the proper state to use and communicate with the internal logic of the device. The functional tables include references to these signals when their state is required for the operation. The designer must perform the appropriate cycle to the device to set or clear these latches as needed prior to the desired functional cycle. The internal latch signals and all other control signals that are not called out within the tables for a specific operation can be considered don't cares.

Table 4−5. Examples of References to Control Signals Within Functional Tables

Note 1: BLT_STATE=(/BLT* • /MWB*)+(BLT_STATE • (/BLT*+/MWB*+LAEN))
Note 2: BLT_INIT=(/BLT_STATE • /BLT* • /MWB*)+(BLT_INIT • /BLT* • /MWB*)
Note 3: DUAL_PATH=(LADO • BLT_INIT)+(DUAL_PATH • /BLT_INIT)

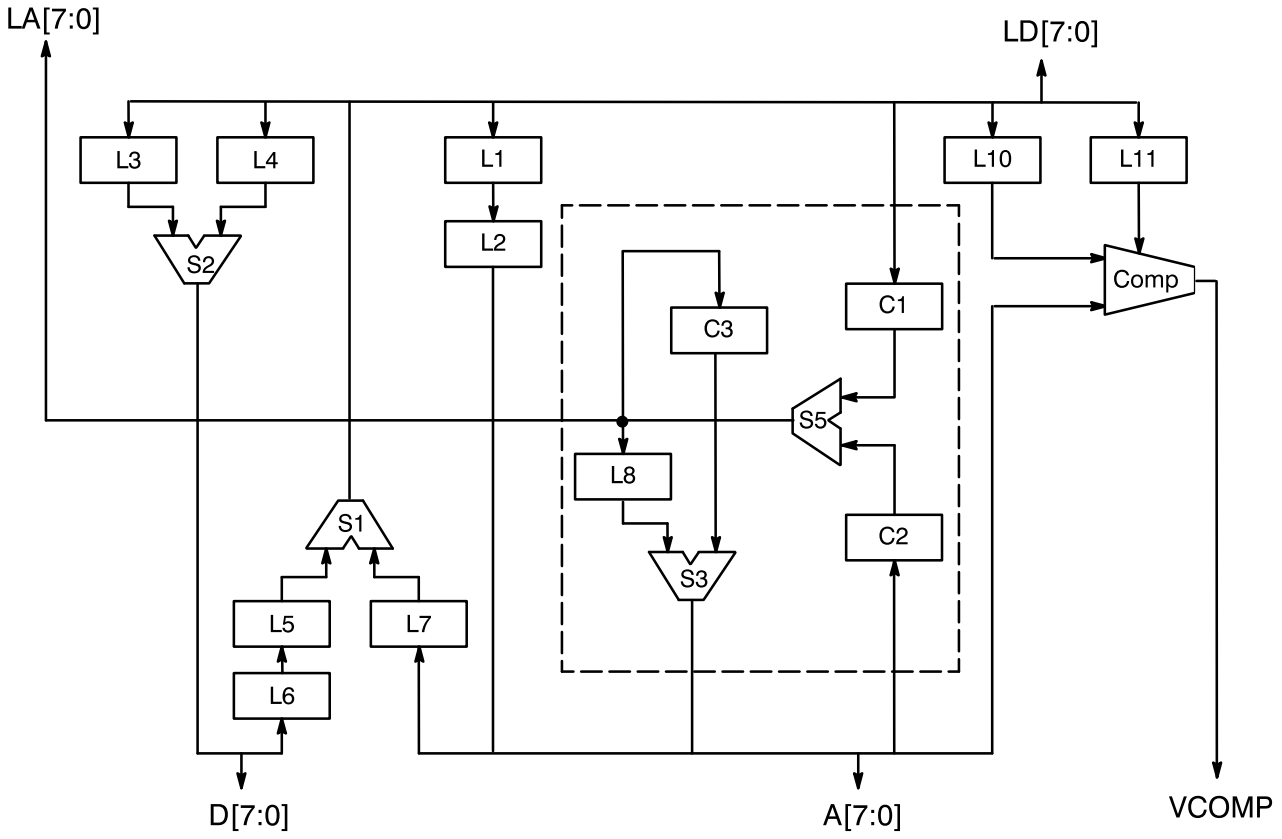

Figure 4−4. CY7C964 Block Diagram: Address Counters and Address Multiplexers

4.5.2 Master Block Transfer Local Address Counter (C1)

Master Block Transfer Local Address Counter supplies the local address to LA[7:0] during master block transfer operations. This 8-bit synchronous counter is cascadable using the LCIN*/LCOUT* daisy-chain. The counter powers up in an uninitialized state and must be initialized for predictable operation. The counter loads from LD[7:0] when both MWB* and BLT* control signals are active (Low). To enable the counter onto LA[7:0], an internal asynchronous latch (BLT_STATE) must be set and Local Address Multiplexer S5 must select counter C1. A falling edge on MWB* or BLT* increments C1. FC1 controls S5. If it is High, as shown in *Table 4−7*, C1 is selected. The internal latch and S5 multiplexer must also be in the proper state to increment the counter. For further information on the S5 Local Address Multiplexer, see section 4.5.3.

Table 4−6. Master Block Transfer Local Address Counter Operation

Logic	Functional Description	Operational Description	Required Condition	Parameter
C1	Load counter	LD[7:0] valid to falling edge of MWB*	BLT*=0, LAEN=0	Set-up t48
				Hold t49
		LD[7:0] valid to falling edge of BLT*	MWB*=0, LAEN=0	Set-up t50
				Hold t51
	Increment counter	MWB* falling edge to LA[7:0] valid	LAEN=1, FC1=1, BLT_STATE=1[1]	Prop t54
		BLT* falling edge to LA[7:0] valid	LAEN=1, FC1=1, BLT_STATE=1[1]	Prop t54
		LCIN* valid to MWB* falling edge	LAEN=1, FC1=1, BLT_STATE=1[1]	Set-up t52
				Hold t53
		LCIN* valid to BLT* falling edge	LAEN=1, FC1=1, BLT_STATE=1[1]	Set-up t52
				Hold t53
	Counter carry out at terminal count	MWB falling edge to LCOUT* valid	LAEN=1, FC1=1, BLT_STATE=1[1]	Prop t55
		BLT* falling edge to LCOUT* valid	LAEN=1, FC1=1, BLT_STATE=1[1]	Prop t55
		LCIN* valid to LCOUT* valid	LAEN=1, FC1=1, BLT_STATE=1[1]	Prop t56
	Minimum pulse widths	BLT*	LAEN=1, FC1=1, BLT_STATE=1[1]	t57
		MWB*		t57

4.5.3 Local Address Multiplexer (S5)

The Local Address Multiplexer S5 routes the outputs of counters C1 or C2 to signals LA[7:0]. The local address counter carry chain LCIN*/LCOUT* is also controlled by this multiplexer. If FC1 is High, counter C1 drives LA[7:0] and LCIN*/LCOUT* are visible/driven by C1, respectively. When FC1 is Low, C2 drives LA[7:0] and is attached to the LCIN*/LCOUT* daisy-chain.

Table 4−7. Local Address Multiplexer Operation

Logic	Functional Description	Operational Description	Required Condition	Parameter
S5	Select C1 counter	FC1 rising edge to LA[7:0] valid		Prop t85
	Select C2 counter	FC1 falling edge to LA[7:0] valid		Prop t86
	Select C1 carry chain	FC1 rising edge to LCOUT* valid		Prop t88
	Select C2 carry chain	FC1 falling edge to LCOUT* valid		Prop t87

4.5.4 Slave Block Transfer Local Address Counter/Latch (C2)

The Slave Block Transfer Local address counter provides two functions: a counter for slave block transfer operations and a transparent address latch for VMEbus slave operations. When the latch control signal LADI is held Low the counter is in a transparent mode: Logic levels present will flow through the device to the inputs of the local address multiplexer S5. FC1 controls the S5 multiplexer and must be Low to select counter C2 as the source for LA[7:0]. Driving either LADI or D64 High exclusively latches the data present on A[7:0]. The counter increments if LCIN* is Low, D64 is High, and a rising edge occurs on LADI. The contents of the counter/latch are enabled onto the local data bus when LADI and FC1 are Low and D64 is High. Counter C2 is not initialized at power-up; for predictable operation the counter should be loaded prior to use.

Table 4−8. Slave Block Transfer Local Address Counter/Latch Operation

Logic	Functional Description	Operational Description	Required Condition	Parameter
C1	Load counter	A[7:0] valid to D64 rising edge	LADI=0	Set-up t58
				Hold t59
		A[7:0] valid to LADI rising edge	D64=0	Set-up t60
				Hold t61
	Increment counter	LADI rising edge to LA[7:0]	D64=1, FC1=0	Prop t64
		LCIN* active to LADI rising edge	D64=1	Set-up t62
				Hold t63
	Counter carry out at terminal count	LADI rising edge to LCOUT*	D64=1, FC1=0	Prop t65
	Minimum pulse width	LADI		t66

4.5.5 Master Block Transfer VMEbus Address Counter (C3)

The VMEbus Master Block Transfer Address stores and increments the VMEbus address during master block transfer operations. The counter loads from LA[7:0] on the rising edge of MWB* provided that the internal asynchronous latch BLT_STATE is set. The contents of the counter are enabled onto the A[7:0] pins if the internal asynchronous latch bits BLT_STATE and multiplexer S3 are in the appropriate state. Depending on the state of DUAL_PATH, either the rising or the falling edge of LADO increments C3. Counter C3 uses the VCIN*/VCOUT* counter daisy-chain. This counter is uninitialized at power-up and should be initialized prior to use for predictable operation.

Table 4−9. Master Block Transfer VMEbus Address Counter Operation

Logic	Functional Description	Operational Description	Required Condition	Parameter
C3	Load counter	LA[7:0] valid to rising edge of MWB*	BLT_STATE=1[1] BLT_INIT=1	Set-up t67
				Hold t68
	Increment counter	LADO falling edge to A[7:0]	BLT_STATE=1[1] DUAL_PATH=1[3] BLT_INIT=0	Prop t69
		LADO rising edge to A[7:0]	BLT_STATE=1[1] DUAL_PATH=0 BLT_INIT=0	Prop t70
		VCIN* valid to LADO rising/ falling edge		Set-up t134
				Hold t135
	Counter carry out	LADO falling edge to VCOUT* valid	BLT_STATE=1[1] DUAL_PATH=1[3] BLT_INIT=0	Prop t71
		LADO rising edge to VCOUT* valid	BLT_STATE=1[1] DUAL_PATH=0 BLT_INIT=0	Prop t72
	Minimum pulse width	LADO (High)		t73
		LADO (Low)		t73

4.5.6 VMEbus Address Latch (L8) and Multiplexer (S3)

The VMEbus Address Latch and Multiplexer selects the source for the VMEbus address signals A[7:0]. The information supplied to A[7:0] originates at one of three sources: the D64 block transfer data pipeline latch L2, the VMEbus master block transfer counter C3, or the VMEbus address latch L8. *Table 4−10* shows how to latch information into the VMEbus address latch L8 and control the selection of the source for signals A[7:0]. Latch L8 is uninitialized at power-up and for predictable operation should be loaded prior to use.

Table 4−10. VMEbus Address Latch and Multiplexer Operation

Logic	Functional Description	Operational Description	Required Condition	Parameter
S3	Select L8	D64 falling edge to A[7:0] valid	BLT_STATE=1[1]	Prop t83
		ABEN* falling edge to A[7:0] valid	BLT_STATE=1[1]	Prop t84
		D64 falling edge to A[7:0] valid	BLT_STATE=0	Prop t81
L8	Load L8	LA[7:0] valid to LADO rising edge		Set-up t40
				Hold t41

4.5.7 VMEbus Address Comparator

The VMEbus Address Comparator is made up of three logic elements: an address mask register, address compare register, and a high-performance, 8-bit, equality comparator. The compare and mask registers control the compare logic. The mask register contains an 8-bit value that enables or disables bits of the comparator. The compare register contains an 8-bit pattern. The enabled bits of the compare register are matched against the value on A[7:0]. If a match is detected (all active bits equal), the VCOMP* output pin is driven Low. Neither the compare register nor the mask register are preset at power-up and must be initialized for predictable operation. The act of writing the compare register clears the mask register. This prevents any inadvertent address compares during the configuration process. See Chapter 4.3 for further information on the VMEbus address comparator.

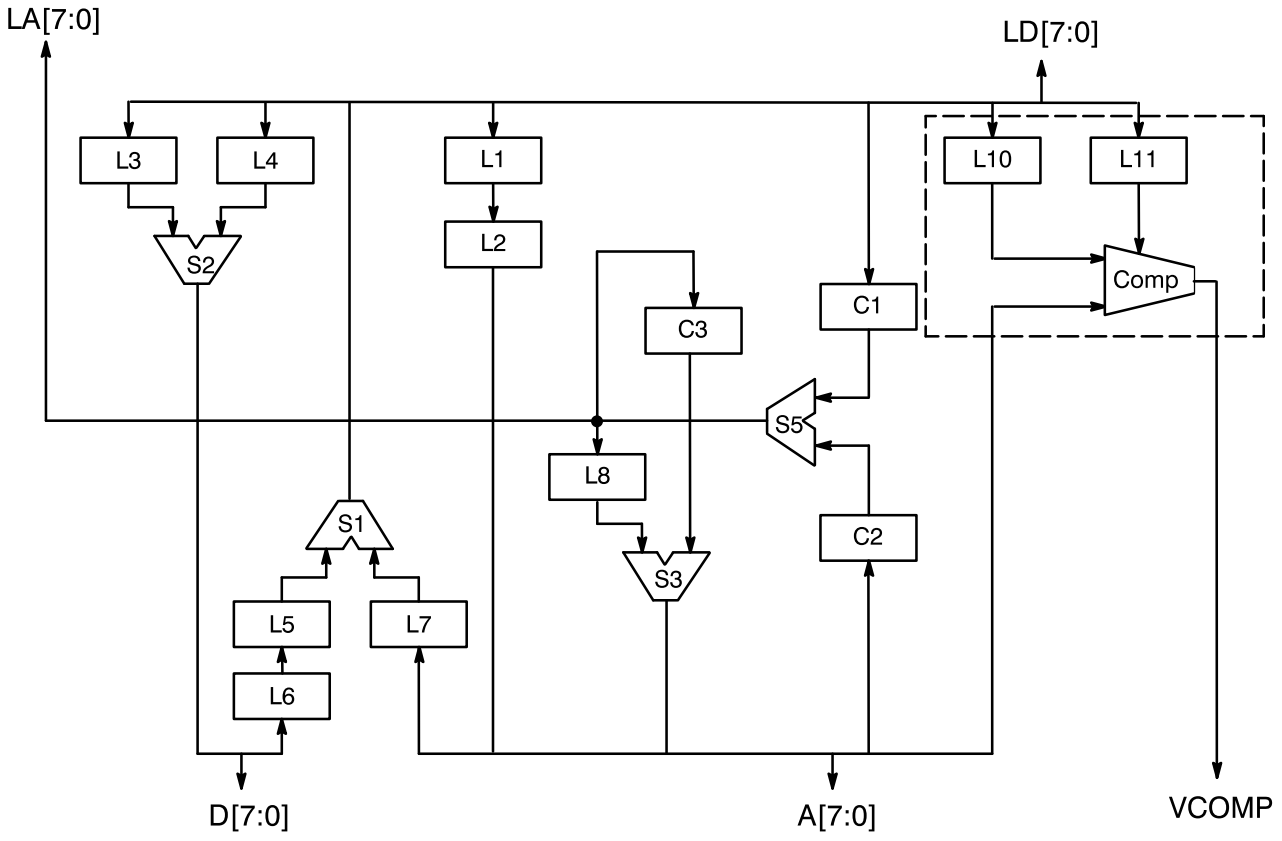

Figure 4−5. CY7C964 Block Diagram: VMEbus Address Comparator

Table 4−11. VMEbus Address Comparator Operation

Logic	Functional Description	Operational Description	Required Condition	Parameter
L10	Select compare register	LDS, MWB* valid to STROBE falling edge	LDS=1, MWB*=1	Set-up t43
				Hold t44
	Load compare register	LD[7:0] valid to STROBE rising edge		Set-up t46
				Hold t47
L11	Select mask register	LDS, MWB* valid to STROBE falling edge	LDS=0, MWB*=1	Set-up t43
				Hold t44
	Load mask register	LD[7:0] valid to STROBE rising edge		Set-up t46
				Hold t47
	Compare out	A[7:0] valid to VCOMP* valid		Prop t23
		A[7:0] valid to VCOMP* invalid		Prop t24
	Minimum pulse width	STROBE minimum pulse width		t47

4.5.8 VMEbus D64 Block Transfer Data Pipeline and Multiplexer

Latches L1 and L2 form a two-stage high-performance data pipeline for D64 block transfer operations. These latches load from the local signals LD[7:0], but drive VMEbus address signals A[7:0]. Latches L3 and L4 load from the local data signals LD[7:0] and in combination with multiplexer S2 drive D[7:0]. On the first cycle of a D64 block transfer, data on LD[7:0] is written to latch L1. During the second local data fetch of a D64 block transfer operation (D64=1), data from LD[7:0] is written to latch L3 and the data within latch L1 moves to L2. Two fetches must be performed to form the 64-bit block transfer data word. During non-D64 modes of operation (D64=0), data from LD[7:0] is written to latch L4. This is the normal data path from LD[7:0] to D[7:0] for all non-D64 operation. Because all the latches are implemented on transparent latches, L2 may be loaded from LD[7:0] when L1 is transparent (LEDO=0). None of the latches are initialized at power-up. Therefore, for predictable operation, these latches should be written prior to their use.

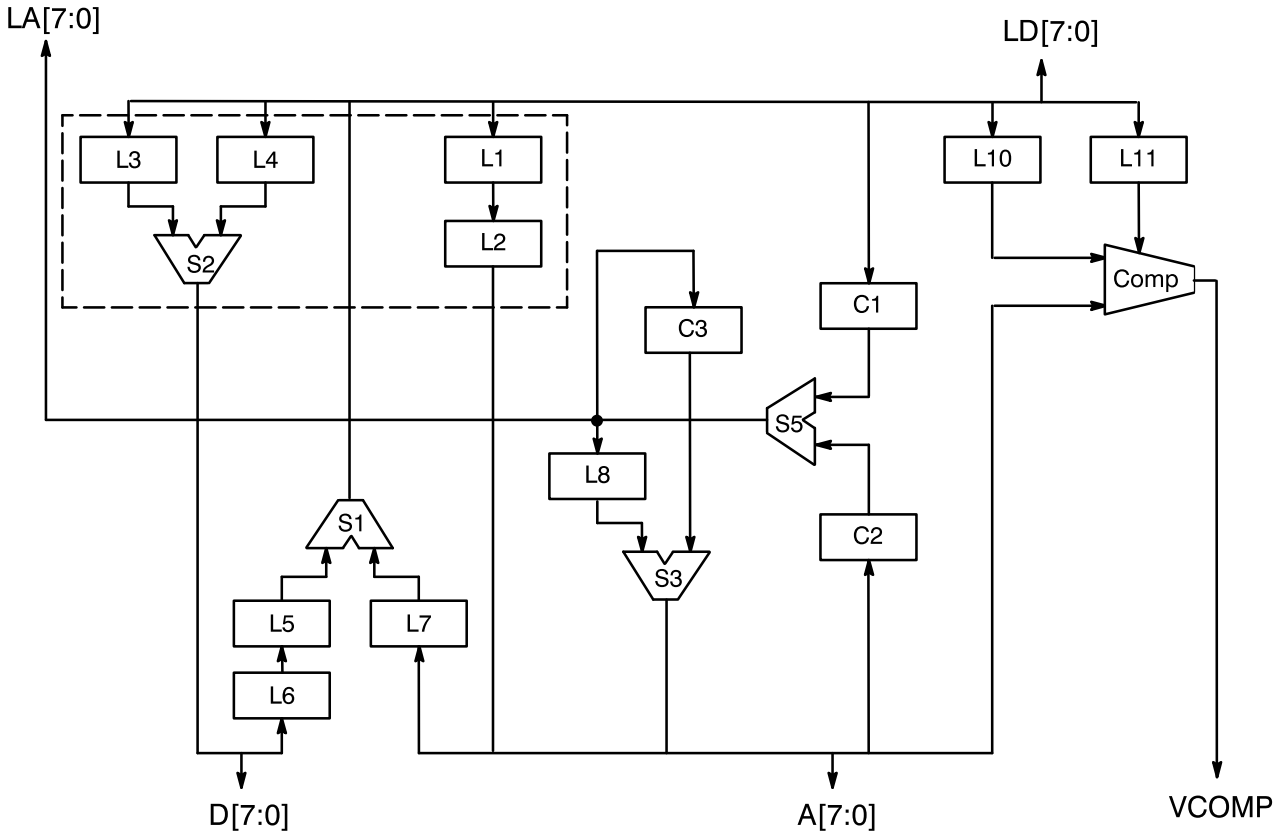

Figure 4−6. CY7C964 Block Diagram: D64 Block Transfer Data Pipeline and Multiplexer

Table 4−12. VMEbus D64 Block Transfer Data Pipeline and Multiplexer Operation

Logic	Functional Description	Operational Description	Required Condition	Parameter
L1	Load register	LD[7:0] valid to LEDO rising edge		Set-up t25
				Hold t26
L2	Load register	LD[7:0] valid to DENO* falling edge	LEDO=0	Set-up t28
				Hold t29
	Drive A[7:0]	D64 rising edge to A[7:0] valid	BLT_STATE=1	Prop t82
L3	Load register	LD[7:0] valid to DENO* rising edge		Set-up t25
				Hold t26
L4	Load register	LD[7:0] valid to LEDO rising edge		Set-up t131
				Hold t132
S2	Multiplexer selects L3 drive D[7:0]	D64 rising edge to D[7:0] valid		Prop t78
	Multiplexer selects L4 drive D[7:0]	D64 falling edge to D[7:0] valid		Prop t79
	Minimum pulse width	DENO*		t30
		LEDO		t27

4.5.9 VMEbus D64 Block Transfer Data Demultiplexer

The VMEbus D64 block transfer data demultiplexer moves data from D[7:0]/A[7:0] to LD[7:0]. The demultiplexer consists of three latches—L5, L6, and L7—and an output multiplexer, S1. During D64 block transfer operations (D64=1), data is written to latches L6 and L7 simultaneously on the rising edge of LEDI. Multiplexer S1 then selects either latch L6 or L7, depending on the state of LDS as a source for LD[7:0]. In most applications, LDS should be connected to LA2, showing that L7 contains even 32-bit words (addresses 0, 8, $10_{16...}$) and L6 contains odd 32-bit words (address 4, C, $14_{16...}$). Latch L6 is also used for non-D64 operating modes. None of these latches are initialized at power-up and for predictable operation should be initialized prior to use.

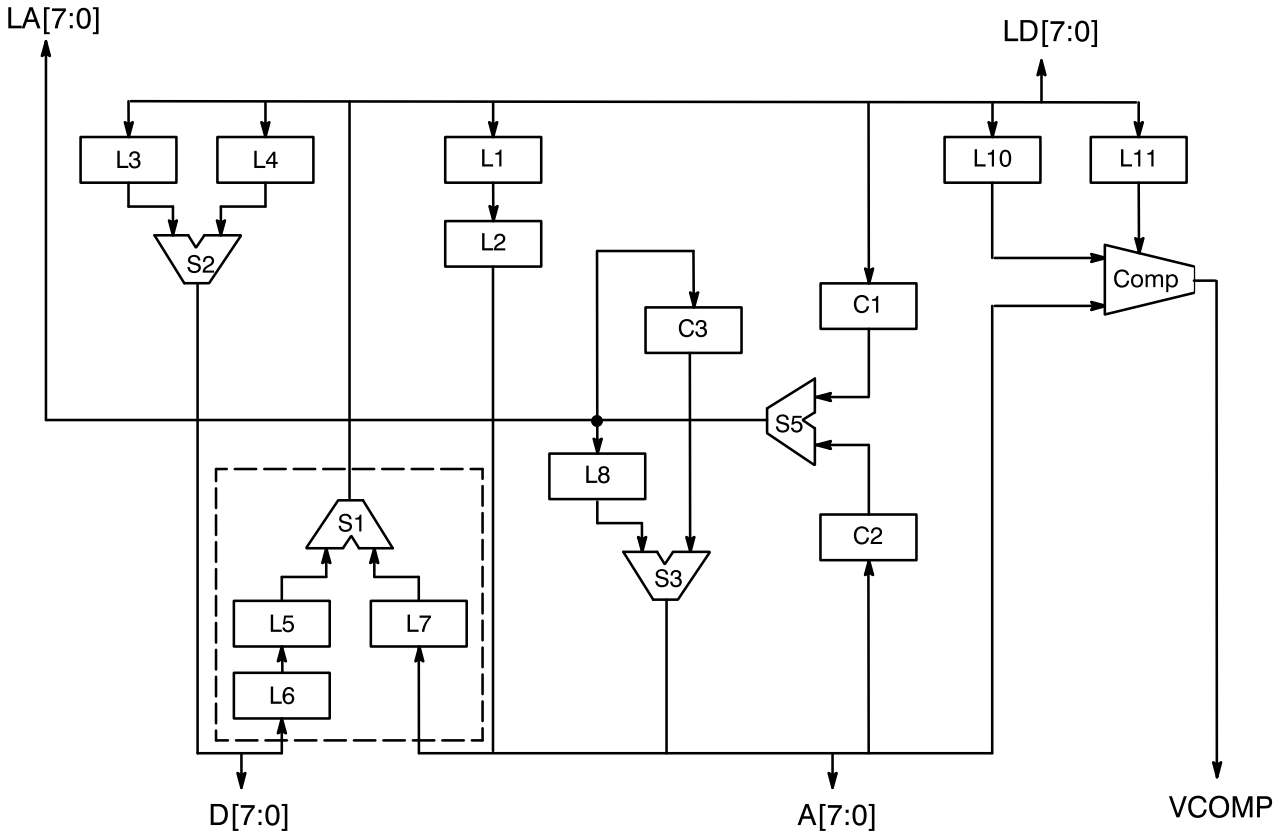

Figure 4−7. CY7C964 Block Diagram: D64 Block Transfer Data Demultiplexer

Table 4−13. VMEbus D64 Block Transfer Data Pipeline and Demultiplexer Operation

Logic	Functional Description	Operational Description	Required Condition	Parameter
L5	Load register	D[7:0] valid to DENIN* falling edge	DENIN1*=0, LEDI=0	Set-up t31
				Hold t32
	Load register	D[7:0] valid to DENIN1* falling edge	DENIN*=0, LEDI=0	Set-up t34
				Hold t35
L6	Load register	D[7:0] valid to LEDI rising edge	LEDO=0	Set-up t37
				Hold t38
L7	Load register	A[7:0] valid to LEDI rising edge	LEDO=0	Set-up t37
				Hold t38
S1	Select L5	LDS rising edge to LD[7:0] valid	D64=1	Prop t74
		D64 rising edge to LD[7:0] valid	LDS=1	Prop t76
	Select L7	LDS falling edge to LD[7:0] valid	D64=1	Prop t75
	Select L6	D64 falling edge to LD[7:0] valid		Prop t77
	Minimum pulse width	DENIN*		t33
		DENIN1*		t36
		LEDI		t39