



CY7C964

Bus Interface Logic Circuit

Features

- Comparators, counters, latches, and drivers minimize logic requirements for a variety of multiplexed and non-multiplexed buses
- Directly drives VMEbus address and data signals
- 8-bit comparator for slave address decoding
- Flexible interface optimized for VMEbus applications
- Companion device to Cypress VMEbus family of components
- Replaces multiple SSI/MSI components
- Cascadable
- 64-pin QFP and 68-pin PGA packages
- See the *VMEbus Interface Handbook* for more information

Functional Description

The CY7C964 integrates several space-consuming functions into one small package, freeing board space for the implementation of added-value board features. It contains counters, comparators, latches, and drivers configured to be of value to implementors of any backplane interface with address and data buses, particularly VMEbus interfaces. The on-chip drivers are suitable for driving the VMEbus directly. The CY7C964 is ideal in applications where high-performance and real estate are primary concerns.

Although having many applications, the Bus Interface Logic Circuit is an ideal companion part to Cypress's VMEbus family of components, the VIC068A, VIC64, the CY7C960, and CY7C961. It is intended to drive the address and data buses, so three or four of these small devices are needed per control-

ler. In every case, the controllers provide the control and timing signals to the Bus Interface Logic Circuit as it acts as a bridge between the VMEbus and the Local bus.

Application with VMEbus Architecture

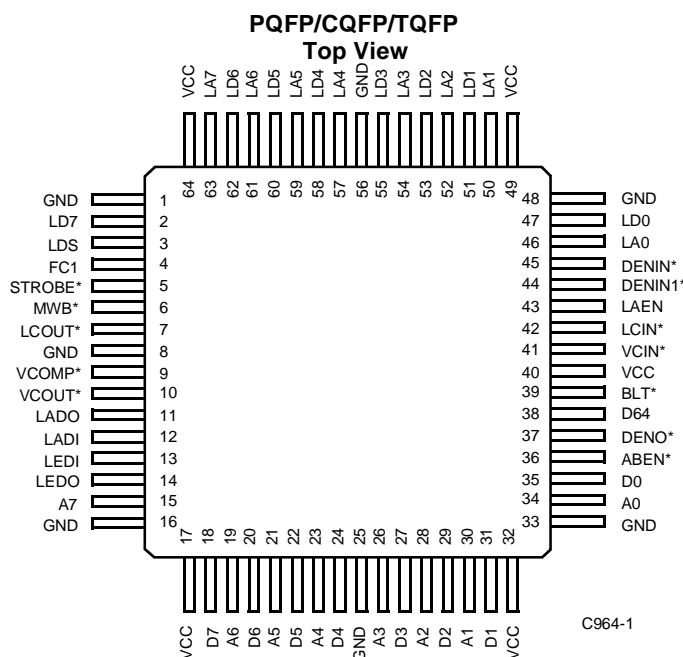
Use with Cypress VMEbus Controllers

The CY7C964 Bus Interface Logic Circuit is a seamless interface between the VIC068A/VIC64 and the VMEbus signals. The device functions equally well in the established 32-bit VMEbus arena and the new 64-bit VMEbus standard. The device contains three 8-bit counters to fulfill the functions of Block counters, and DMA counters as implied by the D64 portion of the VMEbus specification. It also contains the necessary multiplexing logic to allow the 64-bit-wide VMEbus path to be funnelled to and from the 32-bit local bus. Control circuitry is included to manage the switching of the 32-bit address bus during normal (32-bit) operations, and during MBLT (64-bit) operations. The on-chip drivers are capable of driving the VMEbus directly (48 mA).

Use in Other VMEbus Controller Implementations

The CY7C964 circuitry is designed to be of use to designers of VMEbus circuitry, including VSB (VME subsystem bus) and designs not requiring the features of the Cypress VIC068A, VIC64, CY7C960, and CY7C961. The logic diagram includes general-purpose blocks of comparators, counters, and latches that can be controlled using the flexible control interface to allow many different options to be implemented. Although the device is packaged in a small 64-pin package, the use of multiplexed input and output pins provides access to the many internal functions, thus saving external circuitry.

Pin Configuration



Pin Configuration (continued)

68-Pin Ceramic PGA
Bottom View

| | | | | | | | | | | | | | |
|-----------------|-----------------|-------|-------|-----------------|--------|---------|---------|-----|-----------------|-----------------|-----------------|---|---|
| | | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | |
| | A0 | ABEN* | D64 | V _{CC} | LCIN* | DENIN1* | LA0 | GND | V _{CC} | | | | A |
| GND | GND | D0 | DENO* | BLT* | VCIN* | LAEN | DENIN* | LD0 | V _{CC} | LA1 | | | B |
| V _{CC} | D1 | | | | | | | | | LD1 | LA2 | | C |
| A1 | D2 | | | | | | | | | LD2 | LA3 | | D |
| A2 | D3 | | | | | | | | | LD3 | GND | | E |
| A3 | GND | | | | | | | | | LA4 | LD4 | | F |
| D4 | A4 | | | | | | | | | LA5 | LD5 | | G |
| D5 | A5 | | | | | | | | | LA6 | LD6 | | H |
| D6 | A6 | | | | | | | | | LA7 | V _{CC} | | J |
| D7 | V _{CC} | A7 | LEDI | LADO | VCOMP* | LCOUT* | STROBE* | LDS | GND | V _{CC} | | | K |
| | GND | GND | LEDO | LADI | VCOUT* | GND | MWB* | FC1 | LD7 | | | | L |

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Application with Other Bus Architectures

The CY7C964 is optimized for applications requiring wide buffers and high-performance multiplexing operations. The architecture can be configured to provide functions such as 16-bit bidirectional three-state latch and 16-bit comparator with mask

register, or more complex functions such as 16-to-8 pipelined bidirectional multiplexer with address counter/comparator circuitry. The device can be cascaded to generate counters and comparators suitable for multiple byte address/data buses. The on-chip 48 mA drivers can be directly connected to many standard backplane buses.

Ordering Information

| Ordering Code | Package Name | Package Type | Operating Range |
|---------------|--------------|------------------------------|-----------------|
| CY7C964-ASC | A64 | 64-Pin Thin Quad Flatpack | Commercial |
| CY7C964-NC | N65 | 64-Pin Plastic Quad Flatpack | |
| CY7C964-GM | G68 | 68-Pin Ceramic PGA | Military |
| CY7C964-GMB | G68 | 68-Pin Ceramic PGA | |
| CY7C964-UM | U65 | 64-Pin Ceramic Quad Flatpack | |
| CY7C964-UMB | U65 | 64-Pin Ceramic Quad Flatpack | |

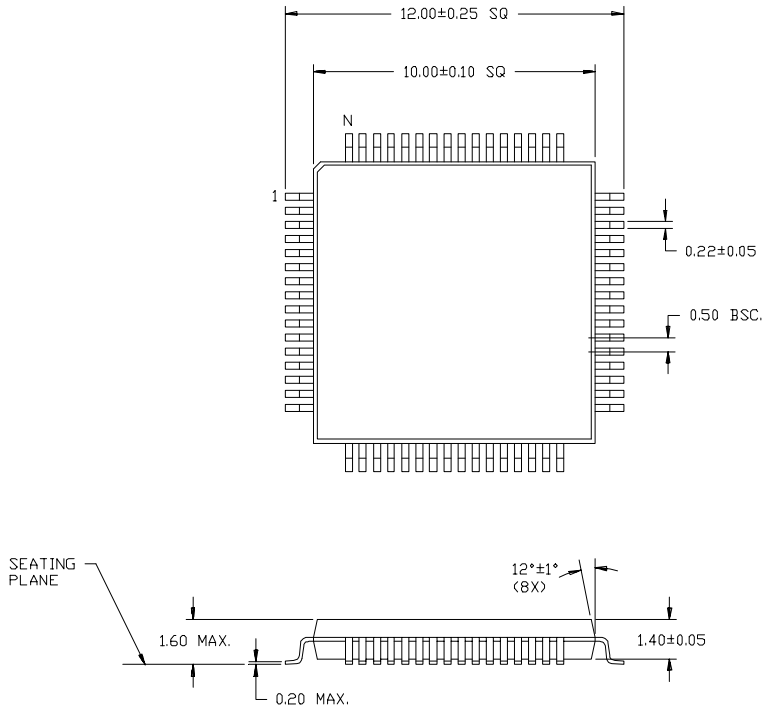
Related Documents

VMEbus Interface Handbook

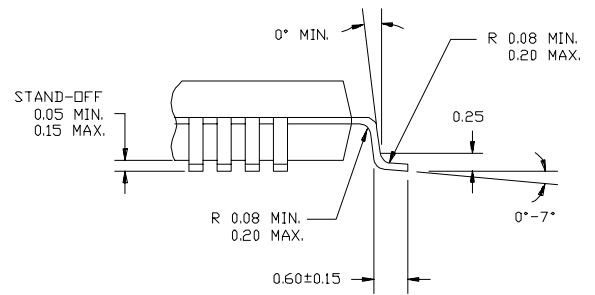
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Package Diagrams

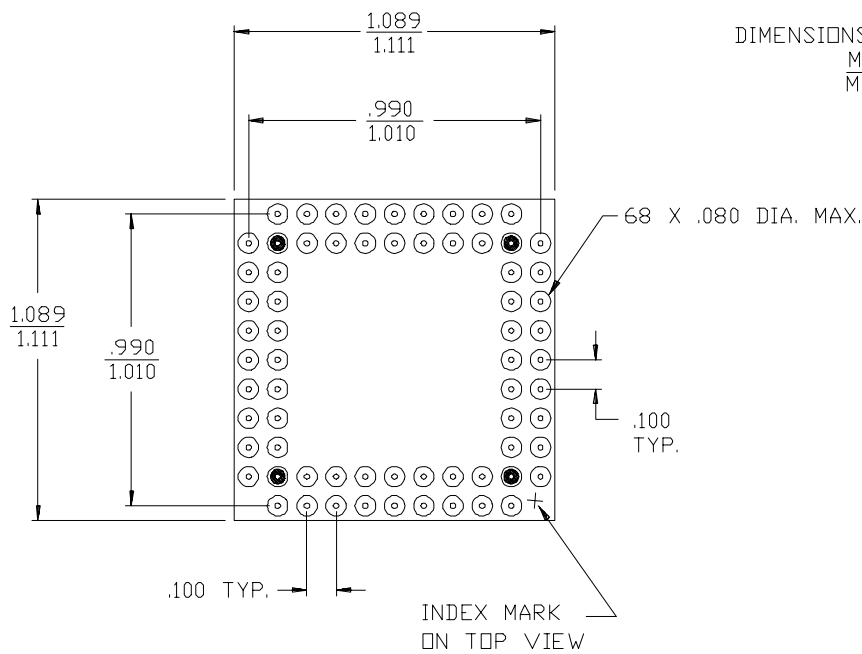
64-Pin Thin Quad Flatpack A64



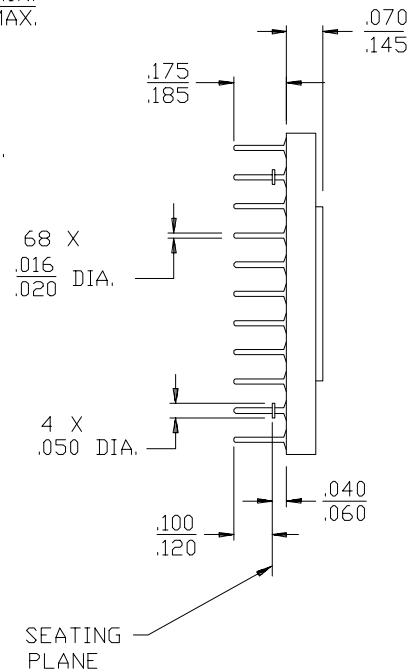
DIMENSIONS IN MILLIMETERS
LEAD COPLANARITY 0.080 MAX.

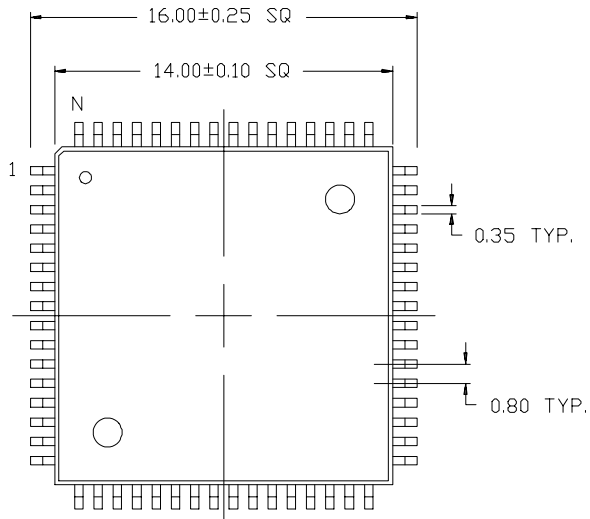


68-Pin Grid Array (Cavity Up) G68

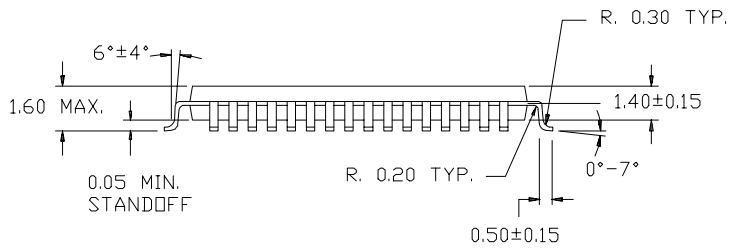


DIMENSIONS IN INCHES
MIN.
MAX.



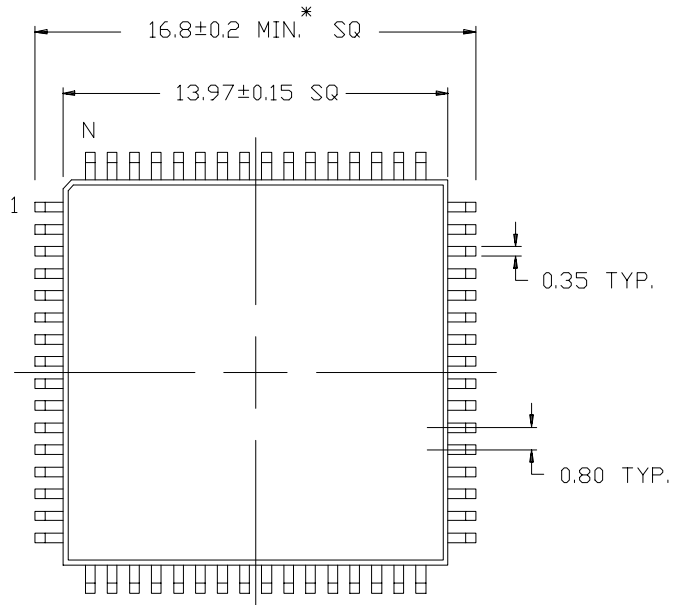
Package Diagrams (continued)
64-Lead Plastic Thin Quad Flatpack N65


DIMENSIONS IN MILLIMETERS
LEAD COPLANARITY 0.102 MAX.



Package Diagrams (continued)

64-Lead Ceramic Quad Flatpack (Cavity Up) U65



DIMENSIONS IN MILLIMETERS
 LEAD COPLANARITY 0.102 MAX.
 DIMENSION MIN.
 MAX.

