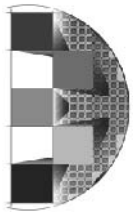


System Design & Troubleshooting

Application Note

Document Number: 9000000_AE005_01
Document Status: Relased
Release Date: December 2001

Tundra Semiconductor Corporation

Trademarks

TUNDRA is a registered trademark of Tundra Semiconductor Corporation (Canada, U.S., and U.K.). TUNDRA, the Tundra logo, System Design & Troubleshooting, and Silicon Behind the Network, are trademarks of Tundra Semiconductor Corporation. All other registered and unregistered marks (including trademarks, service marks and logos) are the property of their respective owners. The absence of a mark identifier is not a representation that a particular product name is not a mark.

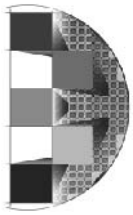
Copyright

Published in Canada

Disclaimer

Tundra assumes no responsibility for the accuracy or completeness of the information presented which is subject to change without notice. In no event will Tundra be liable for any direct, indirect, special, incidental or consequential damages, including lost profits, lost business or lost data, resulting from the use of or reliance upon the information, whether or not Tundra has been advised of the possibility of such damages.

Mention of non-Tundra products or services is for information purposes only and constitutes neither an endorsement nor a recommendation.



1. Tundra Device System Design & Troubleshooting Application Note

Each Customer of Tundra has their own method of designing and debugging their boards; this document outlines some suggestions from Tundra's Applications Engineering team, gained from their experience debugging customer designs.

1.1 Design Tips

Since each design is unique, all of the suggestions outlined below may not apply to your design.

- Read the Device Manual, Errata, Application Notes and Design Notes. The answers to most of the questions we receive can be found in the documentation.
- When you do have a question check the FAQ database (www.tundra.com/faq/) first.
- Read the documentation for all devices over 2 pins in size.
- Review the Evaluation / Reference Board Schematics (Evaluation software if you are creating software).
- If your design varies drastically from the Evaluation board, verify it will work by ensuring you understand the implications of the design changes/ differences.
- Ensure you have debug ports for all bused signals (even if you don't populate them). This will ensure that when a problem arises you can quickly isolate what is ocurring without having to solder hundreds of wires to your board.
- Ensure your power is clean with decoupling caps.
- Minimize clock errors by using clock buffers where youwherever possible.
- Minimize clock line lengths to minimize skew (choose your buffers carefully).
- Ensure clocks are point to point.
- Shield the clock lines to reduce or remove noise on the clocks.

- Follow all design rules (for example, PCI placement, RapidIO trace lengths).
- Perform a netlist check before sending your board design for fabrication.

1.2 Bring up of your design

Now that you have your design finished it is time to ensure that you will not have any problems once your board arrives back in your lab for the first power-up. Below is a list of the key items which Tundra has found invaluable.

- Do you really understand the design? (before you go to layout and get into lab)
- Check PCB before assembly (shorts power& Gnd)
- Check PCB form factor / connectors

Assembly

- Verify the board stuffing to eliminate potential assembly related problems.
- check power planes & ground continuity (shorts?).
- apply power & check current on each source using a current limiting supply.
- apply power & check voltages of each power plane.
- check that the clocks are clean.
- initial set-ups (jumpers / switches).

Program all FPGAs / Programmable devices including boot proms for the local processor.

- Try PCI configuration read of registers using Host (or similar transaction if there is no PCI bus)

1.3 Troubleshooting your design

Below is a list of steps that we recommend you follow when you find a problem on your board. However, since each design is unique, not all of the suggestions outlined below will apply to your design.

1. Determine you have a problem then document the problem. For example if the bus is “frozen”:
    - what are the states of the control signals?
    - what was the last cycle?
    - what was the second last cycle?

    - what is the state of the other busses ? (if any)

2. Isolate the problem such that it can be reproduced regularly and quickly (remove extra code, cards etc.)
3. Find the problem (see Finding the problem below)
4. Fix the problem.
5. Prove that the fix works by running the worst case (as found in step #2) and the normal set-up.

1.4 Finding the problem

Once you have isolated the problem such that you can reproduce it regularly and quickly you can determine the problem's cause using the steps below.

- Place your logic analyzer on all suspected busses (and either side of the suspect part)
- When in doubt of a signal seen on an analyzer use a scope
- Using a scope, check the quality of all clocks and suspect control signals (before, during and after the problem).
- Verify that all set-up and hold times are met for all suspect signals.
- Vary the clock frequencies.
- Vary the temperature artificially to gain timing differences between devices
- Delay or advance the clock to one or multiple chips in the system
- Verify your design against any available design checklist (see www.tundra.com for the latest Tundra documents).

1.5 Still experiencing a problem?

If you are still stuck after following the steps outlined here, Tundra's Applications Engineering team is available to help you. The more information you are able to provide Tundra the faster they can help you resolve your problem.

Before contacting Tundra's Applications Engineering team for support, please complete the following information:

- A complete description of the problem.
- What transaction you are trying to perform.
- Who is the master and slave for the transaction (on all busses)

- Soft copy of timing analyzer trace of the problem transaction at the point of the problem.
- Soft copy of the block diagram and schematics of the system (with off page references).
- Provide a description of the Schematics (in text format).
- Provide a description of the Application and basic data/ control flow.
- Analog scope view of all clocks related to the Tundra Part.
- Analog scope traces of relevant signals around the time of the fail, to check for noise.
    - Relevant Signals: All Control Signals, Clocks, as many data signals as possible.
- Register dump of Tundra parts before and after the problem
- Full part number for the Tundra part in Question