CA91C078 App Note
Interfacing the SCV64 to the VMEbus

BUFFERED SIGNALS

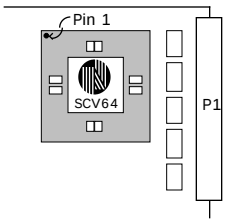
The SCV64 requires ten 8-bit transceivers (or five 16-bit) to buffer the VME address, data, address modifiers, and strobes. While always enabled, the direction of each of these transceivers is controlled by one of three signals generated by the SCV64 (VADDROUT, VDATAOUT, and VSTRBOUT) as shown in the accompanying figure (Figure 1 on the following page).

Tundra Semiconductor recommends the use of '245 transceivers in the VMEbus interface. In particular 'F245, 'FCTAT245, and 'ABT245 may be used. The most commonly used component is the 'F245. These buffers are available in a wide range of packages from many vendors with up to 36 transceivers per package. The low profile of the TSOP package allows the mounting of these components on the backside of VME boards, so this package may be of particular interest to designers with limited real estate. In addition AMP Inc. has developed P1 and P2 connectors with integrated transceivers. Contact your AMP representative for more details about these connectors.

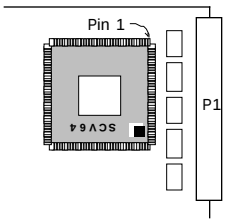
DIRECT CONNECTS

There are many VME signals on the SCV64 that are directly connected to the VMEbus. Although the SCV64 provides enough drive capability to meet VMEbus specification requirements for these lines, note that in order to satisfy the "2-inch" rule, all sources of drive on the VMEbus must be no further than 2 inches from the backplane. While this is a rather archaic rule, it is always best to minimize any potential loading and reflection problems.

To meet the requirements of the "2-inch" rule, the SCV64 should be placed in an orientation on the board that minimizes the distance of the direct connect pins to the connector as shown in Figure 2 below:



CPGA Orientation



PQFP Orientation

Figure 2: Orientation of the SCV64 (CPGA and PQFP) to Minimize Distance to the Connector

BGIN[3:0] SIGNALS

While the BGIN[3:0] signals are direct connects to the backplane bus grant daisy chain, these signals also serve special purposes for system controller configuration and determination. The SCV64's Auto-Syscon Detect mechanism relies upon BG3IN to determine its system controller status at system reset. If BG3IN is low immediately after system reset, then the SCV64 will automatically become the system controller. Otherwise, the system controller functions are disabled. This feature is part of the new VME64 specification, and is fully compliant with revision C systems.

To make use of Auto-Syscon Detect feature, the SCV64 requires a pull-down resistor of approximately 4.7kΩ on the BG3IN signal. This will not in any way impact the performance of the bus grant daisy chain. With this resistor in place, no jumpers are required to configure system controller enabling.

When a card is configured as the system controller, the other three bus grant in signals, BGIN[2:0] , are typically unused. However, the SCV64 uses the BG0IN signal as an off card reset, while the other two signals may be used as off-card configuration inputs, monitored through internal registers.

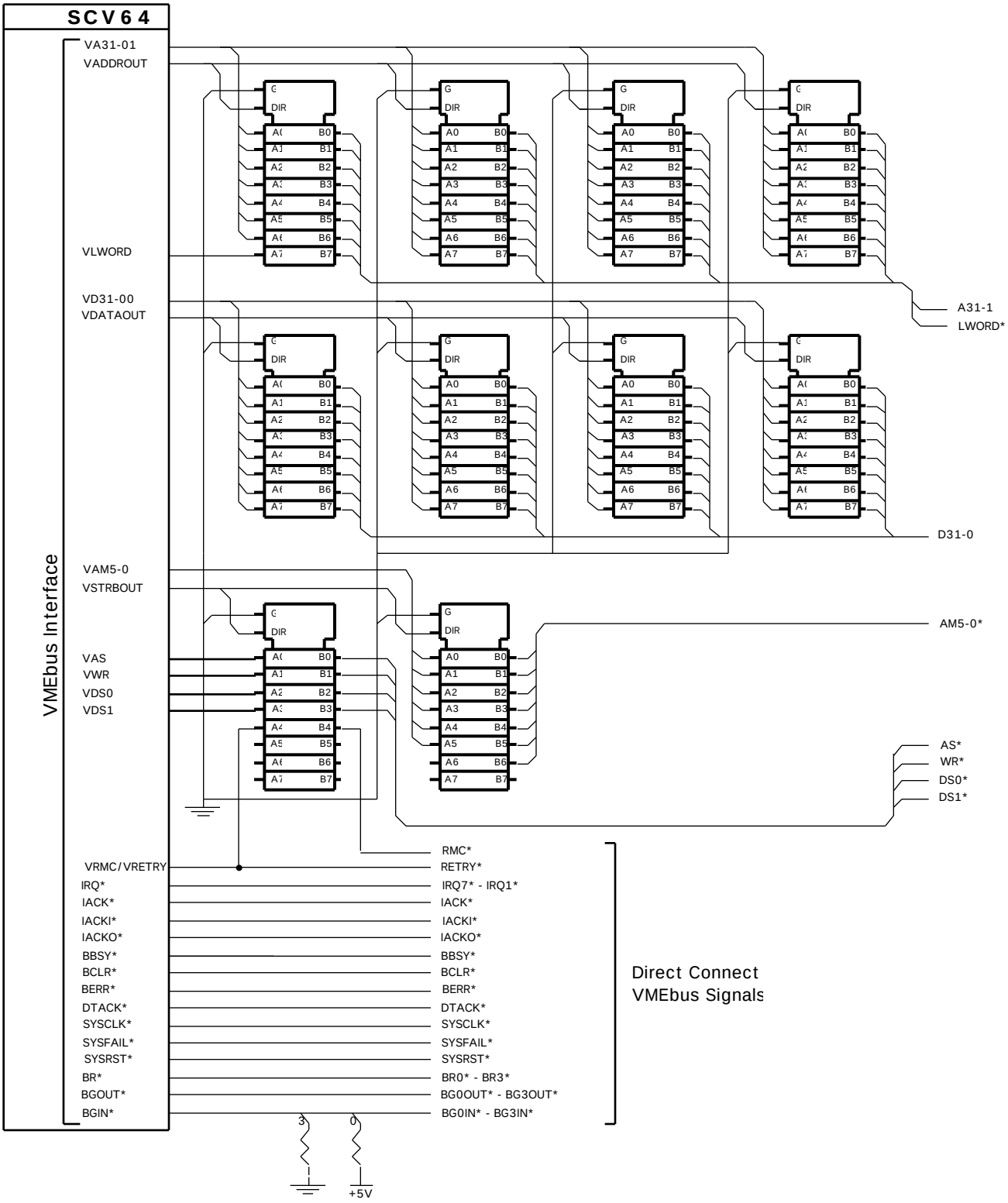


Figure 1: SCV64 Interface to VMEbus

BG0IN will act as an active-low system reset signal when the SCV64 is the system controller. If the BG0IN signal is used in this capacity, then all SCV64 equipped cards must put a pull-up resistor on the BG0IN signal of approximately 4.7kΩ.

BG1IN and BG2IN are configuration inputs only, monitored through the STAT1 register. Since they are non-functional signals, these signals do not need to have pull-ups or pull-downs on them, and may be just left directly connected to the VMEbus. Alternatively, they may be connected to chassis mounted switches.

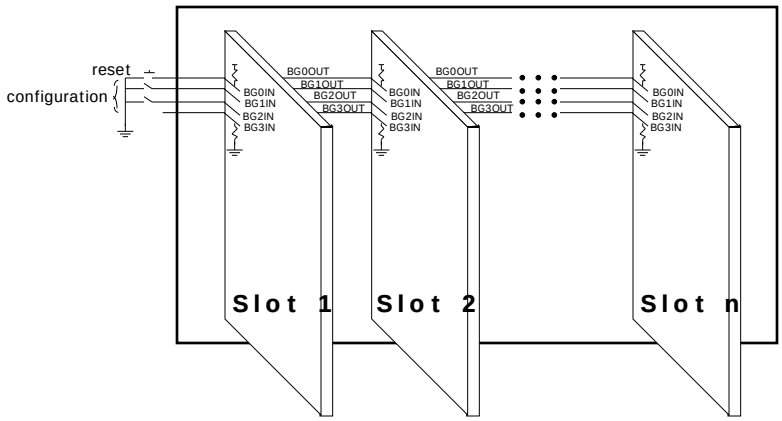


Figure 3 : Bus Grant Daisy Chain Usage In System

RETRY*/VRMC

The SCV64 has a dual purpose pin, RETRY*/VRMC, which may be used as either the VME64 specification RETRY* line, or may be used as a Tundra proprietary read-modify-write (RMW) cycle pin. (Refer to the SCV64 User Manual for more information about the read-modify-write cycle.) The configuration of the RETRY*/VRMC pin is controlled by the RMCPIN bit in the MODE register, and defaults to use as the VRMC pin.

When configured as the VRMC pin, the signal is a bi-direct and must be buffered through a transceiver with direction controlled by VSTRBOUT. One of the unused inputs on the strobe transceiver may be used for this purpose. When configured as RETRY*, the signal acts only as an input. It may be directly connected to the backplane.

RETRY* is defined in the new VME64 specification as occupying the B3 (formerly reserved), on the P2 connector. However, many current implementations of VRMC use that same pin. To maintain compatibility with other board vendors using Tundra's VME interface components, it may be necessary to continue to use this pin, in violation of the new definition of this pin in the VME64 specification. Note that this will only be possible if P2 pin B3 is not being used as the RETRY* in other parts of the system.

To provide as much flexibility as possible, many board vendors choose to use a jumper option to provide the capability of having the pin operate as either the VRMC pin on P2 pin B3, or as RETRY*. This jumper either takes the buffered version of the signal through the transceiver for VRMC, or the direct connect for RETRY*. (see Figure 4 below).

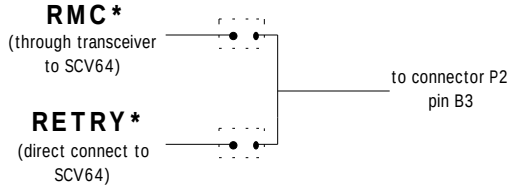


Figure 4 : Implementation of VRMC and RETRY*

Note that if either VRMC or RETRY* is implemented on P2 pin B3, that this signal should be properly terminated on the backplane. VME64 style backplanes will already have provision for the termination of this line. If termination is not provided on the backplane, ensure that there is termination on-board to pull RETRY*/VRMC to the inactive state.

If neither VRMC or RETRY* is to be implemented on the board, ensure that the RETRY*/VRMC is pulled to the inactive state (high) to ensure proper function.

BI-MODE AND IRQ1*

The SCV64's BI-Mode feature may be triggered through four mechanisms:

- reset,
- assertion of the BITRIG pin,
- software (through the SBI bit), and
- assertion of IRQ1* (when configured as such).

IRQ1* defaults upon reset to being a BI-Mode initiator, which means that the SCV64 will enter BI-Mode whenever IRQ1* is asserted. When configured as BI-mode initiator, IRQ1* triggers a local interrupt on level 7 (if so enabled through the BIE bit in the 7IE register). When configured as an interrupt source, a local interrupt on level 1 is generated upon assertion of IRQ1* if that level is enabled in the VIE register.

To reconfigure this signal as an interrupt only, the VI1BI bit in the GENCTL register should be cleared, typically as part of a reset routine.