CA91C078 Application Note
SCV64 Slave Only Application

The SCV64 is intended for use both in applications where a local processor is provided and in applications where no local intelligence processor is provided. This is achieved primarily through a power-up option enabling the device to automatically initialize all internal registers required to enable access to the VMEbus.

INITIALIZATION

All internal register bits required for VMEbus operation are set automatically when the AUTOBAR power-up option is enabled. This option is enabled by pulling KFC2 high and KFC0 low at the rising edge of $\overline{\text{PWRRST}}$. At this time, the VMEBAR register is loaded with the value on the local data bus and all required internal bits are set to enable slave access to the device.

VMEBUS PROGRAMMING

In conjunction with the automatic initialization of the device, additional register accesses may be required to complete initialization of the device or to reprogram functionality. This is achieved by programming any additional internal registers from the VMEbus. Access to the internal registers is made through the slave image programmed during automatic initialization of the device. The SCV64 will generate a cycle on the local bus of the SCV64 in the same way as an access to local memory or any other local bus device. This cycle must be decoded to generate a chip select signal for the SCV64 ($\overline{\text{SCV64SEL}}$). The SCV64 accepts the register access from the local bus and terminates the local cycle with $\overline{\text{KDSACK}}$. Access to the local bus for register programming may be through either A24 or A32 addressing spaces.

An example circuit diagram is provided. In this circuit, an addressing decoding block decodes the select signal for the SCV64 ($\overline{\text{SCV64SEL}}$) in addition to any other select signals required on the local bus. A transceiver in conjunction with user defined programming (resistors or jumpers) provides A24 programming bits for the VMEBAR register during the rising edge of $\overline{\text{PWRRST}}$. 7 bits are shown which select the A24 base address and size. All unused A32 base address and size bits are left undefined in this example. VMEBAR register bits may be left undefined provided that system design and initialization are unaffected by undefined A24 or A32 images. In this case, all initialization must be completed using the defined A24 address space. Alternatively, logic could be provided to program both A24 and A32 base addresses and sizes during power-up.

If there are no other potential masters on the local side $\overline{\text{KBGR}}$ can be tied to $\overline{\text{KBRQ}}$.

Tel: (613) 592-0714 • 1-800-267-7231 • Fax: (613) 592-1320
Document Number : 8091078.MD608.02
support@tundra.com

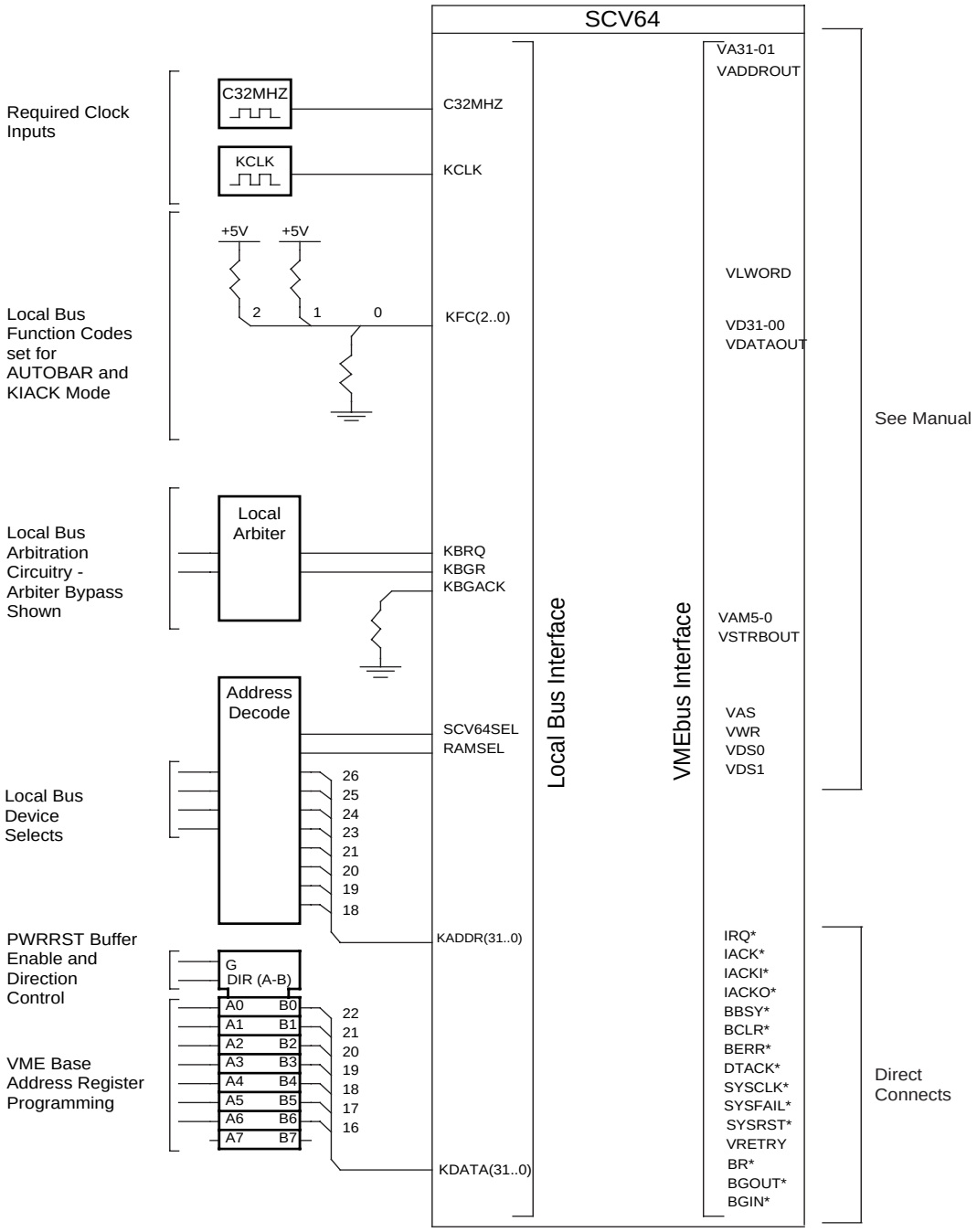

Figure 1 Local Bus Connections for Slave Only Design

Refer to the SCV64 User's manual for directions on how to connect the SCV64's VMEbus Interface.