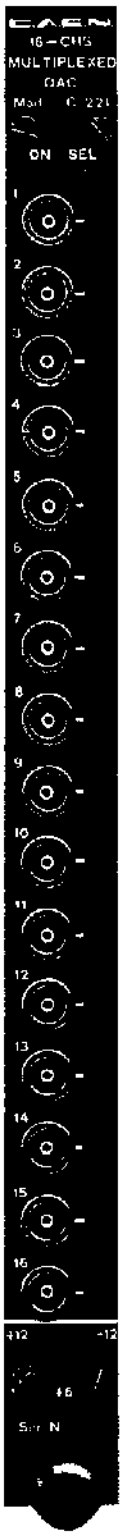
Technical Information Manual

MOD. C 221

16 CH MULTIPLEXED DAC

5th June 1992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1. INTRODUCTION

Model C 221 is a 16 Channel Multiplexed DAC whose outputs (voltages) are digitally programmable through a 12 bit digital to analog converter connected to 16 "sample and hold" circuits.

The module is implemented in a single width CAMAC Unit.

2. GENERAL OPERATION

The voltage value, set via CAMAC W-lines, is stored in one of the 16 internal registers (Digital Memory) selected through the A lines.
These values are cyclically used for the refreshing of the Analog Memories.
The values stored into the digital memory may be read back on the 16 CAMAC R-lines at any time.
It is possible to check the status of the outputs (ON/OFF) during a reading memory operation, through the Dataway line R13.
The output state is visualised with 16 LEDs on the front panel.
Power up, or CAMAC reset procedure, set the voltages of all the channels to zero until the corresponding registers are written via CAMAC functions.

3. DESCRIPTION

3.1 GENERAL

The system may be outlined in the following parts (see Fig.1):
- CAMAC Decoder
- Digital Memory
- Refresh Circuit
- Control Circuit
- DAC
- Enable Output Circuit
- Sampling Circuit.

3.2 DIGITAL MEMORY

The main part of the system is a 16x12 bit **Digital Memory** storing the values of the programmed output voltages. This memory is accessible either by CAMAC or by the internal Refresh Circuit. By CAMAC for standard READ/ WRITE operation, by the Refresh Circuit to direct sequentially the outputs of the DAC to the 16 Analog Memories, via a 1 to 16 De-Multiplexer.

3.3 REFRESH CIRCUIT

The **Refresh Circuit** is used to keep the correct data in the Analog Memory. It causes the sequential commutation of the DAC output through the 16 circuits of the Analog Memory, by controlling the selection inputs of a demultiplexer.
The CAMAC functions F(0), F(16), F(17) with subaddresses A(0) to A(15), select the Digital Memory.
If an F(17) Write cycle operation is used, the CAMAC lines A1-A8 are loaded into the counter holding the addresses for the Refresh cycle. At the end of this CAMAC operation, the Refresh cycle will now restart from the new address set in the counter.
An F(17) function is consequently useful when it is necessary to immediately update an output voltage on a particular channel by by-passing the delay inherent to the scanning cycle. A too frequent use of this function may degradate the content of the Analog Memories thus changing the values of the output voltages.

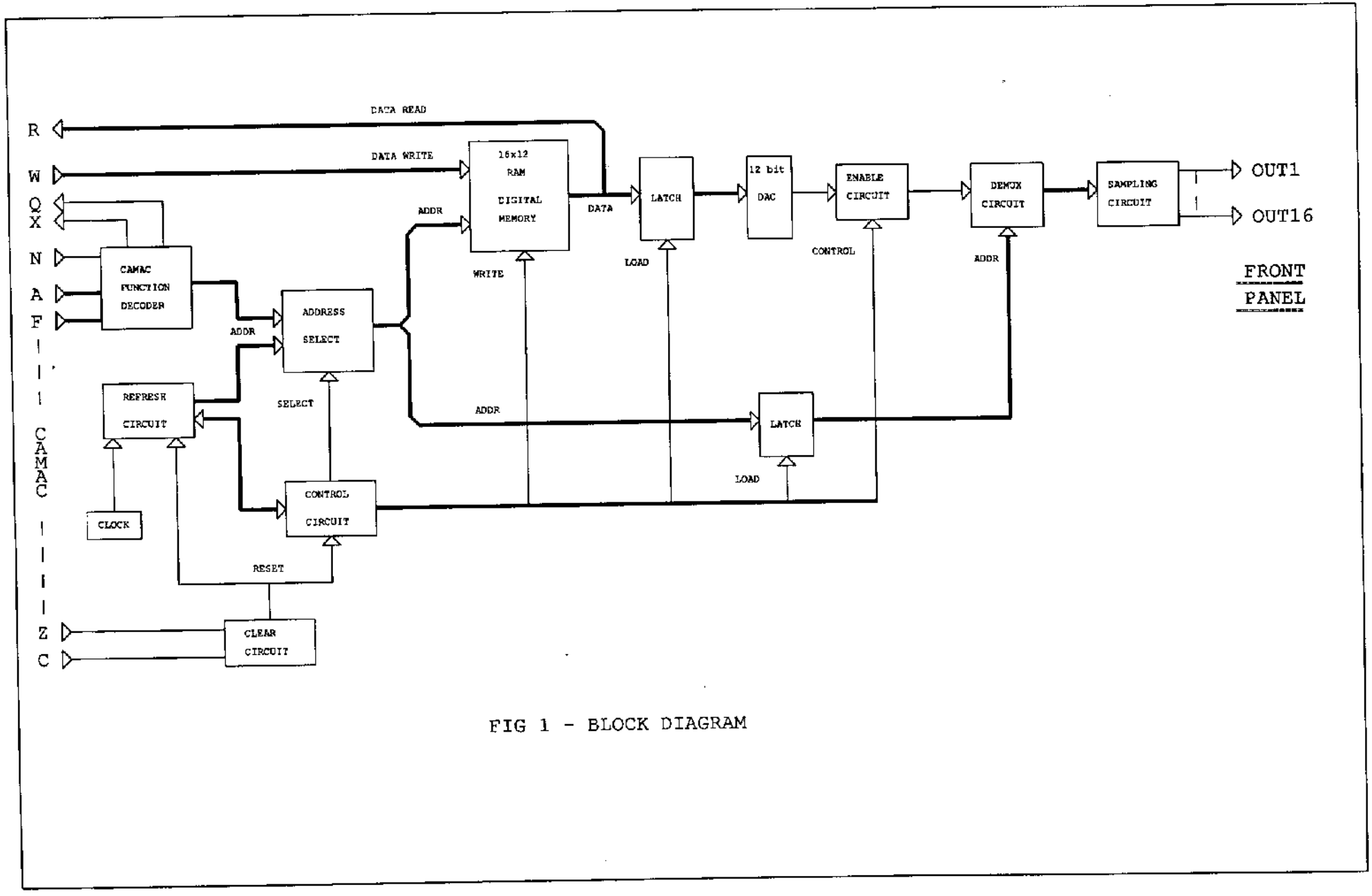

FIG 1 - BLOCK DIAGRAM

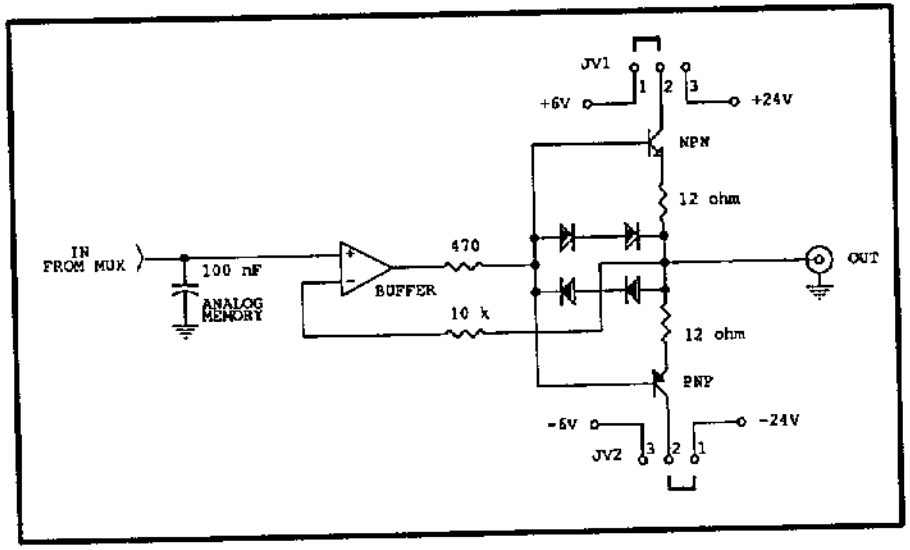

FIG. 2 - SAMPLING CIRCUIT

On the other hand the use of F(0) (READ) or F(16) (WRITE), with a repetition similar to that of the refresh cycle, may cause instability in the output voltage.

3.4 CONTROL CIRCUIT

The System Memory may be accessible by both CAMAC, for standard I/O operations, and by the internal Refresh Circuit.
The **Control Circuit** ensures the normal functioning of the CAMAC and Refresh Circuit operations, by avoiding their possible conflict during memory access.

3.5 ENABLE CIRCUIT

This circuit has the double function of zeroing all the outputs and switching one or more channels ON/OFF.
Due to the fact that the Digital Memory cannot be reset, a 16x1 bit Register is used to switch off the outputs. This Register may be set at the same time the Channel Data are written into the Digital Memory. A bit set on this Register will switch the corresponding input of the De-Mux to ground, thus keeping the output to zero volt.
All the bits of this register are automatically set at power-up, keeping all the 16 outputs to zero volt.

3.6 THE DAC CIRCUIT

The **DAC** used is a General Purpose 12-bit D/A converter. Being of the current- output type, the DAC is followed by a Current-to-Voltage converter.
Through an Analog Switch and a 16 - channel Analog Multiplexer, the output of the Converter is fed to the 16 Analog Memories.

3.7 SAMPLING CIRCUIT

The **Sampling Circuit** (Fig. 2) consists of 16 identical channels, each including the Analog Memory and the Output Stage.
The Analog Memory consists of a 100 nF polyester capacitor connected to a high impedance buffer.
The Output Stage is implemented with two emitter coupled complementary transistors. It can sink/ source up to 50 mA and is short circuit protected.

4. SPECIFICATIONS

4.1 OUTPUT VOLTAGE RANGES

0V to + 10V
0V to + 5V
0V to - 5V
0V to - 10V
-10V to + 10V
-5V to + 5V

The output voltage ranges can be selected through a proper jumper setting (see Fig. 3 and Table 1). The module is set at the Factory to operate in the range 0V to 10V.

4.2 FRONT PANEL

No. 16 coaxial connectors LEMO 00 type
No. 16 LEDs displaying the status of the outputs
No. 3 LEDs displaying the status of the power lines
No. 1 LED monitoring the CAMAC access of the memory
No. 1 LED monitoring the internal Refresh sequence.

4.3 CHARACTERISTICS OF THE SIGNALS

- Output maximum current: +/-50mA
- Resolution: 12 bits
- Differential non-linearity: +/-1/2 LSB
- Integral non-linearity: +/- 1 LSB (max. deviation from a straight line passing through the endpoints of the DAC transfer function)
-Offset on output channels: adjustable via trimmer
-Voltage maximum drift: 50 ppm/°C of F.S.
- Short circuit protection.
-Update time: 2ms max. for F(16),
300 μs for F(17)

4.4 POWER SUPPLY

+6 V at 1.420 A, -6V at 800 mA
+24 V at 800 mA, -24V at 950 mA

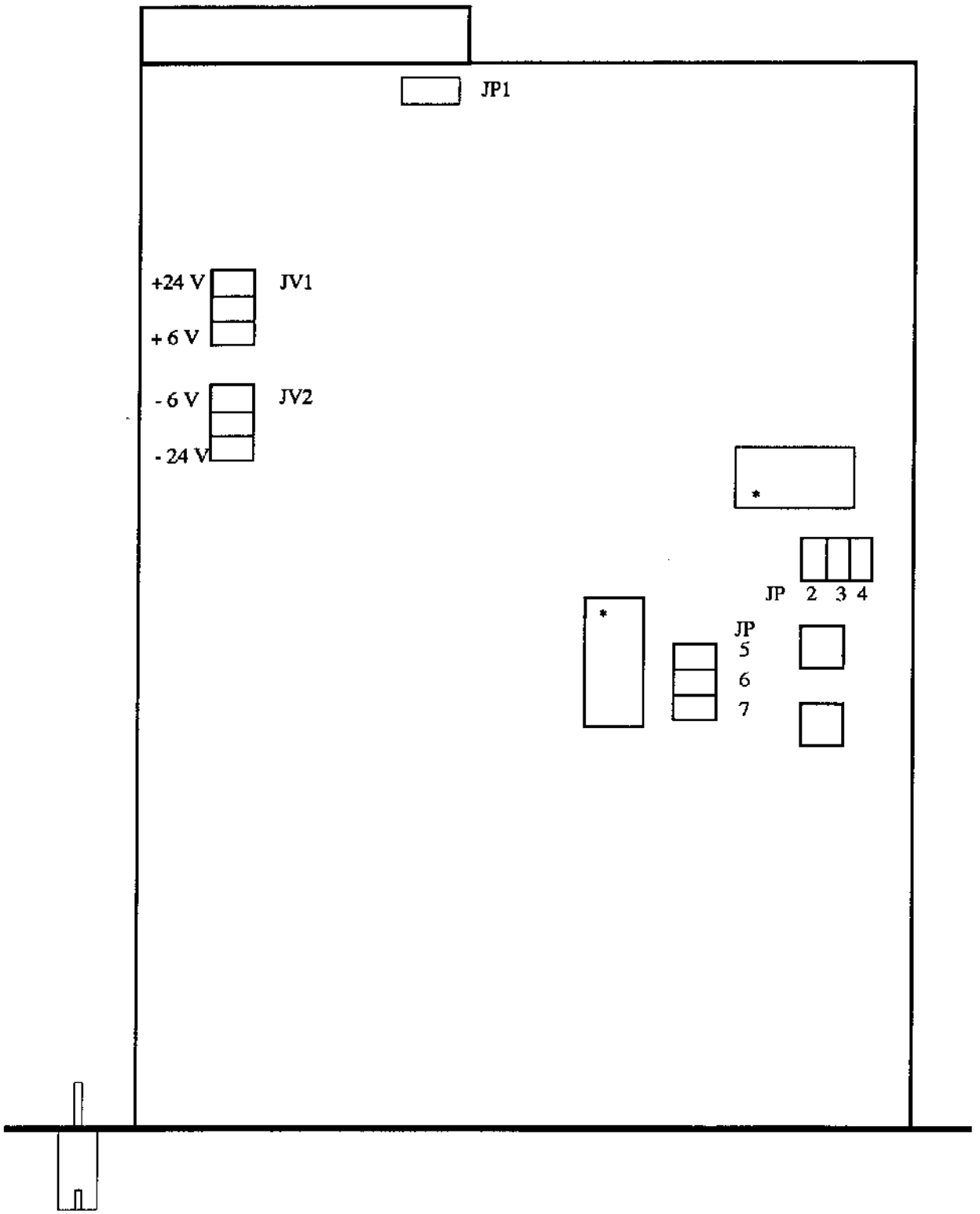

FIG. 3 - JUMPER LOCATIONS (Component Side)

5. CAMAC FUNCTIONS

Commands:

F(0) (A(0) to A(15)) Reads the values stored in the 16 internal registers (Digital Memory):
CH1 corresponding to A(0), CH2 to A(1), etc.
The reading is done through the Dataway lines R1 to R12.
By setting a proper jumper (JP1) it is possible to read the state of the enabling bit on the R13 line (if R13 is ON the channel is enabled).

F(16) (A(0) to A(15)) Writes into the Digital Memory the output voltage values (Dataway lines W1 to W12).

W13 OFF: the output of the selected channel is enabled.
W13 ON: the output of the selected channel is disabled.
This setting is used for RAM test procedure.

F(17) (A(0) to A(15)) It operates similarly to F(16), but the internal Refresh cycle is resetted to the value of the selected address.

ATTENTION:
A too frequent use of the functions F(0), F(16), F(17) may cause the degradation of their content by interrupting the Refresh cycle on the Analog Memories (see p. 3.3).

Controls:

Z or C	All the outputs are disabled and set to 0V.

Status lines:

X, Q	Generated with F(16), F(17), F(0). The signals on these lines are generated by selecting one of the available functions if the access, via CAMAC, to any one of the internal registers is possible. During a reading or writing operation the access via CAMAC is blocked for 15 μs to guarantee the correct Refresh cycle.

6. JUMPER SETTING

Figure 3 shows the physical location of the jumpers on the board.

Table 1 shows the jumper setting.

N.	OUTPUT RANGE VOLTS	JP2	JP3	JP4	JP5	JP6	JP7	JV1	JV2
1	0 to +4.9988	ON	ON	OFF	OFF	ON	OFF	+6	-
2	0 to -4.9988	ON	ON	OFF	OFF	OFF	ON	-	- 6
3	+4.9976 to -5	OFF	ON	OFF	ON	ON	OFF	+6	- 6
4	0 to +9.9976	OFF	ON	OFF	OFF	ON	OFF	+24	-
5	0 to -9.9976	OFF	ON	OFF	OFF	OFF	ON	-	- 24
6	+9.9951 to -10	OFF	OFF	ON	ON	ON	OFF	+24	- 24

TABLE 1 - JUMPER SETTING.