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Front-end electronics of the Belle II aerogel ring imaging detector

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ABSTRACT

A proximity focusing RICH detector with an aerogel radiator is used for charged particle identification in the forward end-cap of the Belle II spectrometer. The detector, consisting of a 4 cm aerogel radiator, a 16 cm expansion volume and a photon detector with 420 Hybrid Avalanche Photo Detectors, is mounted in a very confined space between Central Drift Chamber and Electromagnetic Calorimeter, allowing only 5 cm of space for the readout electronics. In our solution, low power front-end read-out boards are mounted at the back side of each of the HAPD photosensors. These boards have each been tested individually before their installation onto the photosensors and into the spectrometer. Most important design issues and first experiences with the aforementioned front-end read-out boards are presented in this contribution.

1. Introduction

The Belle II spectrometer in Tsukuba, Japan is dedicated to precision measurements of rare decays of B and D mesons and τ leptons [1]. For identification of hadron decay products, a proximity focusing Ring Imaging Cherenkov (RICH) Counter with an aerogel radiator is installed in the 28 cm space between the Central Drift Chamber and the Electromagnetic Calorimeter in the forward end cap of the spectrometer. Cherenkov photons, emitted by charged particles in the aerogel radiator, are detected by a photon detector consisting of 420 144-channel Hybrid Avalanche Photodetector Sensors (HAPD), each with a front-end electronic readout board (Fig. 1) and an HV-divider board at its back [1,2]. The HAPD, the readout board and the divider board are together consisting a Sensor Module. The front-end electronic readout board must be able to detect analog input signals, which are only 35000 e^- high. Due to irradiation damage of the HAPD these signals will gradually decrease during the 10 years of expected spectrometer operation. The whole detector is positioned in a strong magnetic field, thus the boards contain no magnetic materials. The boards are sized to fit the HAPD entrance window surface (75 mm × 75 mm). Due to the limited space available for placement of the electronics — only 5 cm depth between the photon detector mechanical mounting frame and an end-cap cover plate, each of the front-end electronic readout boards is mounted on the back-side of the HAPD, parallel to the entrance window. The digitized signals from up to six front-end boards are collected by a merger board mounted approximately 4 cm above the boards. The electronics is connected via 30 m long cables to power supplies and to the common acquisition system positioned outside of the spectrometer. In the following the RICH detector specific front-end readout board and its operation will be described, alongside with its test results.

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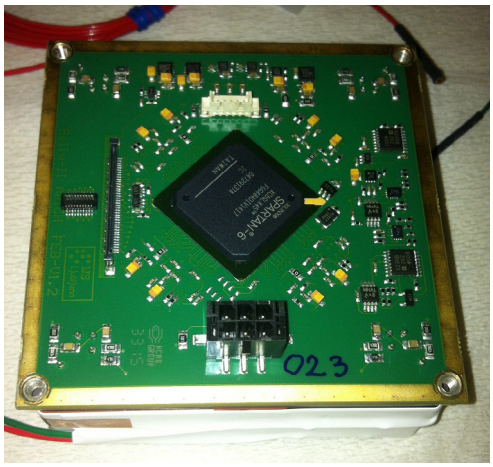

Fig. 1. A photo of the front-end board attached to the HAPD. There are three connectors: one for a data transfer, one for a board power supply and one for a HAPD bias/guard power supply.

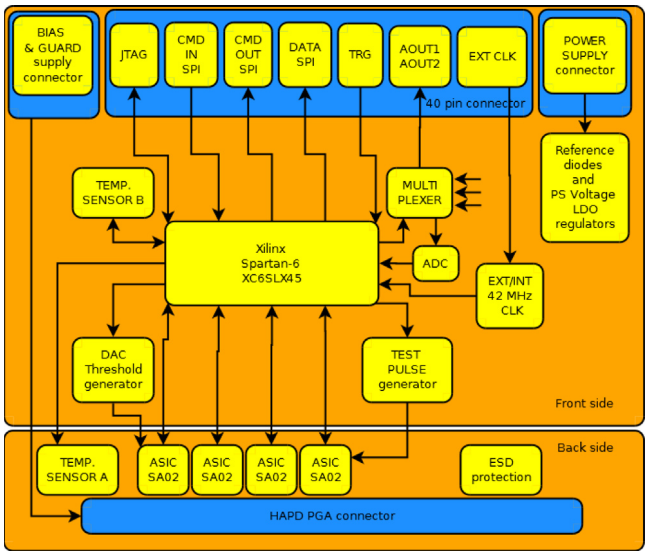

Fig. 2. Functional schematic of the Front-End Board: 4 custom ASICs positioned on the back side of the board digitize the input signals. The digital signals are processed in a Xilinx Spartan-6 FPGA positioned on the front side of the board. The FPGA is responsible for communication and control of the peripheral devices. The front side of the board houses three connectors: a bias and guard supply, a communication and a power supply connector. From three supply voltages, the reference voltage of 1.25 V is generated by a diode, while the other operating voltages are generated by low dropout regulators (LDO). An analog-to-digital converter is used to control the different internal voltage levels, which can be selected by a multiplexer. The chip discriminator level is set by a digital potentiometer. On the board there is also an internal 42 MHz oscillator to clock the FPGA, replaced by an external clock during the operation in the Belle II detector.

2. Front-end readout board

The main purpose of the readout electronics is the discrimination between hit and non-hit HAPD channels. The front-end readout board consists of a 12 layer PCB with a pin grid array connector for the HAPD photosensor and the power supply, bias and data I/O connectors (Fig. 2). The 152 pins HAPD connector has several through-hole pins to gain mechanical stability during possible service sensor detachments. On the photo sensor (back) side, there are 4 custom ASICs, which amplify, shape and digitize 4 × 36 input signals, protected from over-currents with two electrostatic discharge protection (ESD) diode stages. The operation of the ASIC chip is controlled by the internal registers. Its output digital signals are connected to a Xilinx Spartan-6 FPGA. The FPGA, mounted on the front side of the front-end board, controls a discriminator level of the ASIC via a digital-to-analog converter, samples the digital signals and at the trigger signal serializes and sends the data to the merger board. There, the data from up to six front-end boards are collected and sent through an optical link to an experiment data acquisition system. From the merger board, an FPGA firmware can be uploaded via the dedicated JTAG lines. The FPGA accepts the instruction commands via receive, and responds via transmit lines of the data communication cable. The board has a possibility to monitor its supply voltages, temperatures and analog and digital signals from different stages of ASIC. For debugging, the board provides a test pulse signal, generated and controlled by the FPGA.

2.1. Firmware design

The firmware comprises a 64-bit instruction decoder, a data sender, a command receiver and a response sender. The instructions are received via a one way asynchronous Serial Peripheral Interface (SPI). A response of each command is sent back encoded in a response word through a separate dedicated one way SPI. The trigger signal starts the data encoder and sends the data to the merger board through another one way SPI. Each hardware peripheral device has a driver triggered by the instruction decoder. In addition, a data register is used to control a mode of operation, the sampling and the encoder frequencies. The FPGA unique device identifier (DNA) is used to identify the board. The front-end readout board must withstand a 1 MeV equivalent neutron fluence of 10^{12} n/cm^2 and a gamma radiation dose of 100 Gy during the expected lifetime of the Belle II spectrometer. The firmware also includes a Xilinx software SEU mitigation controller which corrects the single event upsets and signals the unrecoverable errors through a separate heartbeat line in the data bus.

3. Board production and quality tests

The front-end boards were produced in 2016 and then tested alone and in the Sensor Module. The tests were comprised of several consecutive firmware downloads, verifications of the voltages and the temperature sensors, and of a loading and a reading of the ASIC operating parameters to and from the ASIC registers. The boards response to random triggered pulses was tested by connecting them to a dummy board, which mimics the capacitance of the final HAPD sensor. In the Sensor Modules, the front-end boards were tested by measuring their response to a focused triggered laser light (λ = 532 nm). By changing the ASIC chip comparator threshold voltage, we measured the response of the Sensor Module to several photons (Fig. 3). Note the sharp steps in the threshold scan demonstrating the ability of the ASIC chip to discriminate between hit and not hit channels. By moving the laser spot over the photo sensor surface, we measured a very homogeneous response (Fig. 4). Over 97% of the boards were fully functional, about 1% were not usable, while 2% were potentially usable having up to five (out of 144) malfunctioning channels.

4. Tests in a high radiation environment

One of the possible limiting factors of the boards is the use of the Xilinx Spartan-6 FPGA. In Spartan-6 a p-type dopant Boron is used during a production of silicon wafers because it diffuses at a rate that makes junction depths easily controllable. Unlike in other types of FPGA chips, the concentration of Boron in the Spartan-6 FPGA is high. Due to a nuclear reaction with the thermal neutrons, this might limit its use.

To test a functionality we irradiated one board in the total neutron fluence exceeded the foreseen values acquired during Belle II lifetime for a factor of 5. The irradiation at rates 700× higher than expected in the Belle II was performed in JSI TRIGA nuclear reactor, where the energy spectrum of the neutrons is similar to the one in the Belle II spectrometer [3]. During the irradiation the board was powered and

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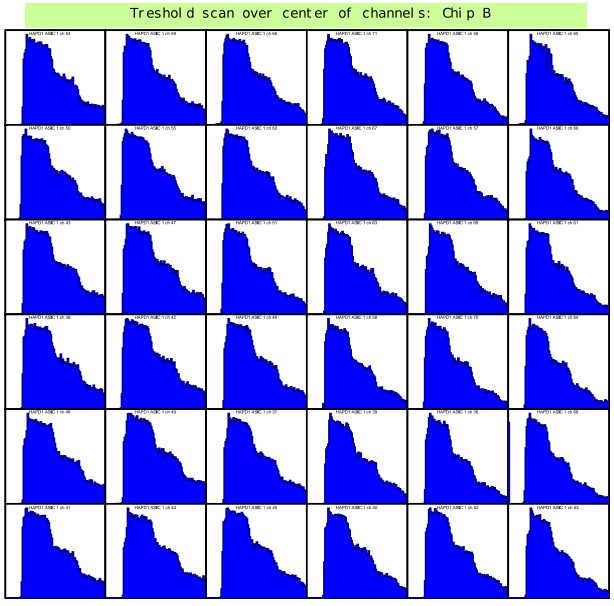

Fig. 3. HAPD sensor response to the short, low intensity light pulses as a function of discriminator threshold (36 channels of one of the 4 chips are shown). The noise, the single and the double photoelectron hits can be seen.

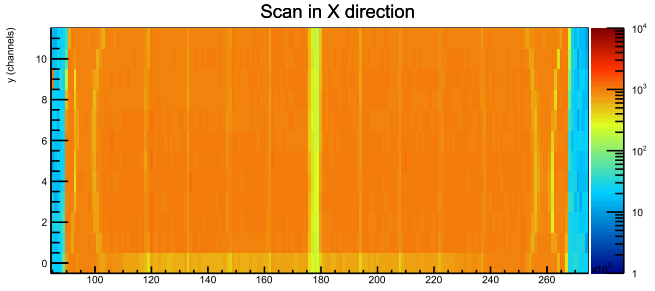

Fig. 4. Sensor surface response to the short, low-intensity light pulses. Due to a long measurement time, granularities in x- and *y*-direction differ.

constantly different checks were performed: a verification of the ASIC chip configuration parameters, a monitoring of the threshold voltages and temperatures, a test of the communication interface, and a counting of the bit changes in a static part of the firmware (Table 1). By extrapolating the results to the Belle II, the errors resulting in a possible malfunctioning of a single board are expected to happen about 8 times per hour. Part of the errors will be automatically repaired by employing Xilinx software mitigation controller while the unrecoverable errors are planned to be reset by uploading the fresh firmware and the operation parameters from a safe environment during the data taking.

Table 1
An irradiation test of a bit flips at neutron fluence rate of 3.275×10^6 n/cm^2/s and γ dose rate of 4.3 Gy/h. Measured bit flip rates in the reactor and extrapolated to the Belle II spectrometer are shown.

Bit flip direction	Rate [1/h]	Belle II rate [1/h]
$0 \rightarrow 1$	2488	7.5
$1 \rightarrow 0$	70.5	0.2

5. Conclusions

In the Belle II Aerogel Ring Imaging Detector a photon detector, consisting of 420 144-channel Hybrid Avalanche Photodetector Sensors (HAPD), each with a front-end electronic readout board and an HV-divider board at its back, is used to read the analog signals and transmit the serialized data from the HAPD sensors to the data acquisition system. After the complex design phase, all the components of the photon detector were manufactured and tested on the bench. The photon detector was constructed by carefully mounting the Sensor Modules, the power supply and the data cables in the mechanical frame. The photon detector was joined with the aerogel plane in the final RICH detector, successfully installed in the Belle II spectrometer in 2017. During a commissioning phase, all electronic components were gradually connected to the power supplies and to the data acquisition system. We confirmed the expected and adequate performance parameters of the front-end boards by registering the cosmic ray and beam collision events and thus expect an excellent performance of the RICH detector in the coming years.

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