The Front End Readout Electronics for the Hybrid Avalanche Photo Detector of the Belle II ARICH

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Abstract

In the forward end-cap of the Belle II spectrometer, the proximity focusing RICH with aerogel radiator will be installed for charged particle identification. At the back side of the Hybrid Avalanche Photo Detector (HAPD), a low power front end electronics board will be mounted. The board consists of a 11 layer PCB with 4 custom ASICs on the HAPD side and a FPGA on the other side. The front end board is designed to work in the 1.5 T magnetic field and withstand the 10 years of neutron irradiation. The 36 channel ASICs are responsible for amplification, shaping and discrimination of small (about 35000 e^-) single photo-electron signals. The Xilinx Spartan-6 FPGA samples the digitized signals and sends the data via optical link to the experiment common data acquisition cards. During the design, the functionality of the boards has been tested on the bench, in the test beam and during the neutron and gamma irradiation in the nuclear reactor. 420 front end boards were produced and tested prior the installation in the detector. In the presentation, we will present the module design, its functionality and the results of different tests.

The Belle II experiment in Tsukuba, Japan, will be dedicated to precision measurements of rare decays of B and D mesons and τ leptons [1]. In the forward end cap of the spectrometer, a proximity focusing RICH with aerogel radiator will be installed in the 28 cm space between the Central Drift Chamber and the Electromagnetic Calorimeter. Cherenkov photons, radiated by charged particles in the aerogel radiator, are detected by the photon detector consisting of 420 bi-alkali 144 channel HAPDs with the front end electronic boards at their back sides [1]. The front end readout board should be able to detect the 35000 e^- high signals which will during 10 years of operation gradually decrease due to irradiation. Because it is positioned in the strong magnetic field it should not include any magnetic materials. Since there is only about 8 cm available for the electronics and the connecting infrastructure, the front end readout boards are oriented parallel to the HAPD entrance window and should not exceed its size (75 mm $\times$ 75 mm). In addition the readout board should also supply the four bias and one guard voltage (175 V to 350 V) to the appropriate sensor pins.

The front end readout board consists of 11 layer PCB with a PGA connector for the HAPD photo sensor, power supply, bias and data I/O connectors and an optional connector for the test plug-in board with a PROM chip. Several different operating and reference voltages are generated by different LDOs. On the sensor side there are 4 custom ASICs. Each ASIC amplifies, shapes and digitize 36 input signals, protected from the overcurrents with two ESD protection diode stages. The operation of the ASIC chip is controlled by the internal registers which are together with the output digital signals connected to the Xilinx Spartan-6 FPGA clocked by either external or on-board 42 MHz oscillator. The FPGA controls the discriminator level of the ASIC via the on-board DACs, samples the digital signals and at the trigger signal serializes the data and send its through the data connector to the merger board, where the data are collected after the trigger signal from up to six front end boards and sent through the optical link to the experiment data acquisition card. From the merger board the FPGA firmware can be downloaded via dedicated JTAG lines. The FPGA also accepts the instruction commands via RX and responds via TX lines of the data IO cable. For the test and control of the board supply voltages, temperatures and monitoring analog and digital signals from different stages of ASIC, the board also has two multiplexers, an ADC and a temperature sensor. For debbuging purposes the board provides a test pulse, generated and controlled by the FPGA.

The firmware consists of an 64 bit instruction decoder, data sender and coommand receiver and response sender. The in-

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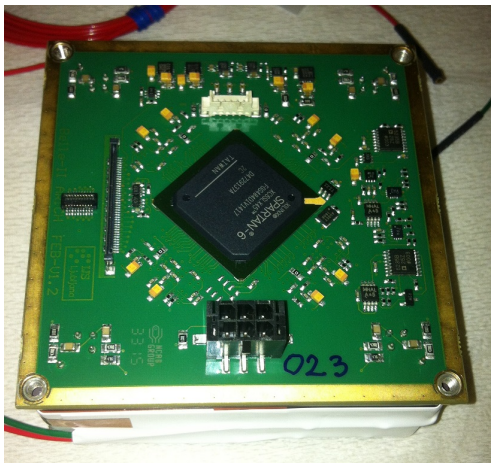

Figure 1: Photo of the front-end board attached to HAPD.

structions (commands + data) are received via one way asynchronous "SPI". Each received instruction is followed by a 64 bit response, encoded through a dedicated one way "SPI". The trigger signal starts the data encoder and sends the data through another one way "SPI".

Each hardware peripheral device has a driver triggered by the instruction decoder. In addition a data register is used to control the mode of operation, the sampling and encoder frequencies. The FPGA DNA is used as a unique identifier of the board.

The front end read-out board should be able to withstand the neutron fluence of 10^{12} 1 MeV equivalent n/cm^2 and gamma radiation dose of 100 Gy during the expected life time of Belle II spectrometer. The firmware core includes a Xilinx software SEU mitigation controller which corrects the SEUs and signals the unrecoverable errors through a separate line in the data bus. The signal enables the reload of the firmware and the operational parameters to the board from the safe environment.

The front end readout board has been developed in several iterations. 440 pcs has been produced and tested before and after the HAPD sensor attachment. The production of the boards was smooth with some difficulties in the placement of the 152 pin surface mount HAPD PGA connector, which has several through hole pins to gain mechanical stability during the service sensor detachments. After successful firmware download, the values of the operational voltage levels and the temperature sensor have been read out several times. The operational parameters were loaded and read back from the ASIC registers. We checked the response of the front end board to the noise, test pulses and triggered short green light pulses for different levels of the discrimination threshold.

More than 97% of the board were fully functional. About 1% of the boards were not usable, while 2% of the boards were potentially usable having one to several unconnected channels.

In the poster presentation, we will show the design of the board and the results of different operational tests. We will also show the results of a prototype of proximity focusing aerogel RICH, where the front end electronics were tested.

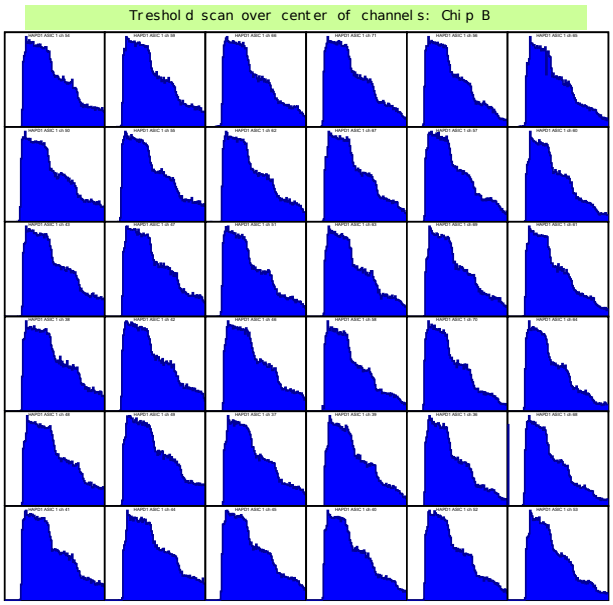

Figure 2: HAPD sensor response to short low intensity light pulses vs discriminator threshold (one of the 4 chips is shown). Noise, single and double photoelectron hits can be seen.

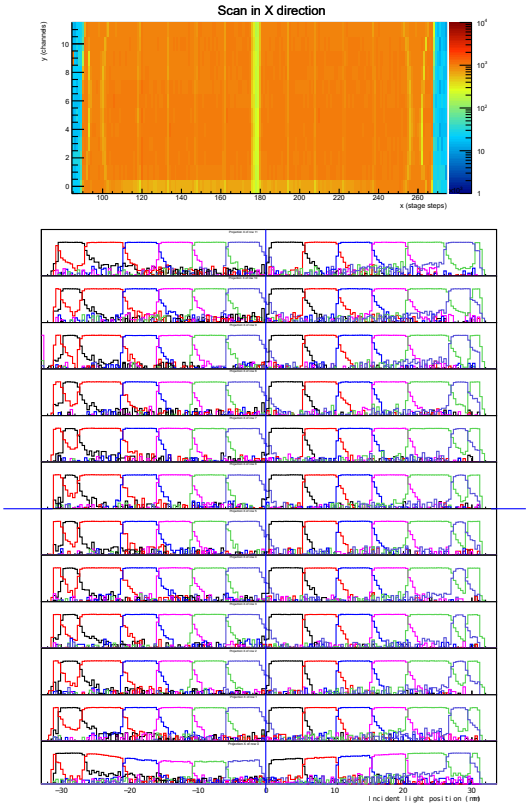

Figure 3: HAPD sensor response to short low intensity light pulses: Position sensitivity during linear scan of the surface of the HAPD sensor.

References

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