HS-C²MOS™ INTEGRATED CIRCUITS

PRELIMINARY DATA

SYNCHRONOUS PRESETTABLE 4-BIT COUNTER

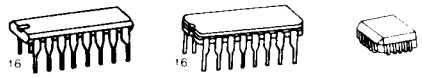
M54/74HC160 Decade, Asynchronous Clear
M54/74HC161 Binary, Asynchronous Clear
M54/74HC162 Decade, Synchronous Clear
M54/74HC163 Binary, Synchronous Clear

DESCRIPTION

The M54/74HC160, 161, 162 and 163 are high speed CMOS SYNCHRONOUS PRESETTABLE COUNTERS fabricated with silicon gate C²MOS technology.
They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
The M54/74HC160/162 are BCD Decade counters and the M54/74HC161/163 are 4 bit binary counters.
The CLOCK input is active on the rising edge. Both LOAD and CLEAR inputs are active on «L» level. Presetting of all four IC's is synchronous to the rising edge of CLOCK.
Clear function on the M54/74HC162/163 is synchronous to CLOCK, while the M54/74HC160/161 counters are cleared asynchronously.
Two enable inputs (TE and PE) and CARRY output are provided to enable easy cascading of counters, which facilities easy implementation of N-bit counters without using external gates.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES

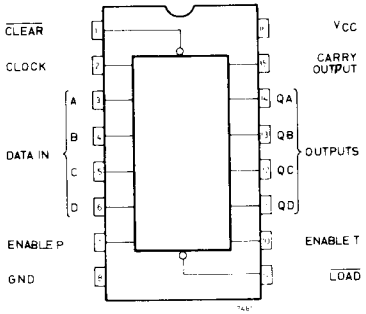
- High Speed
  f_{MAX} = 50 MHz (Typ) at V_{CC} = 5V
- Low Power Dissipation
  I_{CC} = 4 μA (Max.) at T_A = 25°C
- High Noise Immunity
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (Min.)
- Output Drive Capability
  10 LSTTL Loads
- Symmetrical Output Impedance
  $|I_{OH}| = I_{OL}$ = 4 mA (Min.)
- Balanced Propagation Delays
  $t_{PLH} = t_{PHL}$
- Wide Operating Voltage Range
  V_{CC} (opr) = 2V to 6V
- Pin and Function compatible
  with 54/74LS160 ~ 163



B1 Plastic Package
F1 Ceramic Package
C1 Chip Carrier

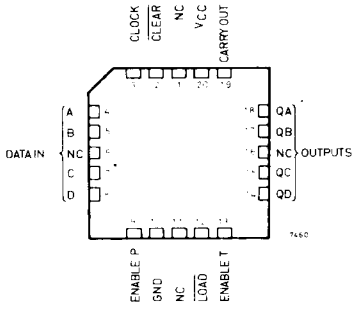
ORDERING NUMBERS: M54HCXXX F1
M74HCXXX B1
M74HCXXX F1
M74HCXXX C1

PIN CONNECTIONS
(top view)



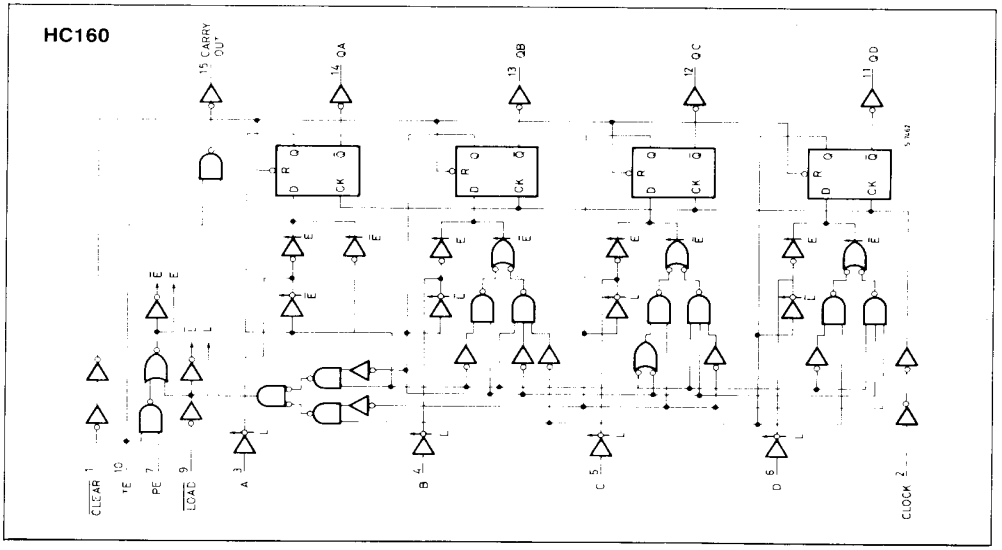
Dual in line

CHIP CARRIER

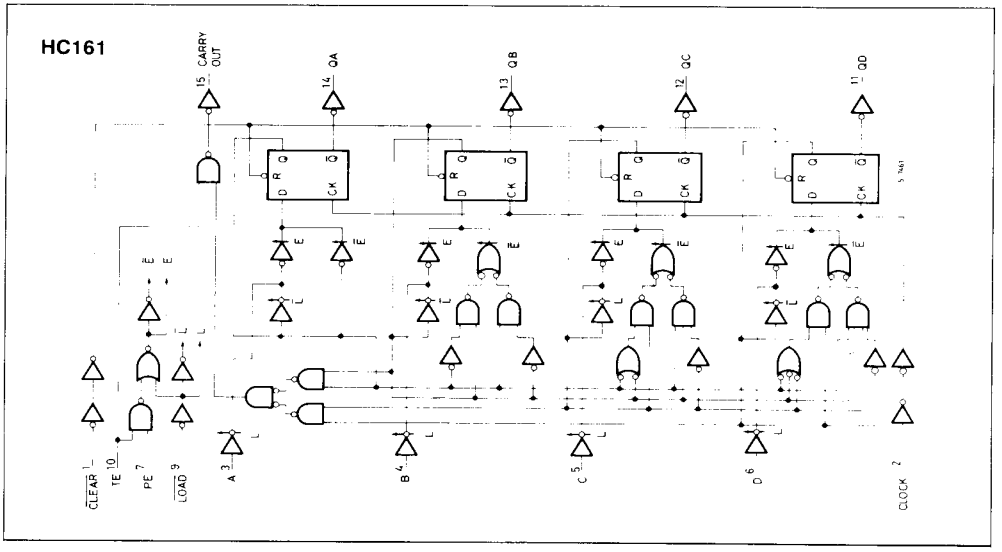


NC = No Internal Connection

LOGIC DIAGRAM

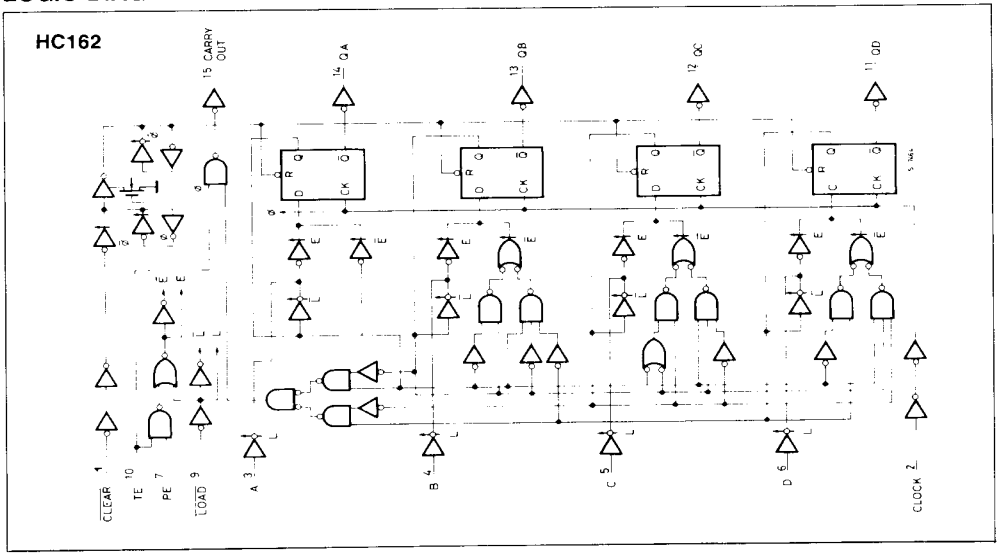


LOGIC DIAGRAM



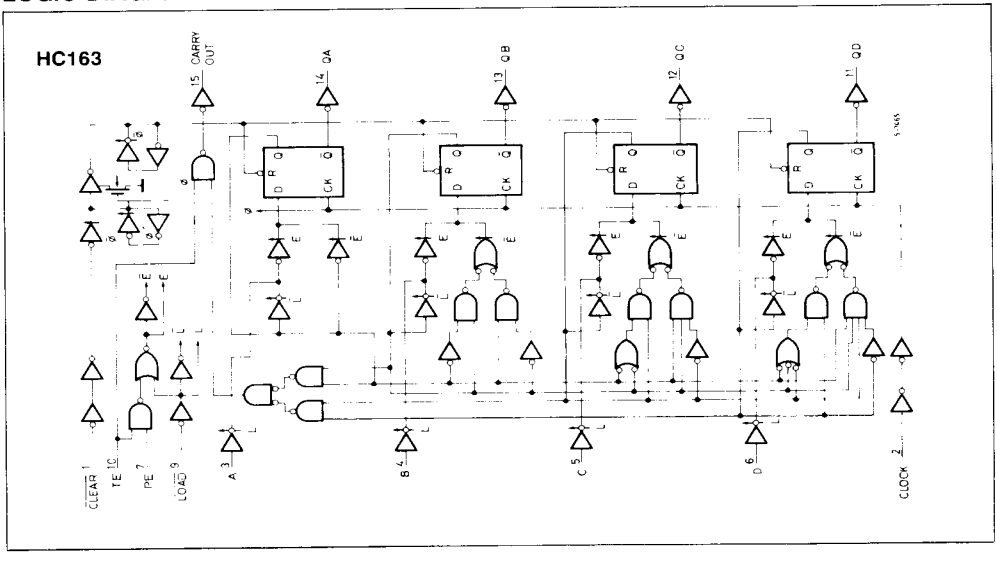
LOGIC DIAGRAM

HC162



LOGIC DIAGRAM

HC163



TRUTH TABLE

M54/74HC160/161					M54/74HC162/163					OUTPUTS				FUNCTION
INPUTS					INPUTS									
$\overline{CLR}$	$\overline{LD}$	PE	TE	CK	$\overline{CLR}$	$\overline{LD}$	PE	TE	CK	Q_A	Q_B	Q_C	Q_D	
L	*	*	*	*	L	*	*	*	↓	L	L	L	L	Reset to "0"
H	L	*	*	↓	H	L	*	*	↓	A	B	C	D	Preset Data
H	H	*	L	↓	H	H	*	L	↓	No Change				No Count
H	H	L	*	↓	H	H	L	*	↓	No Change				No Count
H	H	H	H	↓	H	H	H	H	↓	Count UP				Count
H	*	*	*	↑	*	*	*	*	↑	No Change				No Count

Note * ; Don't Care
A, B, C, D ; Logic level of data inputs
Carry : CARRY = TE · Q_A · $\overline{Q_B}$ · $\overline{Q_C}$ · Q_D ..... (M54/74HC160/162)
CARRY = TE · Q_A · Q_B · Q_C · Q_D ..... (M54/74HC161/163)

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limit	Unit
V_{CC}	Supply Voltage	2 to 6	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_A	Operating Temperature 74HC Series 54HC Series	− 40 to 85 − 55 to 125	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} 2 V: 0 to 1000 V_{CC} 4.5V: 0 to 500 V_{CC} 6 V: 0 to 400	ns

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0		1.5	—	—	1.5	—	1.5	—	V
		4.5		3.15	—	—	3.15	—	3.15	—	
		6.0		4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0		—	—	0.5	—	0.5	—	0.5	V
		4.5		—	—	1.35	—	1.35	—	1.35	
		6.0		—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I / I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}, −20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0		5.9	6.0	—	5.9	—	5.9	—	
		4.5	V_{IL}, −4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0	V_{IL}, −5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0		—	0	0.1	—	0.1	—	0.1	V
		4.5	V_{IH} or V_{IL}, 20 μA	—	0	0.1	—	0.1	—	0.1	
		6.0		—	0	0.1	—	0.1	—	0.1	
		4.5	V_{IL}, 4.0 mA	—	0.17	0.26	—	0.32	—	0.40	
		6.0	V_{IL}, 5.2 mA	—	0.18	0.26	—	0.32	—	0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND	—	—	±0.1	—	±1		±1	μA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND			4		40		80	μA

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C, C_L = 15pF, Input $t_r = t_f$ = 6ns)

Symbol	Parameter	54HC and 74HC			Unit
		MIN.	TYP.	MAX.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK-Q)		19	30	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK-CARRY)		22	35	ns
t_{PLH} t_{PHH}	Propagation Delay Time (TE-CARRY)		11	18	ns
t_{PHL}	Propagation Delay ($\overline{\text{CLEAR}}$-Q)*		21	33	ns
t_{PHL}	Propagation Delay Time ($\overline{\text{CLEAR}}$-CARRY)		24	38	ns
f_{MAX}	Maximum Clock Frequency	28	50		MHz
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CLOCK)		8	15	ns
$t_{W(L)}$	Minimum Pulse Width $\overline{\text{CLEAR}}$*		8	15	ns
t_s	Minimum Set-up Time LOAD, PE, TE		14	25	ns
t_s	Minimum Set-up Time A,B,C,D		8	15	ns
t_s	Minimum Set-up Time $\overline{\text{CLEAR}}$ **		8	15	ns
t_h	Minimum Hold Time		—	0	ns
t_{REM}	Minimum Removal Time $\overline{\text{CLEAR}}$ *		—	15	ns

* For HC160/161 only

** For HC162/163 only

AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, Input $t_r = t_f$ = 6ns)

Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			40 to 85°C 74HC		-55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0		—	30	75	—	90			ns
		4.5		—	8	15	—	18			
		6.0		—	7	13	—	16			
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK-Q)	2.0		—	75	165	—	200			ns
		4.5		—	22	33	—	40			
		6.0		—	19	28	—	34			
t_{PLH} t_{PHL}	Progation Delay Time (CLOCK-CARRY)	2.0		—	95	200	—	240			ns
		4.5		—	26	40	—	48			
		6.0		—	22	34	—	41			
t_{PLH} t_{PHL}	Progation Delay Time (TE-CARRY)	2.0		—	40	100	—	120			ns
		4.5		—	13	20	—	24			
		6.0		—	11	17	—	21			
t_{PHL}	Progation Delay Time (CLEAR-Q)	2.0		—	90	185	—	225			ns
		4.5		—	24	37	—	45			
		6.0		—	21	32	—	39			
t_{PHL}	Progation Delay Time (CLEAR - CARRY)	2.0		—	105	210	—	260			ns
		4.5		—	28	42	—	51			
		6.0		—	24	36	—	44			
f_{MAX}	Maximum Clock Frequency	2.0		5	9	—	4	—			MHz
		4.5		25	45	—	20	—			
		6.0		29	53	—	23	—			
$t_{W(L)}$ $t_{W(H)}$	Minimum Pulse Width (CLOCK)	2.0		—	30	75	—	90			ns
		4.5		—	8	15	—	18			
		6.0		—	7	13	—	16			
$t_{W(L)}$	Minimum Pulse Width (CLEAR *)	2.0		—	30	75	—	90			ns
		4.5		—	8	15	—	18			
		6.0		—	7	13	—	16			
t_s	Minimum Set-up Time (LOAD PE, TE)	2.0		—	50	125	—	150			ns
		4.5		—	14	25	—	30			
		6.0		—	12	22	—	27			
t_s	Minimum Set-up Time (A,B,C,D)	2.0		—	35	75	—	90			ns
		4.5		—	8	15	—	18			
		6.0		—	7	13	—	16			
t_s	Minimum Set-up Time (CLEAR**)	2.0		—	35	75	—	90			ns
		4.5		—	8	15	—	18			
		6.0		—	7	13	—	16			
t_h	Minimum Hold Time	2.0		—	—	0	—	0			ns
		4.5		—	—	0	—	0			
		6.0		—	—	0	—	0			
t_{REM}	Minimum Removal Time (CLEAR*)	2.0		—	—	75	—	90			ns
		4.5		—	—	15	—	18			
		6.0		—	—	13	—	16			
C_{IN}	Input Capacitance			—	5	7.5	—	7.5			pF
C_{PD} (*)	Power Dissipation Capacitance			—	57	—	—	—			pF

Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the following equation.
$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$ *: for M54/74HC160/161 only **: for M54/74HC162/163 only